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Transparent p-type SnO nanowires with unprecedented hole mobility among oxide semiconductors

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p-type tin monoxide (SnO) nanowire field-effect transistors with stable enhancement mode behavior and record performance are demonstrated at 160 °C. The nanowire transistors exhibit the highest field-effect hole mobility (10.83 $cm^2 V^{-1} s^{-1}$) of any p-type oxide semiconductor processed at similar temperature. Compared to thin film transistors, the SnO nanowire transistors exhibit five times higher mobility and one order of magnitude lower subthreshold swing. The SnO nanowire transistors show three times lower threshold voltages (−1 V) than the best reported SnO thin film transistors and fifteen times smaller than p-type Cu_2O nanowire transistors. Gate dielectric and process temperature are critical to achieving such performance. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4833541]

Among field-effect transistors (FET), thin-film transistors (TFTs), which employ a thin film layer of a semiconducting material as the active layer, have been used for decades as a crucial component in commercial displays.[1–4] Polycrystalline silicon (poly-Si) and amorphous silicon (a-Si) are widely used materials to fabricate the switching/driving TFTs for active matrix organic light emitting diode displays (AMOLED) and liquid-crystal displays (LCD), respectively.[1,2,5] Nevertheless, there are intrinsic properties like their lack of transparency, rigidity, low mobility (~1 $cm^2 V^{-1} s^{-1}$ for a-Si), or high processing temperature (poly-Si) that rules them out as alternatives for future display technologies, especially for the emerging transparent and flexible electronics.[6,7] Great efforts have been exerted recently in transparent transistor research to find semiconducting materials that can replace a-Si in backplane TFTs. With transparent TFTs being the fundamental building blocks of potential transparent electronics,[8,9] the suitable candidate(s) must have good optical transparency (>90% in the visible range), high material stability, excellent device performance (high carrier mobility, high on-to-off current ratio, moderate carrier density, low threshold voltage, low sub-threshold slope), and compatibility with existing TFT fabrication technologies.

Semiconducting metal oxides stand out as the most promising candidates for future display technologies and emerging transparent electronics owing to their wide optical band gap (E_g), chemical and mechanical stability, low temperature processing, and excellent device performance. Fully transparent and flexible TFTs with excellent device performance have been reported for different metal oxide semiconducting films.[7,8,10–12] Furthermore, nanowire (NW) field-effect transistors based on n-type oxides such as ZnO, SnO_2, In_2O_3, or other binary and ternary oxides have been also demonstrated to show even higher field-effect mobility (μ_{FE}) to that of poly-Si (150 $cm^2 V^{-1} s^{-1}$)[5,9,13–16] preserving the high optical transparency and material stability. The high mobility values reported for nanowire field effect transistors of different materials have been attributed to confinement-induced effects. Even though the exact mechanisms that produce higher mobility in nanowire FETs are not completely clear, Trivedi *et al.* have shown how increased quantum confinement results in high mobility p-Si nanobelts and nanowire transistors.[17] They have attributed their higher mobility values to a lower hole effective mass dispersion as the channel shrinks in dimension, i.e., holes with closer values of effective mass form the channel. Ju *et al.* have also suggested that a reduction in low-angle carrier scattering by the use of quasi-one dimensional structures might be an important mechanism for mobility enhancement.[5]

Among the promising p-type candidates are cuprous oxide (Cu_2O) and stannous oxide (SnO), which have been demonstrated as p-type active channel materials in TFTs fabricated by several methods[18–26] with the physical vapor deposited films exhibiting the best performance.[19] The PbO-type layered structure tin monoxide is now well known to be a transparent p-type semiconductor[27] with an indirect $E_g \sim 2.7$ to 2.9 eV.[25,26,28] Its intrinsic p-type character originates from the Sn^{2+} vacancy and with relatively high hole mobility attributed to the hybridized Sn 5*s* and O 2*p* orbitals near the valence band maxima.[27,28] The best reported mobility for TFTs fabricated with pure SnO is 1.3 $cm^2 V^{-1} s^{-1}$,[25] but it has recently been demonstrated that excess Sn metal in the SnO films can increase the mobility to above 6.0 $cm^2 V^{-1} s^{-1}$.[29]

Liao *et al.* have demonstrated p-type behavior in CuO and poly crystalline Cu_2O single NW-FETs grown by thermal oxidation of copper foils at 500 °C (for CuO)[30] and further reduction in hydrogen gas for Cu_2O conversion.[31] Their devices exhibited field-effect mobility around 5 and 95 $cm^2 V^{-1} s^{-1}$, respectively. Despite the impressive μ_{FE} of polycrystalline Cu_2O NW-FET, its high threshold voltage (V_T) ~ 15 V, low $E_g = 2.17$ eV, and high processing temperature make it less attractive for future applications. In contrast, the fabrication of field-effect functional devices using SnO nanoscale structures has not been yet demonstrated even though synthesis of SnO structures like nanosheets,[32] nanobelts,[33] and nano-rectangle strips[34] have been reported.

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Here we demonstrate the fabrication of transparent SnO nanowire field-effect transistors with stable and well-behaved enhancement-mode p-type behavior, and a maximum linear $\mu_{FE} = 10.83\ cm^2\ V^{-1}\ s^{-1}$, $V_T \sim -1$ V, I_{ON}/I_{OFF} ratio $> 10^3$ at a record low temperature for active channel crystallization of 160 °C. The single NW back-gate FET structure is depicted in Figure 1(a). Indium tin oxide (ITO)-coated glass is used as transparent substrate while the 150 nm thick ITO layer is used as a global gate. Atomic layer deposition (ALD)-derived high-k (220 nm) HfO_2 and ATO (a stacked multilayer of Al_2O_3 and TiO_2) are used as gate dielectrics. Electron beam lithography (EBL)-patterned SnO NW (from a 15 nm thick thin film) are used as a p-type semiconducting active, and the stack is completed by 8 nm Ti/ 80 nm Au source and drain (S&D) electrodes. SnO films were deposited from a 2 in. metal Tin target (99.99% purity) at an oxygen partial pressure (P_{O2}) of 3.12×10^{-2} Pa in an mixture of oxygen and argon gasses and a DC constant power of 30 W achieving a deposition rate of 0.8 Å s^{-1}. The single post-annealing treatment (150 °C, 160 °C, 170 °C) was performed after source and drain fabrication, in a tube furnace in air, in order to crystallize the SnO NWs as well as to improve the S&D contact to SnO.

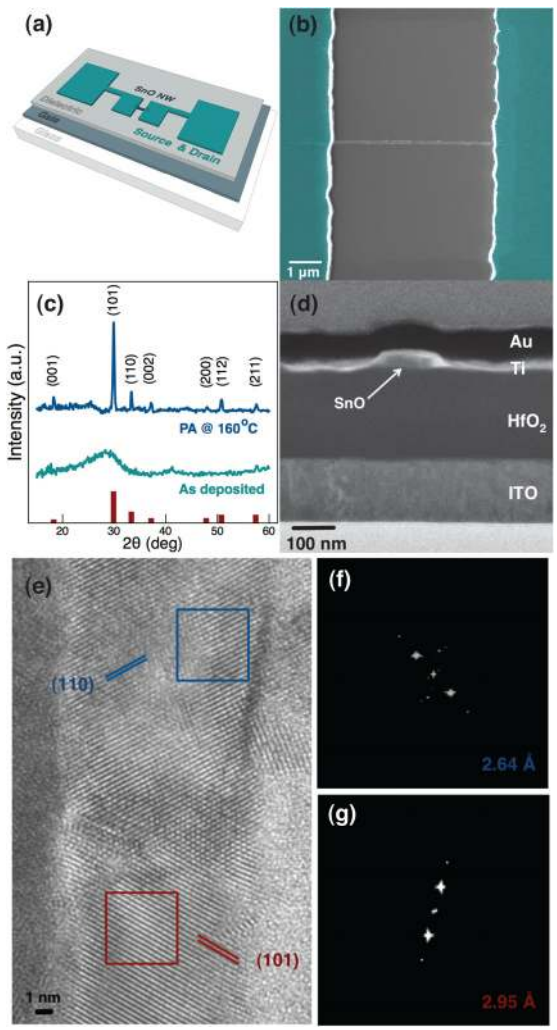

FIG. 1. (a) Conceptual design of the fabricated devices (150 nm ITO gate electrode/220 nm HfO_2/ATO gate dielectric/EBL-patterned SnO nanowire channel/8 nm Ti, 80 nm Au source and drain electrodes). (b) Top view scanning electron microscopy image of fabricated device with channel length of 5 μm and channel width defined by the nanowire planar width of 100 nm; (c) x-ray diffraction patterns of amorphous as-deposited SnO films and crystalline SnO films after annealing in air at 160 °C. The diffraction pattern of tetragonal SnO (JCPDS Card No. 06-0395) is shown by the red bars; (d) cross-sectional TEM image of the stack, showing the rectangular cross-sectional area of a 100 nm wide EBL-patterned structure; (e) HRTEM image of the SnO nanowire, viewed vertically. FFT analysis of the grains observed in the HRTEM image showing the interplanar spacing of the (g) (110) and (f) (101) lattices of tetragonal phase SnO.

Top view scanning electron microscopy (SEM) image of a NW-FET is shown in Figure 1(b) of a device with an effective channel length (L) of 5 μm and channel width (W) defined by the planar NW width of 100 nm. SEM images of the 200 nm and 500 nm devices are shown in Figure S1 of the supplementary material.[35] The as-deposited films are amorphous, but do crystalize after a post-annealing treatment in air, in a tube furnace at temperatures as low as 160 °C. Figure 1(c) shows X-ray diffraction (XRD) patterns of as-deposited amorphous and crystallized SnO films showing the presence of single-phase tetragonal SnO. The optimized tin monoxide layer is polycrystalline with an extracted crystallite size of 10–15 nm as confirmed by transmission electron microscopy (TEM) analysis. The SnO films themselves are transparent with an average optical transmission of 92% in the visible region of the electromagnetic spectrum (400 nm–700 nm), as shown in Figure S2 of the supplementary material.[35] Figure 1(d) shows a cross-sectional TEM image of the stack, showing the rectangular cross-sectional area of a 100 nm wide EBL-patterned structure. Figure 1(e) corresponds to a high-resolution TEM (HRTEM) image showing the polycrystalline nature of the nanowire. Figures 1(f) and 1(g) show the fast Fourier transformation (FFT) analysis of the SnO grains observed in the HRTEM image showing the interplanar distance of 2.64 Å and 2.95 Å, consistent with the (110) and (101) lattices of the tetragonal SnO phase.

Figure 2 shows the characteristic transistor curves for the best performing devices, which correspond to FETs fabricated using HfO_2 as the gate dielectric and post-annealed at 160 °C. Figures 2(a)–2(c) show the output characteristics of the 100 nm, 200 nm, and 500 nm NW-FET, respectively. No current crowding at low drain-source voltage (V_{DS}) is observed, showing Ohmic contact with the Ti/Au source and drain contacts. The well-behaved output curves exhibit a clear pinch-off and current saturation for all the FETs when operating in the negative V_{DS} region. p-channel operation is confirmed by the transfer characteristics shown in Figure 2(d) since drain-source current (I_{DS}) increased in all the tested devices when a negative gate-source voltage (V_{GS}) was applied at a fixed $V_{DS} = -1$ V. Multiple dual-sweep I_{DS}-V_{GS} were obtained for several devices for each channel geometry and all curves show comparable behavior, with consistent on-off current ratio (I_{ON}/I_{OFF}), sub-threshold swing (*SS*), linear-region field-effect mobility (μ_{FE}), and threshold voltage (V_T) values.

Multiple dual-sweep characterization was performed following the recommendations by Wager,[36] and it was found that all the measured devices exhibit *non-equilibrium, steady state behavior*: dual-sweep log (I_{DS})-V_{GS} transfer characteristics show hysteresis and retraceable positive-going and negative-going behavior after multiple scans. I_{DS} increased for all FETs when a negative V_{GS} was applied, exhibiting enhancement-mode operation ($I_{DS} \approx 0$ at $V_{GS} = 0$) as shown in

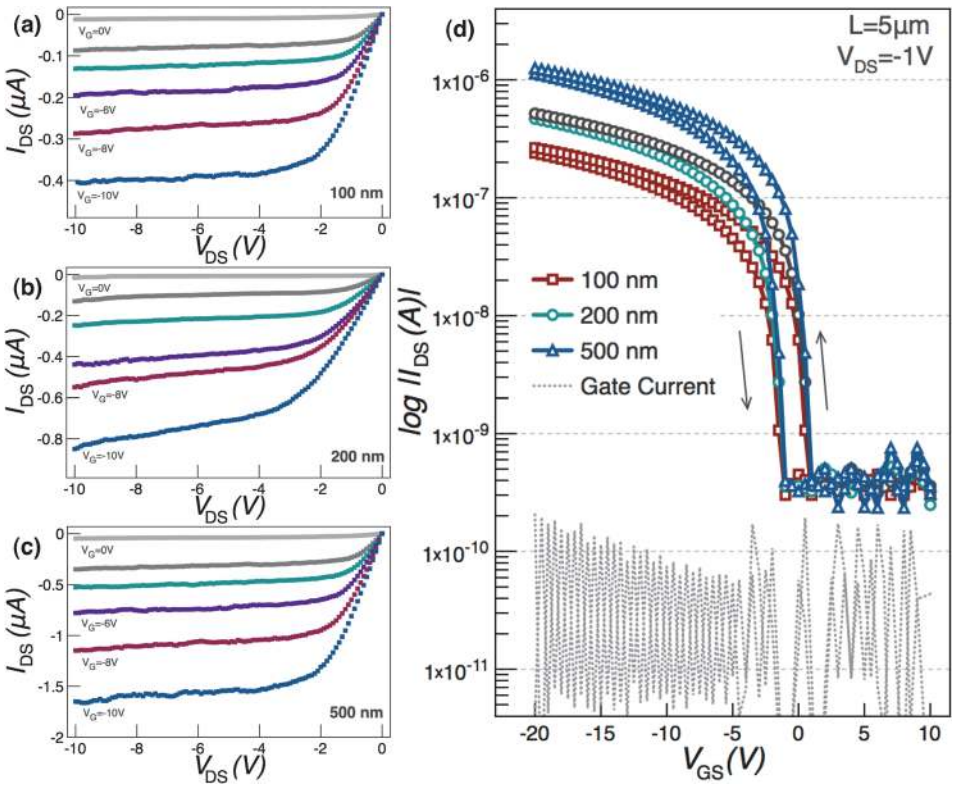

FIG. 2. Output characteristics of (a) 100 nm, (b) 200 nm, and (c) 500 nm nanowire transistors (NW-FETs), respectively. (d) Transfer characteristics of NW-FETs annealed at 160 °C as a function of nanowire width when using HfO_2 as the gate dielectric.

the output characteristics of Figure 2. The off-current is $<4 \times 10^{-10}$ A for all devices while the gate leakage is $<3 \times 10^{-10}$ A reflecting the good insulating properties of the HfO_2 gate dielectric. A maximum μ_{FE} of 10.83 $cm^2 V^{-1} s^{-1}$, 10.58 $cm^2 V^{-1} s^{-1}$, and 10.30 $cm^2 V^{-1} s^{-1}$ for the 100 nm, 200 nm, and 500 nm devices, respectively, with $V_T \sim -1$ V, $SS \approx 0.74$ $Vdec^{-1}$, and effective hysteresis density of $N_{HYS} \approx 7.5 \times 10^{11}$ cm^{-2} was achieved for FETs annealed at 160 °C as extracted from the transfer characteristics displayed in Figure 2(d).

The single phase SnO TFTs deposited at $P = 1.8$ mTorr and 13% O_{PP} showed more inferior performance compared to the nanowire FET (μ_{FE} of 1.87 *vs* 10.83 $cm^2 V^{-1} s^{-1}$), clearly demonstrating the effectiveness of nanoscaling. Table I shows the important device parameters comparing the NW FET and TFT devices fabricated with 15 nm thick of the same single-phase SnO film and same gate (ITO) and gate dielectric (HfO_2) materials. It is clear from the data in Table I that the 1-D structure (nanowire) results in substantially improved device performance. The NW-FET has 5 times higher mobility, three time smaller threshold voltage, which is also closer to zero (−3.66 V for TFT to around −1 V for NW-FET), lower I_{OFF}, and lower density of interfacial trap states (D_{it}) extracted from the *SS*. Furthermore, the NW devices show enhancement-mode operation in contrast to depletion-mode behavior of TFTs. It is important to highlight that the *SS* for the nanowire FET is one order of magnitude lower than the thin film device (7.65 $Vdec^{-1}$ for the TFT and 0.70 $Vdec^{-1}$ for the NW-FET), which gives a clear indication of the dramatic reduction in the density of interfacial trap states for nanoscale channel dimensions. The reduction in the I_{OFF} when compared to the TFTs indicates the reduction of the surface defects (e.g., additional oxygen), which is advantageous to maximize device performance. Our optimized post annealing temperature for the best TFT performance is 180 °C, but for the NW-FET, the best performance is observed at 160 °C. This small temperature difference is crucial to avoid additional oxygen incorporation into the film, and hence we get a better mobility. TFTs annealed at 160 °C show very poor performance, most likely attributed to the incomplete crystallization of the SnO channel. The higher annealing temperature of TFTs allows additional oxygen to go into the exposed SnO surface contributing to an oxygen-rich surface and hence a higher off current. The smaller dimensions of the SnO nanowires allow their complete crystallization at lower temperature, which in turn reduces the likelihood of an oxygen-rich surface formation. The transfer characteristics of TFT and the 500 nm NW-FET are depicted in Fig. S3 of the supplementary material.[35] In order to rule out narrow and short channel effects in the nanowire FETs, at least 10 devices of each NW width were tested showing consistent results.

The important FETs parameters are summarized in Figure 3 as a function of NW width and post-annealing

TABLE I. Performance comparison of NW-FET and TFT devices fabricated using the same single-phase SnO material.

	NW FET			TFT
	100 nm	200 nm	500 nm	W/L = 50 × 50 μm
μ_{FE} ($cm^2 V^{-1} s^{-1}$)	10.83	10.58	10.30	1.87
V_T (V)	−1.06	−1.08	−1.20	−3.66
I_{OFF} (A)	4×10^{-10}	4×10^{-10}	4×10^{-10}	1×10^{-9}
ΔV_{ON} (V)	1.99	2.07	2.03	3.61
SS ($Vdec^{-1}$)	0.76	0.69	0.60	7.65
D_{it} ($eV^{-1} cm^{-2}$)	4.45×10^{12}	4.00×10^{12}	3.43×10^{12}	4.82×10^{13}
N_{HYS} (cm^{-2})	7.42×10^{11}	7.72×10^{11}	7.57×10^{11}	1.35×10^{12}

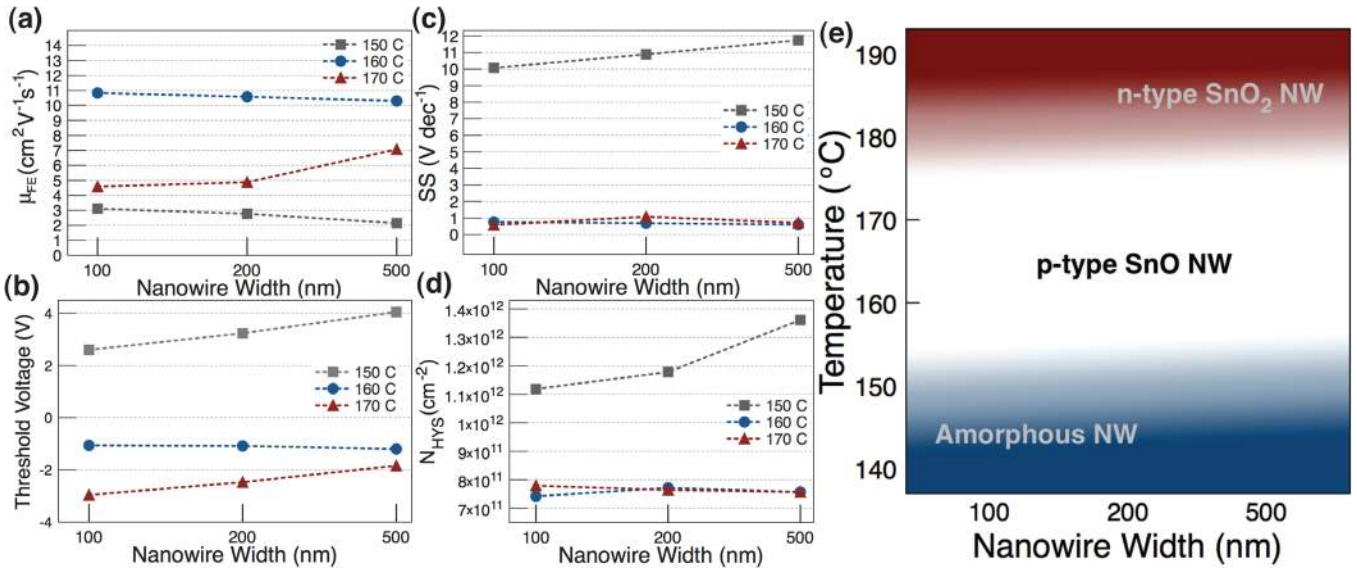

FIG. 3. Important NW-FET parameters measured as a function of nanowire width and anneal temperature: (a) field-effect mobility (μ_{FE}); (b) threshold voltage (V_T); (c) subthreshold swing (SS); (d) effective hysteresis density (N_{HYS}). All devices shown here were fabricated using HfO_2 gate dielectric. (e) Process map depicting process conditions where p-type conduction is observed in SnO NW FETs.

temperature for devices fabricated using HfO_2 as gate dielectric. Output and transfer characteristics are shown in Figure S4 of the supplementary material.[35] At 150 °C SnO is not completely crystallized (as shown in TEM, Fig. S5 (Ref. 35)), so the devices show a rather modest μ_{FE} (Fig. 3(a)), positive V_T (Fig. 3(b)), large SS (Fig. 3(c)), and high N_{HYS} (Fig. 3(d)). The last two parameters reflect a high density of trap states in the SnO channel (SS) and the SnO/HfO_2 interface (N_{HYS}), which significantly reduces as the annealing temperature increases. At 160 °C and 170 °C, SS reduces from around 11 Vdec^{-1} at 150 °C to an average of 0.74 Vdec^{-1} (Fig. 3(c)), showing that once the active layer is completely crystallized the SnO/HfO_2 interface is of relatively high quality. This statement is confirmed in Fig. 3(d), where the N_{HYS} is nearly the same for all devices annealed at 160 °C and 170 °C. Nevertheless, the mobility and threshold voltage degrades at temperatures higher than 160 °C, as observed for devices annealed at 170 °C. The devices convert to weak n-type conduction when annealed at 180 °C (not shown) and mainly attributed to the oxygen disproportionation mechanism[37] in which the incorporation of excess oxygen into SnO causes a transformation to an oxygen-deficient SnO_2 phase. In summary, at 150 °C the SnO NWs are not completely crystallized, at 160 °C they show the best p-type performance, at 170 °C they are affected by additional oxygen incorporation, and at 180 °C they exhibit weak n-type conduction as summarized in Figure 3(e).

Figure 4 compares the important FET parameters for devices fabricated at the best performance condition when using HfO_2 and ATO as gate dielectric. μ_{FE} on ATO is around half of the μ_{FE} on HfO_2 while there is no clear trend on V_T as shown in Fig. 4(a). The I_{ON}/I_{OFF} ratio is in general one order of magnitude higher on HfO_2 (10^3) as shown in Fig. 4(b). The gate leakage current of ATO is as high as 3×10^{-9} A, which significantly affects the device off current, thus reducing the I_{ON}/I_{OFF} ratio. Figure 4(c) shows the huge difference in the SS for both dielectrics, indicating a much better interface formation between the SnO and HfO_2, which is also confirmed by the lower N_{HYS} (Fig. 4(d)) extracted from devices fabricated on HfO_2. Despite the fact that these two high-k oxides have comparable dielectric constant (~14 for HfO_2 and ~15 for ATO, and similar C_{ox} was used), the low V_T, SS, and N_{HYS} of devices fabricated on HfO_2 compared to the higher variability of V_T as a function of NW width, higher SS, N_{HYS}, and gate leakage current of devices on ATO shows that SnO/HfO_2 interface is more suitable for maximizing device performance. The relatively poorer performance on ATO seems to arise from the higher

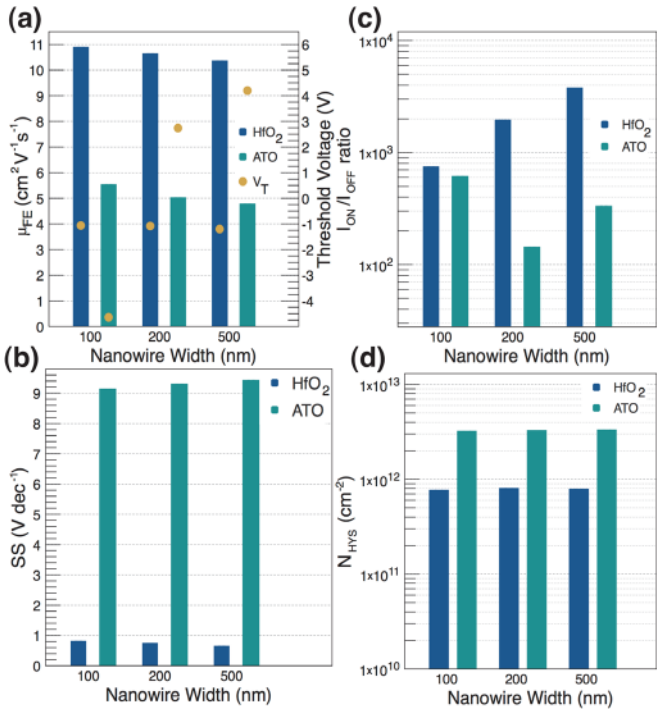

FIG. 4. Effect of gate dielectric material on the performance of NW-FETs fabricated at the optimum anneal temperature (160 °C). (a) Field-effect mobility (μ_{FE}) and threshold voltage (V_T); (b) subthreshold swing (SS); (c) on-to-off current ratio (I_{ON}/I_{OFF}); (d) effective hysteresis density (N_{HYS}).

density of trap states at the SnO/ATO interface as well as from the degradation of ATO during the fabrication process caused mainly by e-beam exposure during the active patterning.

We have demonstrated the fabrication of transparent p-type SnO NW-FETs with unprecedented performance at low process temperatures (160 °C). The SnO NW-FETs exhibit the highest reported field-effect hole mobility ($10.83\ cm^2\ V^{-1}\ s^{-1}$) of any p-type oxide semiconductor processed at such low temperature. Compared to thin film transistors (TFTs) using the same SnO film, the NW-FETs exhibit five times higher mobility and one order magnitude lower subthreshold slope. In addition, the SnO nanowire FETs show exceptionally low threshold voltages (~ -1 V), which is nearly three times smaller than the thin film device. We have also shown that the use of HfO_2 as gate dielectric increases SnO nanowire device mobility due to a better dielectric/semiconductor interface with reduced trap states.

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