Trapping Effects and Microwave Power Performance in AlGaN/GaN HEMTs

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***Abstract*—The dc, small-signal, and microwave power output characteristics of AlGaN/GaN HEMTs are presented. A maximum drain current greater than 1 A/mm and a gate-drain breakdown voltage over 80V have been attained. For a 0.4 μm gate length, an f_T of 30 GHz and an $f_{\max}$ of 70 GHz have been demonstrated. Trapping effects, attributed to surface and buffer layers, and their relationship to microwave power performance are discussed. It is demonstrated that gate lag is related to surface trapping and drain current collapse is associated with the properties of the GaN buffer layer. Through a reduction of these trapping effects, a CW power density of 3.3 W/mm and a pulsed power density of 6.7 W/mm have been achieved at 3.8 GHz.**

***Index Terms*—GaN, HEMT, heterojunction, microwave transistor, MODFET, trapping.**

I. Introduction

GAN-BASED microwave power HEMTs have defined the state-of-the art for output power density [1], [2] and have the potential to replace GaAs-based transistors for a number of high-power applications. The GaN-based material system, consisting of GaN, AlN, InN and their alloys, has become the basis of an advanced, microwave-power-device technology for a number of reasons. GaN has a breakdown field that is estimated to be 3 MV/cm [3], which is ten times larger than that of GaAs, and a high peak electron velocity of 2.7×10^7 cm/s [4]. In addition, this material system is capable of supporting a heterostructure device technology with a high two-dimensional electron gas (2-DEG) carrier density and mobility. As a result of these properties, excellent high-frequency, high-power performance has been achieved with GaN-based HEMTs.

Although significant progress has been made in the past few years, additional developmental work is required for GaN HEMTs to become a viable technology [5]. One area of active research deals with the reduction of trapping effects in GaN-based devices. Historically, a variety of trapping effects have been observed. These include transconductance frequency dispersion [6], current collapse of the drain characteristics [7], light sensitivity [7], gate- and drain-lag transients [8]–[10], and restricted microwave power output [11], [12]. The research activity that is directed toward understanding and eliminating these effects parallels that of the GaAs-based technology, where previously significant attention was directed toward the minimization of trapping effects [13]–[15]. In this paper, the dc, small-signal, gate- and drain-lag, and microwave power output characteristics of GaN-based field-effect transistors are presented. The relationships between the measured drain current transients, microwave power output, and the device surface and buffer layer properties are discussed.

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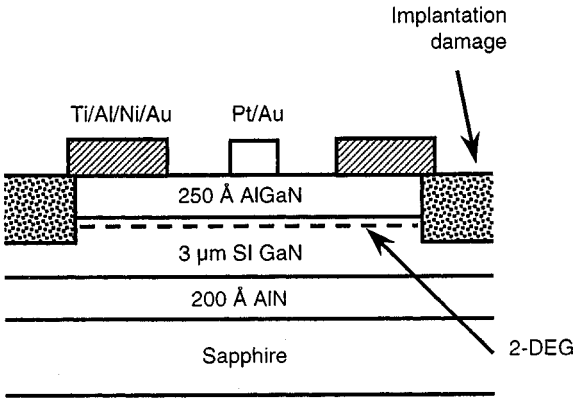

Fig. 1. Typical AlGaN/GaN HEMT cross section.

II. Materials Growth and Device Fabrication

A representative device cross section is shown in Fig. 1. The epitaxial layers used in this work were grown on sapphire by MOCVD, using parameters reported elsewhere [16]. The AlGaN/GaN HEMT structures consist of a 3 μm thick, undoped, high-resistivity GaN buffer layer grown on a 200 Å low-temperature AlN nucleation layer. The thick buffer layer was employed to spatially remove the active part of the device from the higher-defect-density material near the substrate interface. An AlGaN layer with a nominal thickness of 250 Å and a nominal Al composition of 30% was grown on the GaN buffer. Devices with and without Si doping in the AlGaN layer were studied, but less than 10% of the 2-DEG sheet carrier concentration (n_{sh}) is attributed to Si doping due to the strong piezoelectric effect in this material system [17]. For the starting material considered here, n_{sh} values as high as 1.2×10^{13} cm^{-2} with a Hall mobility of 1460 cm^2/V-s have been demonstrated at 300 K. In the devices discussed in this paper, the source-drain spacings are 2 to 4 μm and gate lengths are 0.2 to 1 μm. The gate metallization was defined with electron beam lithography. The ohmic contacts are alloyed

Ti/Al/Ni/Au and have a contact resistance as low as 0.4 Ω-mm. The gate metallization is Pt/Au (100/3000 Å). Either He or N implantation-induced damage was used for device isolation [18]. The ion implant isolation procedure results in a planar wafer surface and avoids the possibility of increased leakage current due to the gate metal contacting the 2-DEG as it crosses the mesa edge in a mesa isolation process.

Some of the HEMTs considered in this study were passivated with silicon nitride, denoted in this paper SiN. In that case, the nitride was deposited after the ohmic alloy, implant isolation, and gate metal deposition processing steps were completed. A low-temperature, plasma-enhanced chemical vapor deposition process using SiH_4 and NH_3 was used to deposit the nitride with a thickness of 1200 Å and an index of refraction of 1.8. In the samples studied to date, the nitride passivation leads to a 20% increase in n_{sh} as determined from Hall measurements. At present, the reasons behind this increase are uncertain, but it is probably due to a reduction of surface depletion effects or an additional charge contribution from the deposited nitride layer.

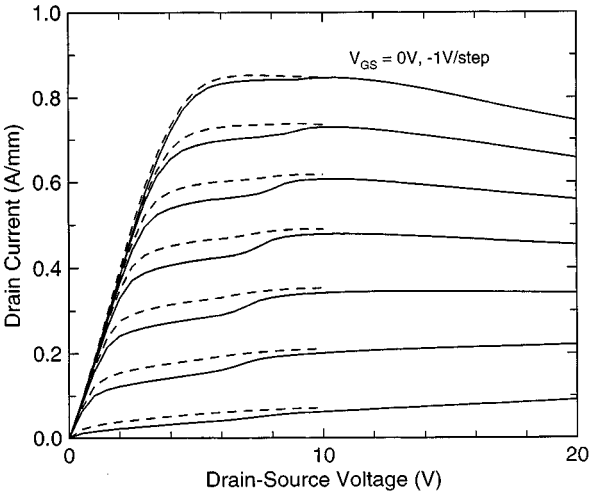

Fig. 2. Drain characteristics for a HEMT with a 250 Å AlGaN layer and a width of 50 μm. The drain characteristics indicated by the dotted lines are for V_{DS} restricted to <10 V and the solid lines are for V_{DS} up to 20 V.

III. DC Characterization

The drain characteristics for a GaN HEMT with a 250 Å Si-doped AlGaN layer are shown in Fig. 2. The AlGaN thickness was determined from capacitance-voltage (*C–V*) measurements. These characteristics were measured with an HP4145B semiconductor parameter analyzer. In this figure, two sets of characteristics are shown for the same device. The characteristics indicated by the dashed lines are the result when the maximum V_{DS} is restricted to 10 V, whereas the solid lines are the characteristics that are measured when the maximum V_{DS} is 20 V. By comparing these characteristics, a reduction in drain current for $V_{DS} < 8$ V is noted. This reduction in current after the application of a high drain voltage is referred to as current collapse. This effect is similar to that reported for GaN MESFETs and is attributed to hot electron injection and trapping in the buffer layer [7], [19]. At a high drain voltage, electrons are injected into the GaN buffer layer, where they are trapped. This trapped charge depletes the 2-DEG from beneath the active channel and results in a reduction in drain current for subsequent V_{DS} traces. The trapped charge can be released through illumination or thermal emission. The gradual reduction in current for $V_{DS} > 10$ V, seen in Fig. 2, is attributed to self-heating.

The effect of SiN passivation on the drain characteristics is shown in Fig. 3. These characteristics are for the same device before and after SiN passivation. The drain current is increased as a result of the increase in n_{sh}. It can be seen that the reduction in current associated with the current collapse phenomenon is unaffected. This is consistent with our proposed mechanism for current collapse, i.e., hot electron injection and trapping in the buffer layer without surface involvement.

The transfer characteristics of the device shown in Fig. 2 and a device with a 200 Å AlGaN layer are shown in Fig. 4. Maximum drain currents, $I_{\max}$, (measured at a forward gate current of 1 mA/mm) of $>$1.0 A/mm are obtained. To obtain high $I_{\max}$ values, tight source-drain spacings are required [20]. It can be seen from the figure that the thicker AlGaN layer results in a lower, but flatter transconductance curve. This result is consistent with the gate electrode being further away from the 2-DEG. The maximum g_m for the device with the 200 Å AlGaN layer is 220 mS/mm.

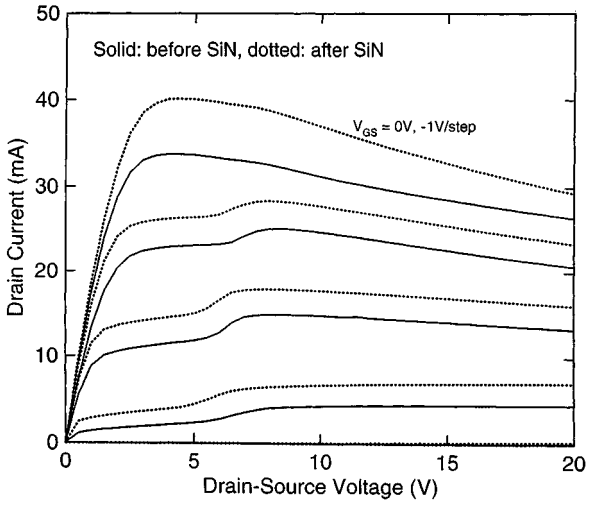

Fig. 3. Measured drain characteristics before and after SiN passivation.

The gate-drain current–voltage (*I–V*) characteristic for the device with the 200 Å AlGaN layer is given in Fig. 5. The gate-drain reverse breakdown voltage is greater than 80 V with a leakage current less than 0.01 mA/mm. These dc characteristics demonstrate the clear advantages of the GaN technology to support high drain currents in conjunction with very large gate breakdown voltages.

IV. Small-Signal Performance

The S-parameters of these devices were measured as a function of frequency and bias using on-wafer probing. The corresponding current gain, $|h_{21}|$, maximum stable gain, MSG, and

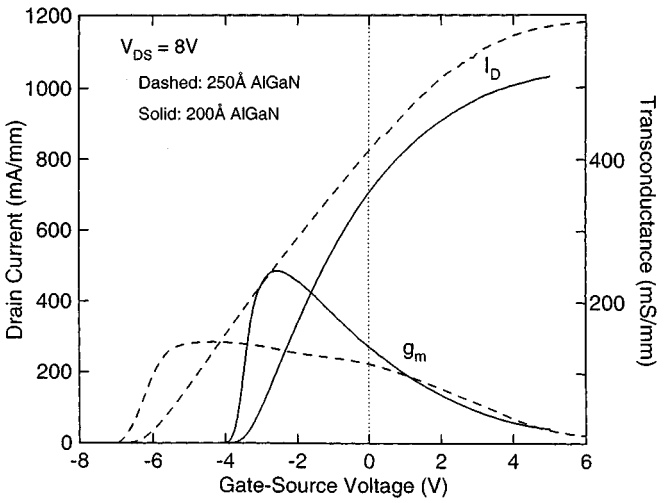

Fig. 4. HEMT transfer characteristics. The following Hall properties were determined from on-wafer test patterns: 250 Å AlGaN layer, $R_{sh} = 360\ \Omega/\square$, $\mu = 1460$ cm^2/V-s, and $n_{sh} = 1.2 \times 10^{13}$ cm^{-2}; 200 Å AlGaN layer, $R_{sh} = 490\ \Omega/\square$, $\mu = 1460$ cm^2/V-s, and $n_{sh} = 8.8 \times 10^{12}$ cm^{-2}.

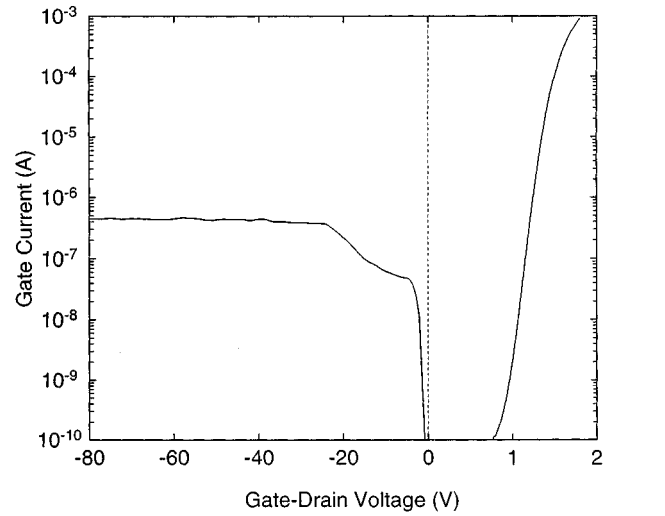

Fig. 5. Gate-drain *I–V* characteristics for the HEMT with the 200 Å AlGaN layer. The device width is 50 μm. The forward voltage scale is expanded for clarity.

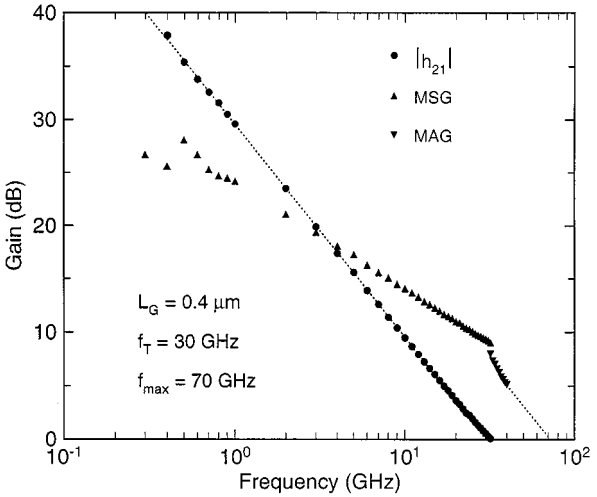

Fig. 6. Short-circuit current gain, maximum stable gain, and maximum available gain obtained from measured S-parameters.

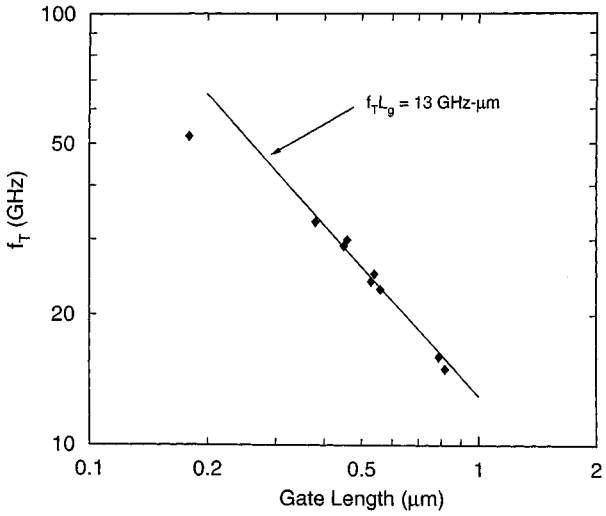

Fig. 7. Cut-off frequency, f_T, as a function of gate length for several HEMTs.

maximum available gain, MAG, are given as a function of frequency in Fig. 6 for a 0.4 μm gate length for the wafer with the 200 Å AlGaN layer. The usual 6 dB/octave extrapolation yields f_T and $f_{\max}$ values of 30 and 70 GHz, respectively. These results were measured on unpassivated devices. It was found that for the typical wafer, the small-signal response was not significantly affected by passivation.

In Fig. 7, f_T is plotted as a function of gate length, L_g. The solid line fit to these data corresponds to an $f_T \times L_g$ product of 13 GHz-μm. This small-signal high-frequency performance is comparable to that of GaAs MESFETs. The effective electron velocity, v_{eff}, was determined to be 8×10^6 cm/s from the relationship $v_{\text{eff}} = 2\pi L_g f_T$. This value is comparable to that reported elsewhere [21].

V. Drain Current Transients

An estimate of the maximum microwave power output obtainable from an FET can be determined from the dc drain characteristics and the operating point. It is frequently observed, however, that the microwave power output of GaN HEMTs is significantly less than that predicted from this estimate [11], [12]. This discrepancy is due in part to trapping effects. The responsible trapping centers could be located in several regions, including the GaN buffer layer, the AlGaN barrier layer, and the AlGaN surface. Buffer trapping results in lower power output as a result of an increase in the knee voltage and a reduction in $I_{\max}$. Surface trapping leads to a slower large-signal response time and restricted microwave power output because the drain current can not follow the applied ac gate signal. We have employed gate lag (I_D response to a V_{GS} pulse) and drain lag (I_D response to a V_{DS} pulse) measurements in an effort to identify trap locations. In general, as established with the conventional

III–V technologies, gate lag measurements are more sensitive to surface effects and drain lag measurements are more sensitive to buffer layer effects [13]–[15]. Our findings, reported below, are consistent with this behavior.

A. Gate Lag Measurements

Two extremes in gate lag response that have been observed in our GaN HEMTs are shown in Fig. 8. It is important to note that both curves in Fig. 8 are for the same device, but before (curve B) and after (curve A) SiN passivation. In these measurements, V_{GS} is pulsed from the threshold voltage, V_{th}, to 0 V while V_{DS} is held constant at a low-field value to avoid the complications of device heating. In the figure, the drain current value is normalized to I_{DSS}. Obviously, very limited drain current response occurs before passivation and nearly ideal response occurs afterwards. It should be noted that the pulse length used in this measurement is short relative to the time constant of the gate lag. If much longer pulses are used, both curves, A and B, will approach unity, i.e., I_{DSS}. In general for unpassivated devices in this study, a gate lag response that covers the range between these two extremes has been observed, but the results are highly variable [12].

Gate lag is usually attributed to surface states that act as electron traps located in the access regions between the metal contacts. The trapped electrons deplete the 2-DEG in the access regions of the device, thereby limiting the current. Although additional study is necessary to establish with certainty that surface states are involved in the gate lag phenomenon in GaN HEMTs, the observation that the gate lag response dramatically improves after deposition of a SiN dielectric layer strongly supports the surface trapping explanation. We have previously reported that gate lag is correlated with microwave output power in samples that did not have nitride passivation [12]. The effect of nitride passivation on microwave power output is discussed in more detail later in this paper.

B. Drain Lag Measurements

The current collapse phenomenon, defined earlier, has a characteristic time dependence. After a sufficient time lapse, the normal drain current characteristics are restored through thermal emission of the trapped charge in the buffer layer. The temporal response of the current collapse can be investigated with drain lag measurements. In addition to establishing the time dependence, drain lag measurements are also useful for quantifying this effect since devices that exhibit minimal current collapse also exhibit minimal drain lag.

Drain lag measurements for several devices are shown in Fig. 9. For these measurements, the device is taken from an equilibrium condition at a low V_{DS} value (10–100 mV) to a high V_{DS} value (15–20 V) and then returned to the low V_{DS} value. V_{GS} is maintained at 0 V. The plotted drain current is normalized to the low-field value. A typical long-term drain lag characteristic is given by curve A. The recovery time is on the order of minutes. This device has a drain lag ratio, DLR, (the ratio of the I_D values immediately before and after the application of the high drain bias) of 0.85. Significantly lower DLR values have been measured. For device B, the DLR is 1.

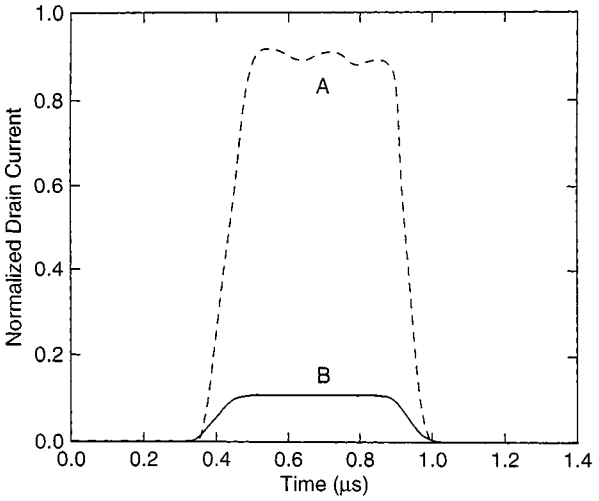

Fig. 8. Gate lag measurements. The drain current is normalized to I_{DSS}. V_{GS} is pulsed from the threshold voltage to 0 V. Curve A: device passivated with SiN. Curve B: same device before passivation.

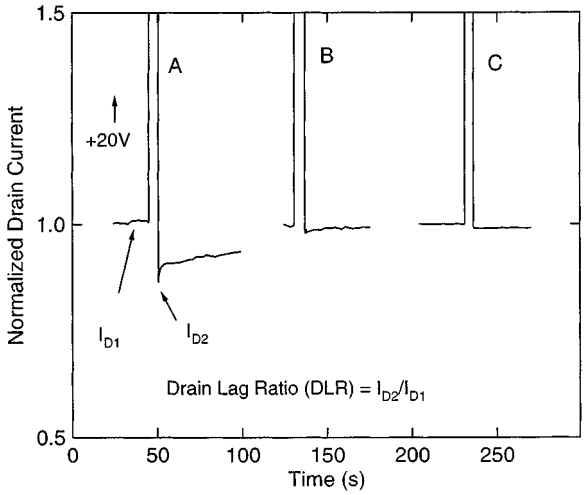

Fig. 9. Drain lag measurements. The drain current is normalized to the low-field value. A: typical response. B: device on a conductive buffer layer. C: device on an optimized GaN buffer layer.

Devices A and B were fabricated on the same wafer, which, however, had a varying conductivity with location. On the more conductive parts of the wafer (with resistivity estimated to be $<10^2$ Ω-cm), where the drain current could not be pinched off beyond 15% of $I_{\max}$, the DLR was 1, as in device B. The degree of drain lag is apparently related to the conductivity of the buffer layer. The deep levels responsible for producing the high resistivity material are also likely to be responsible for this trapping effect. The observed response on conductive buffers is consistent with fewer traps in the buffer regions, or with the filling of these traps by shallow donors. It is possible to grow resistive (10^5 Ω-cm) buffer layers that result in devices with no drain lag as demonstrated by device C in Fig. 9, which is the drain lag characteristic for the device of Fig. 2. The transient response of device C has also been examined on a shorter time scale. The drain current response can be characterized by a single exponential time constant of 6 μs, which is consistent with the thermal response time.

The data presented here provides strong evidence that the current collapse phenomenon is directly tied to the buffer layer. However, this set of experiments cannot conclusively rule out the possibility that trapping in the AlGaN layer is a contributing factor. However, the presence of similar trapping effects in GaN MESFETs grown on similar buffer layers [7] supports the view that the buffer layer is the source of the traps that are primarily responsible for current collapse in GaN HEMTs.

VI. Microwave Power Performance

Both the CW and pulsed microwave power performance of the GaN HEMT's described above have been measured. The pulsed measurements were used to distinguish between the trapping and thermal effects because they eliminate most of the device self-heating. In addition, higher V_{DS} can be applied under pulse bias because it avoids the permanent degradation that has been observed under high voltage ($V_{DS} > 25$ V) dc operation. Devices with a gate width of 150 μm were measured at 3.8 GHz using microwave probes. Impedance matching was accomplished with manually-adjusted tuners. For the pulsed power measurements, both the drain voltage and the input signal were pulsed using a 5 μs pulse and a 1% duty cycle.

The maximum CW power output that has been obtained from these devices is 3.3 W/mm with a 45% power-added efficiency and a 10 dB gain. This result is for the SiN passivated devices with a 0.4 μm gate length and a 200 Å thick AlGaN layer, described earlier. Pulsed microwave measurements at the same V_{DS} setting of 20 V used for the CW measurement resulted in an increase in power density to 4.3 W/mm. This increase in performance is attributed to a higher drain current level associated with a lower operating temperature in the device active region. The results of a pulsed power measurement for a V_{DS} of 35 V are shown in Fig. 10. A power output of 1 W (6.7 W/mm) with 48% PAE and 13 dB gain were measured. At the 1 and 2 dB gain compression points, the power output is 3.2 and 4.6 W/mm, respectively. These CW and pulsed results are among the highest achieved for GaN HEMTs on sapphire substrates and are significantly higher than what can be achieved with other III–V technologies.

The dependence of pulsed power output on drain voltage is shown in Fig. 11. In this figure, the measured power output as a function of drain voltage is plotted for several devices fabricated from three different wafers. Wafer 2 and 3 correspond to the 250 Å and 200 Å AlGaN layer thicknesses, respectively, discussed previously. Wafer 1 is representative of earlier-generation HEMT material. Devices from this wafer display a higher amount of current collapse than the devices from wafers 2 and 3. The power output results fall into two categories. The first category consists of devices that are strongly limited by surface trapping, as represented by wafer 1. In this case, the addition of the passivation layer dramatically improves the gate lag response and increases the power substantially ($>2\times$). These devices, however, may still be limited by buffer layer trapping. The resulting saturation of power output with drain voltage is consistent with trapping, mostly likely in the buffer layer since this effect would be more pronounced at higher drain bias. The

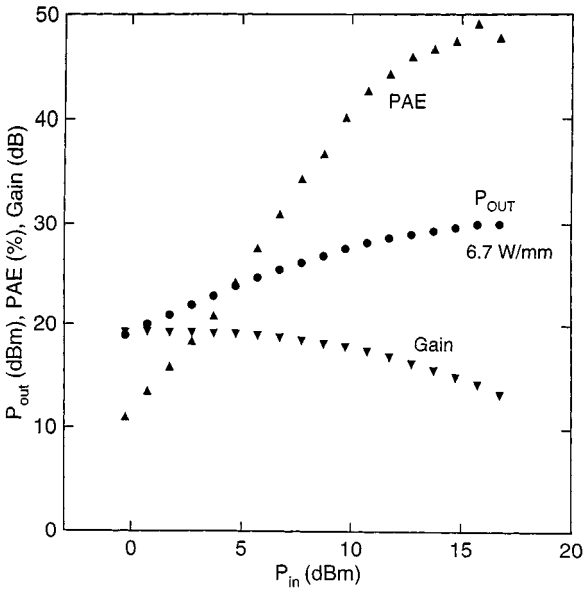

Fig. 10. Pulsed power performance at 3.8 GHz for a 5 μs pulse width and 1% duty cycle.

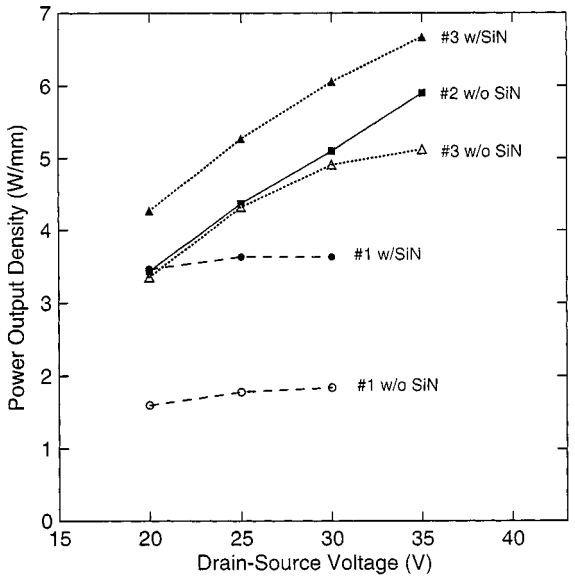

Fig. 11. Pulsed power output dependence on drain-source voltage. The results are obtained on devices from three different wafers.

effectiveness of SiN passivation in improving power output depends on how severely the device was being limited by surface trapping. The second category applies to devices that are not limited by surface trapping, represented by wafer 2 and 3. In this category, the power output is not saturated and increases with V_{DS} as expected. These devices have excellent gate lag response without passivation and the improvement seen in power output as a result of passivation is only about 25%. This degree of improvement is of the same approximate increase seen in I_D after passivation. These results make it clear that both surface and buffer trapping effects need to be minimized in order to obtain high power devices.

VII. Summary

AlGaN/GaN HEMTs grown on sapphire substrates have demonstrated a maximum drain current greater than 1 A/mm and a gate-drain breakdown voltage over 80 V. Devices with a 0.4 μm gate length have exhibited an f_T of 30 GHz and an $f_{\max}$ of 70 GHz. At 3.8 GHz, a CW power output of 3.3 W/mm with 45% power-added efficiency and 10 dB gain and a pulsed power output of 6.7 W/mm with a 48% PAE and 13 dB gain were attained. The results presented here detail the effect of buffer and surface trapping on device performance. The observed current collapse in GaN HEMTs is attributed to buffer layer trapping. This is consistent with the observations that 1) the amount of current collapse is related to the resistivity of the buffer layer, 2) the current collapse is not affected by a SiN passivation layer, and 3) the previous observation that current collapse is also observed in GaN MESFETs. Silicon nitride passivation has been shown to be effective in improving the gate lag response of GaN HEMTs. The resulting degree of power output improvement is related to how significantly the device was compromised by surface trapping prior to nitride passivation. The reduction of these surface and buffer layer trapping effects have resulted in improved microwave power performance.

Acknowledgment

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