# Trends in Nanotechnology: Self-Assembly and Defect Tolerance

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## ABSTRACT

In this paper we discuss the concept of using self-assembly coupled with novel switching elements and a defect-tolerant architecture to fabricate advanced nanoelectronics. Self-assembly should allow small features to be fabricated at a markedly lower cost than that projected by extrapolating current trends because of the defect tolerance and the use of coarser lithography to position device features, rather than fine lithography to form the critical device dimensions.

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## INTRODUCTION

As the feature size on an integrated circuit decreases according to Moore's Law of doubling functionality on a chip every two years [1], fabricating the chips becomes increasingly difficult. Although recent demonstrations of MOS transistors with 30–50 nm gate lengths [2] have shown that fabrication technology can be extended to these small sizes, which will be needed in less than ten years [1], the cost and complexity of the fabrication process increases greatly.

In addition to cost and complexity, another fundamental limit must be addressed when scaling to such small dimensions. The number of electrons in the active region of the device decreases as the physical channel size decreases. As the number of electrons decreases, the statistical fluctuation in their number can become an appreciable fraction of the total number of electrons. This variation has already limited analog circuit design for several years, and will become visible in digital circuits within a few years. More fundamentally, however, the number of electrons in a device will approach one in about fifteen years if present scaling trends continue. At this point fundamentally different devices will be needed.

## POTENTIAL DEVICE STRUCTURES

A number of potential devices have been proposed: (1) Single-electron transistors (SET's) [Fig. 1(a)], in which the addition of one electron changes the conducting properties of a channel (even though many electrons may be physically present in the critical element of the device). Single-electron devices may be limited by a background charge of a fraction of an electron, making controlled operation difficult. (2) Quantum cellular automata (QCA) [Fig. 1(b)], in which a pair of electrons in a cell occupies one of two low-energy positions. Coulomb interactions between

neighboring cells allow transfer of information from one cell to an adjacent cell. One attractive feature of QCA is that separate interconnections are not needed within the array of cells. (3) Quantum computing elements, which may allow totally different types of information processing with an exponential increase in information-processing capability for selected classes of problems. The principles of quantum computation are just now being demonstrated at a rudimentary level, and practical realization of solid-state quantum computers is many years away. (4) Molecular electronics [Fig. 1(c)], in which molecules in a single monolayer have two or more states. The state of the molecules can be changed electrically, with an associated change in the electrical properties of the molecules. Eventually the device size should be scalable to a single molecule or a few molecules. The principles of molecular electronics have been demonstrated, and some of the many possible molecules are being explored. One class of molecules contains elements that can be physically rearranged by electric fields. Each arrangement has different electrical properties, allowing information to be stored or processed. For example, cooperative work between Hewlett-Packard (HP) and the University of California at Los Angeles (UCLA) has shown that the state of a catenane molecule with two interlocking rings [Fig. 1(c)] can be changed by using an electric field to rotate one of the rings [3]. One state is nonconducting, while the other is conducting, with a diode-like characteristic.

## SELF-ASSEMBLED NANOSTRUCTURES

Although more than one of these possible new devices may prove to be controllable enough to be used in a new class of electronics, we still must consider “Moore's second law,” which deals with the ever-increasing cost of an integrated-circuit fabrication facility. Manufacturing facilities currently cost several billion ($10^9$) U.S. dollars, and their cost is projected to continue doubling with almost every generation of smaller devices. The main costs of the facility are the expensive lithography needed to form ever-smaller features and the requirement for ever-cleaner environments to prevent defects. Even one defect in a critical part of the circuit can destroy an entire chip.

To reduce the need for fine lithography, “self-assembly” techniques are being explored. The basic idea of self-assembly in this context is to use natural forces to form a device feature, although its position may be determined by coarser lithography. Thus, the less-expensive equipment associated with a previous technology generation may be used, along with self-assembly techniques, to fabricate circuits for the next generation of devices. One technique of forming such nanostructures relies on the stress resulting from the lattice mismatch of a substrate and a deposited layer. As the layer is deposited, the atoms in the layer register with the lattice of the underlying material, even though the intrinsic lattice constant of the depositing material is different. The resulting stress tends to deform the depositing material, eventually forming three-dimensional structures. If the lattice mismatch is the same in two orthogonal directions, zero-dimensional nano-islands form (commonly called “quantum dots” although they are often larger than suitable for quantum confinement of electrons). An example of a nanoisland formed by the deposition of Ge on Si with its 4% lattice mismatch is shown in Fig. 2 [4].

Alternatively, self-assembly can be used to form structures for molecular electronics. A single molecular monolayer (or a controlled number of monolayers) can be routinely formed on a substrate by techniques such as Langmuir-Blodgett deposition.

Once the devices are fabricated by self-assembly, the interconnections should also be formed by self-assembly. “Nanowires” can be formed by the stress from lattice mismatch discussed above. If the lattice mismatch is small in one direction and large in the other direction, an anisotropic

structure can result, as illustrated in Fig. 3, which shows a structure formed by depositing erbium on Si(001) and annealing to form an $ErSi_2$ nanowire [5]. The nanowire can be used directly to carry electrical signals, or it can be used as an etch mask to define an underlying layer, such as a conductor on an insulating substrate.

An alternative technique can be used to form a nanowire that is not constrained along its length by the substrate. A metal-containing nanoisland is first formed on the substrate. The metal in the island then catalyzes the decomposition of a gas. For example, the Ti in a $TiSi_2$ island promotes the decomposition of a Si-containing gas, such as silane ($SiH_4$) or dichlorosilane ($SiH_2Cl_2$), in a chemical vapor deposition (CVD) reactor [6]. The resulting Si atoms can then diffuse through or around the $TiSi_2$ particle and precipitate on the underlying Si substrate, pushing the $TiSi_2$ nanoisland upward. As more Si atoms arrive, they continue precipitating on the underlying Si, forming a nanowire, and the $TiSi_2$ nanoparticle moves along with the growing tip of the nanowire [Fig. 4(a)]. The nanowire is single-crystalline, as shown by the high-resolution transmission electron micrograph in Fig. 4(b) [6]. The nucleating nanoislands can be formed by the stress from lattice mismatch, as discussed above for Ge on Si. The large lattice mismatch between $TiSi_2$ and Si causes the islands to be small (of the order of 10's of nm), and the resulting wires have approximately the same diameter.

Thus, forming nanoislands or long nanowires by self-assembly is possible. However, to interface with the surrounding circuitry (conventional CMOS or an alternative), the position of the nucleating nanoislands must be predetermined. Irregularities purposely formed on the surface of the underlying substrate can serve to position the nanoislands. As an example, Fig. 5 shows Ge islands formed on a patterned Si(001) substrate by the stress from the lattice mismatch of the two materials [7]. Before growing the Ge islands, a raised region of Si was formed on the underlying substrate. The subsequently formed Ge islands positioned themselves at the edges of the raised Si stripe, probably because the additional atomic steps in the substrate at irregularities provide lower-energy positions, which immobilize depositing atoms. The resulting atom accumulations at these positions serve as precursors for island formation. Thus, the islands nucleating the nanowires can be positioned at specific locations determined by coarser lithography, without having to control the critical nanowire or nanoisland dimensions with lithography. The wires can be positioned to connect to CMOS in an underlying substrate (especially to interface with input/output circuitry). Gain can be provided in the underlying circuitry or possibly by building field-effect transistors directly in the Si nanowires.

## DEFECT TOLERANCE

Although fine nanowires and nanoislands can be formed by self-assembly, a significant number of the structures formed by any thermodynamically controlled fabrication process will be defective. The effect of defects can be minimized by basing much of the circuit on a simple and dense cross-bar array architecture, which can be made tolerant of defects [8,9]. The cross-bar array essentially contains two orthogonal sets of wires separated by a layer that forms the devices. Wherever two wires intersect, a device is automatically formed. A nonlinear element (*e.g.,* a diode) contained within the device allows efficient programming of individual devices. However, the device must have a well-defined threshold to allow switching of only the desired element, without affecting other devices in the same row or column of the array. Because the cross-bar array is very regular, its repetitive structure allows it to be configured to avoid random defects. The defects are located by initially testing the array, and then the array is programmed to avoid the defects and to accomplish the desired electronic task. Thus, an architecture based on cross-bar arrays can be tolerant of defects by its simple structure and configurability. The defect-tolerant architecture can

be used even with conventional devices to reduce the need for cleaner environments as device features become smaller, and the principle has been demonstrated using conventional field-programmable gate arrays [8].

## SUMMARY

In this paper we have discussed the possible use of self-assembly coupled with novel switching elements and a defect-tolerant architecture to fabricate advanced nanoelectronics. The cost of such fabrication should be markedly less than that expected from current trends of device fabrication because of the defect tolerance and the use of coarser lithography to position device features, rather than fine lithography to form the critical dimensions of the devices.

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**FIGURES**

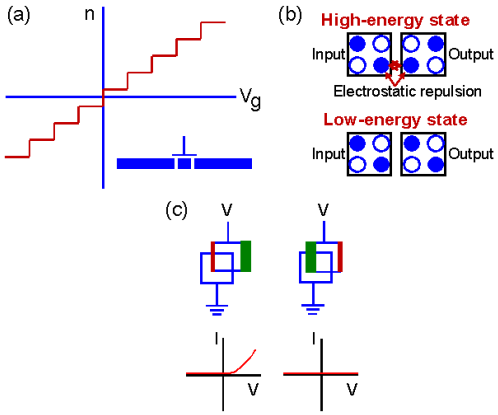


Fig. 1: (a) Change in the number of electrons in a single-electron transistor as the applied voltage changes. (b) In a quantum cellular automata Coulomb forces from electrons in one cell determine the position of electrons in an adjacent cell, allowing information propagation. (c) An electric field can rotate part of a molecule, changing its electrical properties.

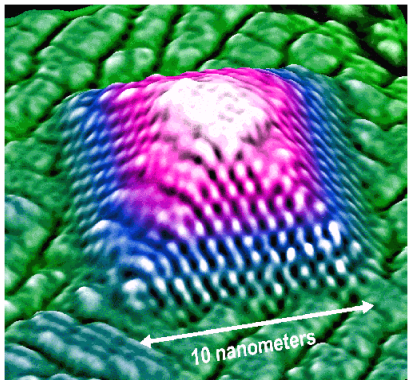


Fig. 2: Atomic-resolution, scanning-tunneling micrograph of a small pyramidal, self-assembled Ge island bounded by {105} facets on a Si(001) substrate.

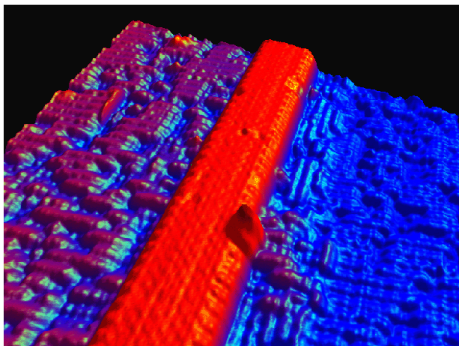

Fig. 3: Atomic-resolution, scanning-tunneling micrograph of self-assembled $ErSi_2$ nanowire on Si(001).

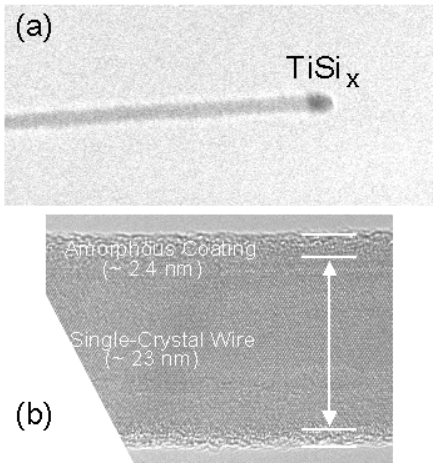


Fig. 4: (a) Transmission-electron micrograph of Si nanowire with a nucleating Ti silicide particle on the free end of the wire. (b) High-resolution, transmission-electron micrograph of Ti-nucleated Si nanowire.

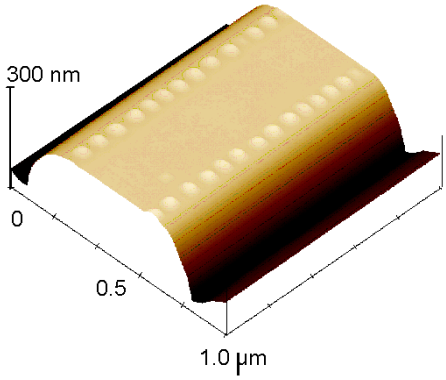


Fig. 5: Atomic-force micrograph of self-assembled Ge islands self-positioned at the edges of a Si pattern.