Trends in silicon technology and device research

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TRENDS IN SILICON TECHNOLOGY AND DEVICE RESEARCH

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During the past years silicon has been deeply investigated and many results have been published.

Presently a lot of other semiconductors like GaAs, InP... seem to find a wide interest among researchers [1]. Does that means that silicon and silicon technology are perfectly known ?

The advent of micron size devices, in fact, rises a lot of new problems that remain unsolved. These problems in the field of MOS technology mainly, are related to :

— the material itself and its associated defects ;
— the technology with the need of more controlable steps : doping, oxidation, etching, masking ;
— the devices themselves : physical understanding of their behavior, quality and reliability.

Material. — Scaling down devices needs thinner epitaxial layers either on bulk silicon or on sapphire : quality and controlability of the characteristics must be reached on epitaxial layers of typically, 5 µm.

— Gettering of metallic impurities becomes more and more necessary and a better understanding of the physical processes involved is required.
— Electrical defects responsible for a decrease in yield and reliability are to be studied in relation with a decrease in component size.
— Doping homogeneity is a sensitive parameter for threshold voltage uniformity on a given wafer.

Defects. — The observed defects (stacking faults, twins...) are either existing in the material or process induced. Their density is mainly related to the nature of the treatment and the temperature.

— Their electrical behavior is not always clear and besides revealing them it is necessary to make a correlation between their physical presence and their electrical properties as related to device parameters (mobility, leakage currents...).
— Gettering of these defects in non active parts of the substrate is presently the best way to avoid degradation of the device characteristics. The gettering process involves a lot of complex mechanisms.
— Yield and reliability will be improved if a better understanding of defects physics is reached.
— Component size in the micron range could be similar to defect size indicating a possible increase in spread between components or a higher noise level.

Doping. — Basic mechanisms for exchanges of impurities between two mediums (gas-silicon, SiO_2-silicon...) are not well understood and the microscopic diffusion mechanisms are often still unknown, models are limited in accuracy and range of applications (doping level, temperature range...).

— Ion implantation is widely used as an elementary step of a *cold process*. Defects annealing associated with ion implantation for certain classes of devices is not well understood and residual defects contribute to increasing device noise.
— Two dimensional effects define the main electrical characteristics of devices and must be taken into account for the realisation of shallow and small area junctions. Their prediction needs two dimensional solutions of Fick's equations with adequate boundary conditions.
— Small epitaxial layers either on bulk silicon or on insulating substrate are generally used for making small devices and it is necessary to take these boundary conditions into account for doping profiles prediction. The existence of such boundaries is generally associated with defects interacting with diffusing impurities and adding a new level of complexity to the problem to be solved.

Oxidation. — In the MOS technology the improvement of device performance relies on the availability of thin SiO_2 layers (30 nm to 50 nm) with good yields and stability under temperature-bias stresses. This requires a physical understanding of thin layer growth and defect formation with respect to cleaning procedures, this being applied to conventional oxidation processes or new processes like HIPOX (high pressure oxidation), C.V.D. (C.V.D. deposition with subsequent thermal annealing) or LOPOX (low pressure oxidation).

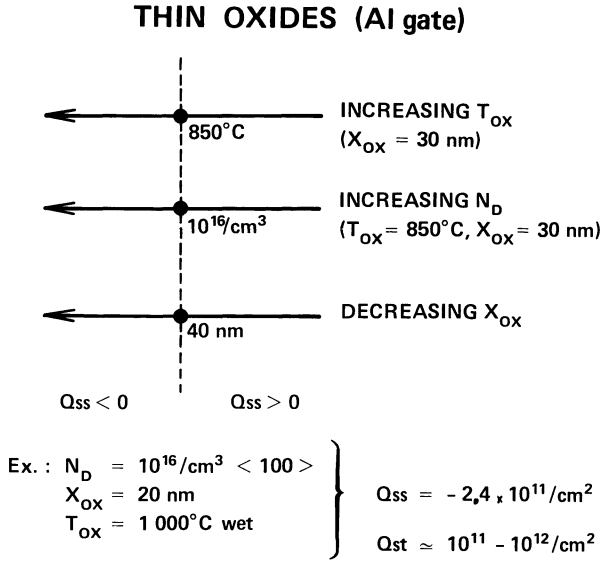

FIG. 1. — Negative Q_{SS} effect ion thin SiO_2 layers.

The interface modelling of SiO_2 growth is still poor and transition layers between silicon and SiO_2 are not well known. It appears that in specific cases negative Q_{SS} values can be seen on p type MOSFET devices whereas on neighbouring n type MOSFET devices there is still a positive Q_{SS}. This is qualitatively illustrated on figure 1 [2].

As seen later anomalous metallic diffusion at low temperature occurs in SiO_2 and in other dielectrics.

Etching. — Small geometries are more easily achieved using dry etching, either plasma etching or ion etching.

Though more controlable, these techniques are not well known as far as the interaction of the activated species and surface are concerned (selectivity of etching different kinds of materials), in plasma etching for instance :

— Identification and characteristics of active and producted species.
— Electrical phenomena.
— Radiation.
— Chemical parameters.
— Determination of mask materials.

In both these techniques the interaction between the plasma or the ions and the device must be studied so as to minimize degradations.

Masking. — This is the first domain where an effort has been done to decrease device size. There are several new techniques that will not be discussed because this has been done extensively in recent conferences.

Besides the more obvious solutions as using deep U.V. or electron beam, there are extensive studies on X rays and ions beams, such techniques will be necessary for submicron devices processing.

Devices. — Submicron devices involve physical effects that are not included in present analysis of their behavior (diffusion currents, punch through currents... etc.) and these must be considered for proper scaling down of these devices. It is also believed that submicron geometries will allow different devices to be built using different combinations of oxides and diffused regions.

As far as present results are concerned two major characteristics are to be improved :

QUALITY. — Smaller dimensions need the same relative accuracy as we have presently, say 10 % control on most of the *active* geometries (gate length and width...). This requires an absolute value of the spread in dimensions within $\pm$ 0.1 µm to $\pm$ 0.2 µm on the processed device, so much less spread at each technological step. Other parameters, like threshold voltages for example, are also important to control with higher accuracy, mainly because supply voltage values tend to decrease (< 5 V).

Due to a higher density of defects around the junctions, small MOSFET devices will have much more interface states as shown on figure 2 [3]. Values of N_{ST} around $10^{12}/cm^2$ can be reached.

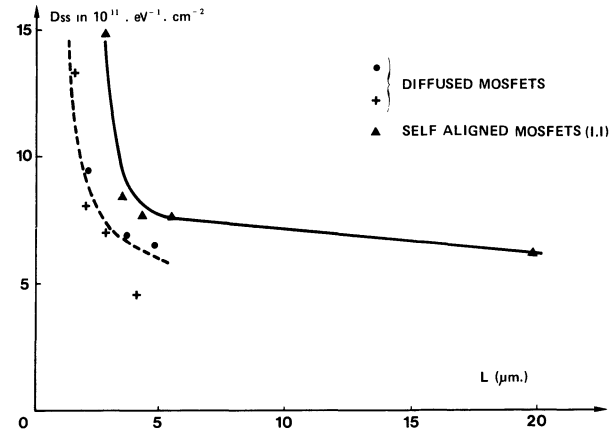

FIG. 2. — Surface state density *versus* channel length.

A similar problem in controlling Q_{SS} values is found due to the specific relation of Q_{SS} with oxidation temperature, substrate doping nature and thickness of the layers as seen previously. This is particularly important in CMOS technology where threshold values must be matched.

Reliability. — Thin SiO_2 layers are more sensitive to surface defects and their passivation (PSG passivation for example) is more difficult to achieve. More generally interactions between gate materials (metal or polysilicon) and dielectric layers can produce interface instabilities. Charge injection can also be a reason for parameters drift as can be seen on figure 3 [4] higher electrical fields within the device cause hot carrier

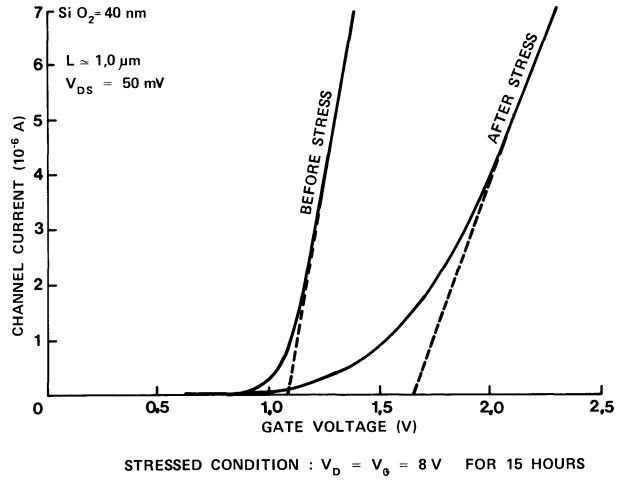

FIG. 3. — Stress effects on short channel MOSFETS.

injection through SiO_2 layers and degradation of parameters drift as can be seen on figure 3 t]. Higher seen.

Metallic diffusion in aluminium gate MOSFETS also causes a degradation of the interface and the volume near the surface and could be a cause of lower reliability. Figure 4 we have shown all profiles within SiO_2 and silicon in an MOS structure for different annealing temperatures of the structure [4]. Care must be taken, in the process, to minimize such an effect because surface recombination velocity and bulk lifetime are affected by increasing all concentrations at the silicon surface. In silicon gate technology low shett resistivity requires high doping levels but keeping dielectric integrity of the MOS structure.

Solutions are also to be found for the interconnection layers to insure high reliability (new metals, silicides...) of conductors and contacts.

In summary a better physical understanding of all these processes is certainly the way for improving quality and reliability of the scaled down devices, the most critical point being the technology of the active SiO_2 layer for the gate of the MOSFET.

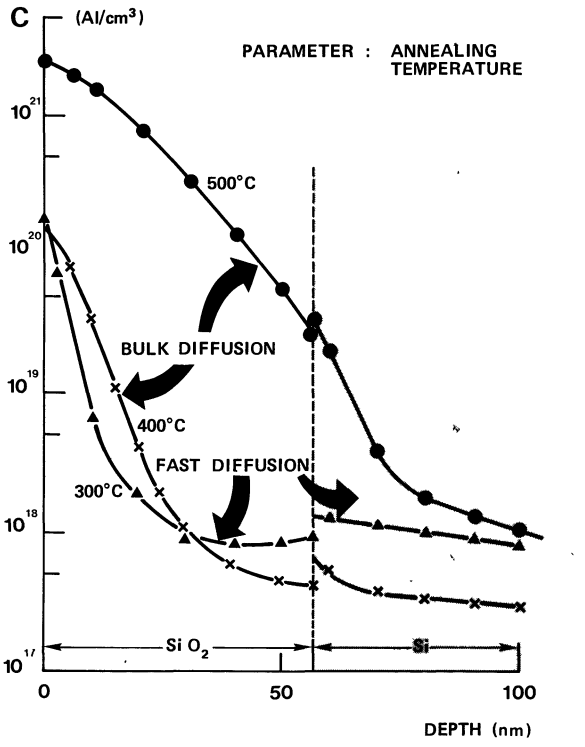

FIG. 4. — All profiles in SiO_2 after different annealing temperatures ($Al/SiO_2/Si$ structure).

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