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Triangular Power Supply Based Adiabatic Logic Family

Shipra Upadhyay, R.A. Mishra, R.K. Nagaria, S.P. Singh and Amit Shukla
Department of Electronics and Communication Engineering,
Motilal Nehru National Institute of Technology, Allahabad-211004, India

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Abstract: This paper presents the design and performance evaluation of a modified complementary energy path adiabatic logic (MCEPAL) circuit. A simulative investigation on the proposed MCEPAL based, multiplexer, JK flip flop and 3 bit counter has been done using VIRTUOSO SPECTRE simulator of cadence in 0.18µm UMC technology and its performance has been compared with the previous adiabatic (i.e. CEPAL) multiplexer, JK flip flop and 3 bit counter circuits. The MCEPAL based, multiplexer, JK flip flop and 3 bit counter circuit exhibits the power saving of 77%, 25% and 48% respectively to its corresponding CEPAL circuits at 100 MHz frequency and 1.8V operating voltage.

Key words: Adiabatic · CEPAL · Multiplexer · Power clock

INTRODUCTION

Power has become an important design parameter in today's ultra low submicron digital designs. Adiabatic logic style has emerged as a promising approach to achieve ultra-low power without sacrificing noise immunity and driving ability. Energy recovery techniques and adiabatic logic topology minimizes energy dissipation by maintaining low voltage drop across conducting devices at all times. The un-dissipated energies related to the charges stored in the circuit capacitors are recycled. Thus the energy is not dissipated as heat. This method can usually be applied in addition to other approaches like power supply voltage reduction and algorithmic techniques for reduced logic transitions. In conventional CMOS logic we use constant voltage source to charge the load capacitance [1-4] whereas all adiabatic logic families are based on the time varying ramp voltage supply. The following mathematical analysis, based on time period (T), stored charge (CLV), load capacitance CL and channel resistance R is sufficient to understand adiabatic logic principle.

$$P_{diss}=2(\frac{RC_L}{T})C_L V_{DD}{}^2 \int V_t{}^2 C_L$$

Hence as given by above equation, keeping the clock transient time T much larger than intrinsic time constant RCL of a device; we can reduce power dissipation in a switching transition. The extra power dissipation due to the threshold voltage drop (Vt) is classified as a non adiabatic loss [5]. Various adiabatic circuit topologies have been proposed over the past decade. Most of these circuits have relied on multiple-phase power-clocks to steer currents and recycle charges [6-10]. They are not attractive for high speed design, due to their relative complex control requirements. In contrast to multiphase circuits, single phase adiabatic circuits [7, 10, 11] have simple clocking requirements, thus they enjoy minimal control overheads and are capable of operating at high speeds, while achieving high-energy efficiency. Complementary energy path adiabatic logic (CEPAL) inherits all the advantages of single phase adiabatic circuit with additional improvement in robustness and throughput.

In this paper we propose the design of a modified CEPAL (MCEPAL) circuit. In addition to power/energy measurements, our paper includes a simulation based comparison of the proposed MCEPAL based multiplexer, JK flip flop and 3 bit counter circuit with its CEPAL and static CMOS counterpart. A CEPAL and conventional CMOS based multiplexer, JK flip flop and 3 bit counter circuit with the same features i.e. no. of transistors, supply voltage and frequency were also simulated and their performances were measured.

Corresponding Author: Shipra Upadhyay, R.A. Mishra, Department of Electronics and Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad-211004, India.

MCEPAL based, multiplexer, JK flip flop and 3 bit counter circuit were found to be more power efficient than the corresponding CEPAL and CMOS circuits.

This paper has been segmented into six sections. Section I deals introduction part while in section II and section III, we describe the previous work related to CEPAL circuit and proposed MCEPAL circuit respectively. The proposed MCEPAL based multiplexer, JK flip flop and 3 bit counter circuits are described in section IV. Section V and section VI presents results and discussion and conclusion respectively.

Previous Work: The structure and operation of CEPAL circuit are described in [12]. CEPAL is composed of two charging pMOS diodes (P1 and P2), a pull-up (P) network, two discharging nMOS diodes (N1 and N2) and a pull down (N) network. Two sinusoidal supply clocks in complementary phases (i.e. PC and $\overline{PC}$) are used. Assume that initially output (Vout) is LOW and the P-network is on while the N-network is off then the output either follows PC or its complement as it swings HIGH. Once Vout becomes HIGH the followed power clock then swings down and output node of CEPAL becomes floating but this situation is soon removed because at the same time the complement of the followed power clock swings up, thereby eliminating the weak HIGH at the output node.

Similarly the weak LOW at the output can be eliminated by the complementary energy paths. CEPAL have two more diodes in comparison to quasi static energy recovery logic (QSERL)[13], but power dissipation due to these additional diodes is not very large as there is only one charging or discharging transistor turned on at an instant of time. Thus QSERL and CEPAL circuits have similar power consumption however considerable improvements in area and power overheads can be achieved in CEPAL circuits because the keeper used in QSERL circuits to avoid erroneous operation during hold phase is removed.

Proposed Mcepal Logic

Power Supply: In the previous published papers on adiabatic circuits, different shapes of power clocks have been used [14-16] (like trapezoidal, sinusoidal and triangular etc). It has been observed that the energy dissipation for a trapezium waveform is more than that in the case of a triangular waveform. It may be due to the fact that the capacitor is allowed to charge to a higher value of voltage corresponding to logic '1' since the duration of the peak value of supply voltage is longer compared with that of the triangular waveform.

In the case of a sine wave, the energy dissipation is more than that in the above two cases [17] and this may be attributed due to the fast voltage rise near the zero crossing. Thus, we can say that the triangular supply waveform is suitable for less energy dissipation.

Design of MCEPAL Circuit: As we have discussed above that the energy dissipation for a triangular power supply is lesser than the other power supplies (i.e. sinusoidal and trapezoidal) thus we can use triangular power supply instead of sinusoidal in adiabatic circuits. With this modification we can further reduce the energy dissipation significantly. The structure of a MCEPAL circuit is shown in Fig. 1. The basic structure of MCEPAL circuit is similar to the CEPAL circuit except the supply clocks. In our proposed MCEPAL circuit two complementary triangular supply clocks (PC and $\overline{PC}$) are used. If output (Vout) is LOW and p network becomes on then Vout will follow PC or $\overline{PC}$ (it will be charged up to the peak value of triangular power clock) and becomes HIGH. When the followed power swings down at the same time its complementary power clock swings up and it will eliminate the floating weak HIGH output. Similar action will happen when n network is on to eliminate weak LOW at the output.

MCEPAL Versus CEPAL: A basic CEPAL inverter and MCEPAL have been simulated and their power dissipation and delay have been measured in 0.18µm UMC process with all the transistors of equal sizes of W/L= 0.24µm/0.18µm and supply voltage, power clock frequency (f_{PC}), input frequency (f_{in}) and load capacitance are 1.8V, 500MHz, 50MHz and 5fF respectively.

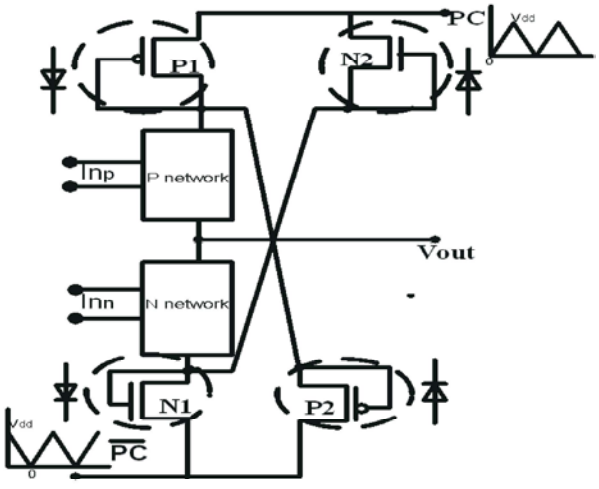

Fig. 1: Proposed MCEPAL topology

Table 1: Comparison of MCEPAL and CEPAL inverters

Circuit	Power dissipation (nW)	Delay (ns)	Output swing
CEPAL	418	0.27	0.327 to 1.39
MCEPAL	87.4	0.74	0.302 to 1.36

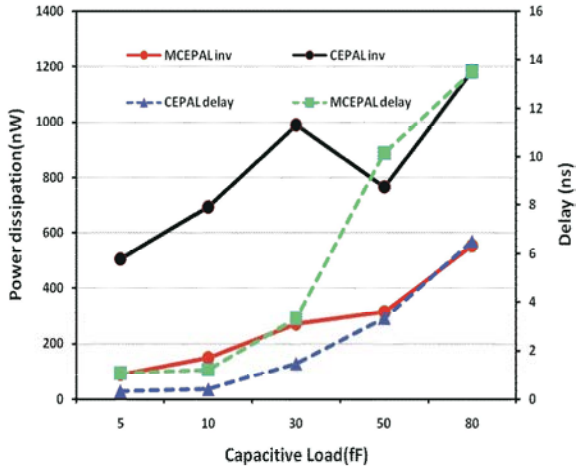

Fig. 2: Power dissipation and delay as a function of load capacitance (at f_{PC} =500MHz, V_{DD}=1.8V and f_{in}=50MHz).

It is observed that in MCEPAL inverter, power efficiency is 78% improved with slight increase in delay in comparison to the CEPAL inverter circuit.

Driving Ability: To check the driving ability of the MCEPAL circuit, a load analysis at f_{PC} =500MHz, V_{DD}=1.8V and f_{in}=50MHz has been done. Fig. 2. shows the variation of power dissipation and delay versus capacitive load for CEPAL and MCEPAL inverters. It may be observed from the figure that as load capacitance increases there is a large increase in power dissipation and delay for both the inverters (CEPAL and MCEPAL). Whereas MCEPAL inverter has lesser power dissipation at all load capacitances than CEPAL inverter. MCEPAL inverter has a little bit larger delay than CEPAL inverter but this can be traded off with low power.

It is also observed that at very high load capacitances, output swing of both the inverters (CEPAL and MCEPAL) becomes very small which results in incorrect output that does not satisfy the inverter characteristics. Thus at very high load capacitances irregular trend of power dissipation (decrease in power dissipation from 30fF to 50fF and then increasing power dissipation) is obtained.

Effect of Variation of Frequency: This simulation is carried out by varying the input frequency and supply frequency simultaneously (keeping the supply frequency

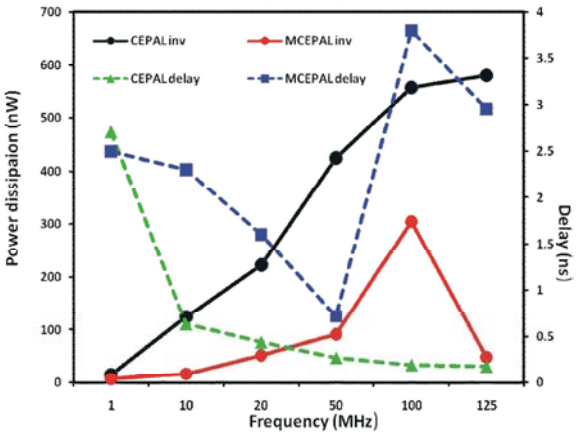

Fig. 3: Power dissipation and delay as a function of operating frequency(at f_{PC}/f_{in}=10, V_{DD}=1.8V and C_L=5fF).

ten times the input frequency) from 1MHz to 125 MHz and power dissipation and delay has been measured. From Fig.3. It is observed that as frequency increases power dissipation in both the inverters (CEPAL and MCEPAL) increases while their delay decreases.

With increasing frequency output swing of both the inverters decreases and after 100MHz output swing of MCEPAL inverter becomes very small which results in improper output. Thus at very high frequencies trend of power dissipation and delay is unpredictable in MCEPAL inverters.

But because MCEPAL inverter works with the significant reduction in power dissipation for a sufficient range of frequencies so it may be a good choice over CEPAL circuits.

Adiabatic Circuits Using Mcepal: Previously reported adiabatic logic styles focused mainly on combinational logic designs such as CLA, ALU and multipliers [18]. However, flip-flops, multiplexers and sequential circuits cannot be neglected in digital systems, as we cannot build adiabatic sequential circuits by simply using conventional method. In this section we focus on the design and analysis of a MCEPAL based multiplexer, JK flip flop and 3 bit counter circuit.

MCEPAL based Multiplexer: The proposed 2:1 multiplexer may be designed using three MCEPAL NAND gates and an MCEPAL inverter as shown in Fig. 4(a). First of all we have to design a 2 input MCEPAL NAND gate and an MCEPAL inverter and then we can use them to design a multiplexer.

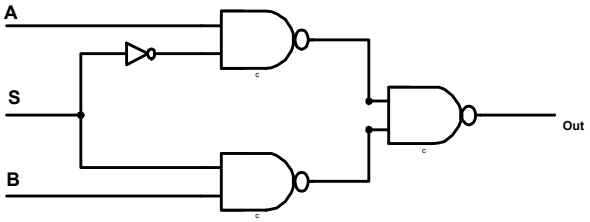

Fig. 4(a): 2:1 MUX logic diagram

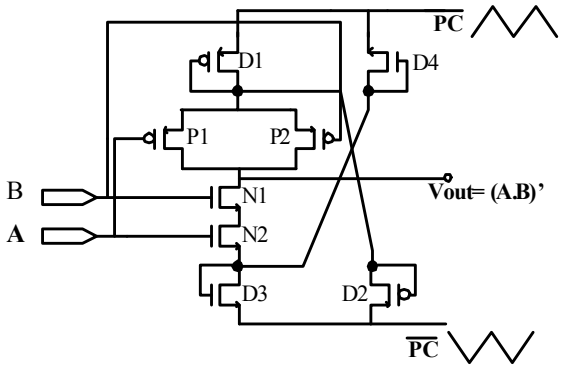

Fig. 4(b): Schematic diagram of MCEPAL NAND gate

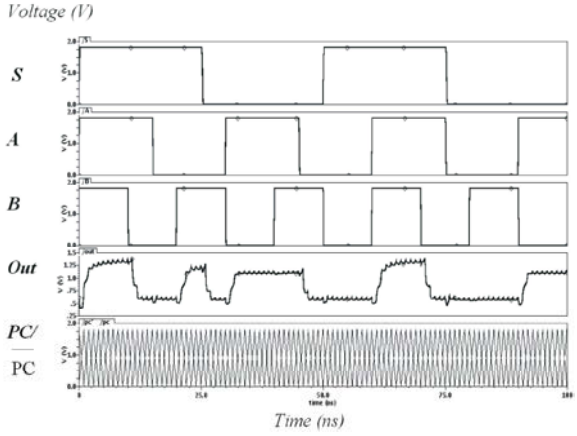

Fig. 5: Simulated MCEPAL MUX timing waveforms

Schematic of a MCEPAL based NAND gate is shown in Fig. 4(b). It consists of two p-channel MOSFETs (P1 and P2 connected in parallel) and two pMOS diodes D1 and D2 in the charging path. Similarly in the discharging path we have two n-channel MOSFETs (N1 and N2 connected in series) and two nMOS diodes D3 and D4. Supply voltages are two complementary triangular power clocks (PC and $\overline{PC}$.

Simulated timing waveforms are shown in Fig. 6. Supply clocks are triangular waveforms (PC and $\overline{PC}$). The inputs of a 2:1 MUX are A and B with select input S and output as Out.

The combination of inputs '11, 10, 00, 01' are given in the form of a strings A= '1100', B= '1001' and select input S= '1110'. The output is obtained as strings, out= '10010'.

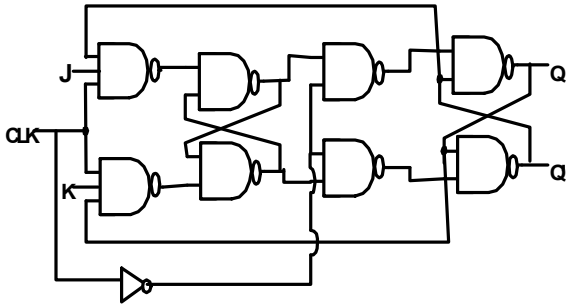

Fig. 6(a): MCEPAL based master slave JK flip-flop circuit diagram

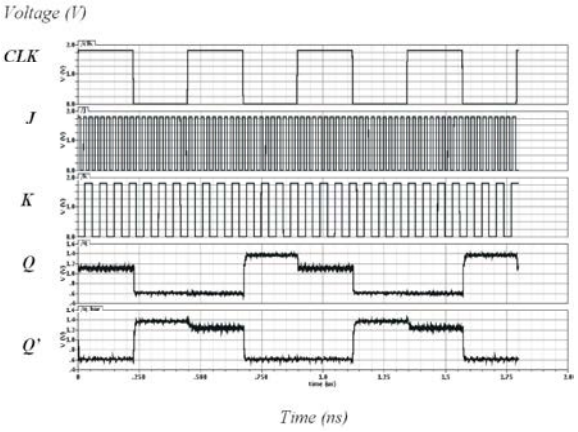

Fig. 6(b): Simulated MCEPAL JK flip flop timing waveforms

MCEPAL Based JK Flip Flop: The latches are generally designed by connecting two inverters or two NAND/NOR gates in a cross coupled manner. The proposed MCEPAL master slave JK flip flop was designed using MCEPAL NAND gates and MCEPAL inverter as shown in Fig. 6(a). The structure of MCEPAL NAND gate is shown in Fig. 4(b). The inputs are J and K along with the clock signal CLK. Q and Q' are the outputs where Q' is the complement of Q. The supply voltages are slowly varying complementary triangular waveforms (PC and $\overline{PC}$).

Simulated timing waveforms are shown in Fig. 6(b). The combination of inputs at each negative edge of clock pulse '10, 01, 11' are given in the form of strings. The output Q and Q' changes according to the inputs at each negative edge of clock pulse. Q= '1' and Q'= '0' when J='1' and K= '0'. Similarly Q= '0' and Q'= '1' when J= '0' and K= '1'. Output Q will be complemented when J= '1' and K= '1'. Further the outputs Q and Q' are lathed to their corresponding values other than the negative edges of clock pulses. It may be observed that the waveforms of outputs Q and Q' have ripples, that is due to the continuous charging and discharging through the triangular type power clocks.

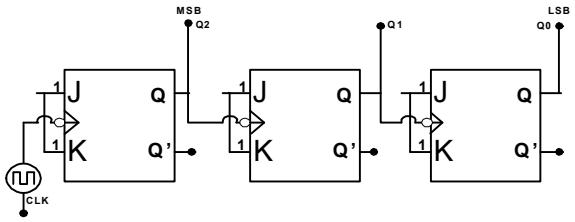

Fig. 7(a): MCEPAL based 3 bit up-counter circuit diagram

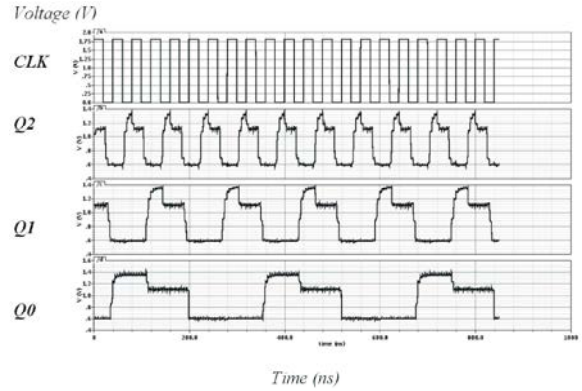

Fig. 7(b): Simulated MCEPAL 3 bit up-counter timing waveform

MCEPAL Based 3 Bit Binary up Counter: The proposed 3 bit binary up counter can be designed by using 3 MCEPAL JK flip flop for each binary bit. This counter will increment once for every clock cycle and count from zero to seven before it overflows. Supply clocks are triangular waveforms (PC and $\overline{PC}$).

Simulated timing waveforms of 3 bit up-counter are shown in Fig. 7(b). Q2 is always toggle at each negative edge of clock pulse (J and K are HIGH). Q1 is toggle at negative edge of Q2.

Similarly Q0 is toggle at negative edge of Q1. The combination of outputs (Q2Q1Q0) at different negative edge of clock pulse is '000, 001, 010, 011, 100, 101, 110, 111'. This is asynchronous counter thus its delay will be large but due to its simplicity it have been frequently used in literature. It may be observed that the output waveforms have ripples that are due to the continuous charging and discharging through the triangular type power clocks. The power dissipation due to these ripples or glitches is very small so can be neglected.

RESULTS AND DISCUSSION

The comparison of a MCEPAL, CEPAL and CMOS based MUX, JK flip-flop and 3 bit counter circuits with similar parameters (f_{in}<100MHZ,f_{pc}=100MHZ and V_{DD}=1.8V) has been shown in Table 2.

It is observed that MCEPAL based counter, JK flip flop and 2:1 multiplexer exhibits a power saving of up to 48%, 25% and 77% respectively with an increase in delay to their respective CEPAL counter parts but this increased delay can be traded off because in our proposal performance is dominated by low power. The delay in counter circuit is very large because of its asynchronous behavior. It is also observed that both the adiabatic inverters have significant power saving in comparison to their CMOS counterparts.

The layout of a MCEPAL inverter circuit has been drawn as shown in Fig. 8. From the layout it has been characterized that the chip area of a MCEPAL ineverter is higher than the CMOS circuit due to the four extra MOSFET diodes. MCEPAL inverter has 41.23µm^2 area while CMOS inverter has 14.54µm^2.

Table 2: Comparison of MCEPAL, CEPAL and CMOS based circuits

		Topology		
Circuits	Parameters	MCEPAL	CEPAL	CMOS
2:1 MUX	Power dissipation(µW)	0.008	0.037	0.35
	Delay (ns)	3.75	0.92	0.22
	Output swing	0.5 to 1.36	0.48 to 1.38	0to 1.8
JK flip-flop	Power dissipation(µW)	0.002	0.003	0.379
	Delay (ns)	3.04	0.73	0.31
	Output swing	0.56 to 1.47	0.56 to1.47	0to 1.8
3-bit counter	Power dissipation(µW)	0.098	0.19	2.5
	Delay (ns)	3.04	0.73	0.31
	Output swing	0.56 to1.47	0.56 to1.47	0to 1.8

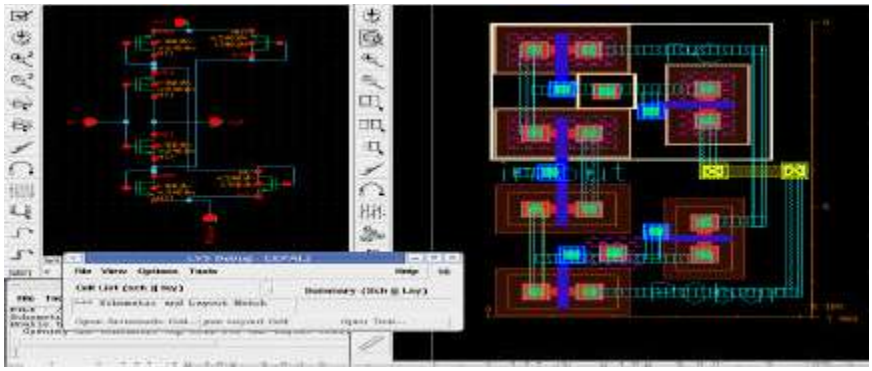

Fig. 8: Layout of a MCEPAL inverter circuit

CONCLUSION

We have presented a new adiabatic topology i.e. modified CEPAL (MCEPAL) circuits and its performance with different parameter variation have been evaluated in terms of power dissipation and delay. We have also proposed MCEPAL based multiplexer, JK flip flop and 3 bit counter circuit. MCEPAL based circuits consumes lesser power with an incremented delay compared to already available adiabatic (i.e. CEPAL) circuits and conventional CMOS circuit. The presented circuit has low on chip power density and thus it can be used in power aware high-performance VLSI circuitry.

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