True Material Limit of Power Devices - Applied to 2D Superjunction MOSFET

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Abstract— **Predictions on limits of silicon in power devices have failed spectacularly in the past, but in spite of that, the theory that generated them is still used today and adapted for wide bandgap materials to justify their superior standing against silicon. The superjunction MOSFET was the first device to break by more than one order of magnitude the so-called 'limit of silicon' above 600V. The current theory of superjunction seems however to define a new technology based limit rather than a material based only limit. This implies that by scaling down the dimensions, in particular the cell pitch, the on-state resistances can continually decrease by several orders of magnitude, without a boundary. This paper shows that the down scaling of the cell dimensions cannot happen indefinitely and there is a material dependent intrinsic limit for any power device, which no longer is limited by the geometry or the technology available. Using an analytical approach, and backed up by advanced numerical simulations, we show that the minimum cell pitch is 0.18 µm for silicon and 0.05 µm for 4H-silicon-carbide, and further reduction in the cell pitch would result in an increase in the specific resistance. Finally, a new figure of merit for a superjunction MOSFET based on a rigorous 2D analysis is defined.**

Index Terms— **Power devices, Superjunction, JFET, Limit of superjunction.**

I. INTRODUCTION

From the 1980s, the power metal oxide semiconductor field effect transistor (MOSFET) has been dominating a major part of the power industry for high frequency and high voltage applications. In particular, the power MOSFET with a vertical drift region can sustain high voltages in the off-state with a moderately low on-state resistance. *Baliga* has shown that the specific on-state resistance of the power MOSFET ($R_{sp.standard}$) increases with the square of breakdown voltage, V_B, and is inversely proportional to the cube of the critical field [1], [2]. The specific on-state resistance can be expressed as:

$$R_{sp.standard} = \frac{4V_B^{\,2}}{\mu_n \varepsilon_S E_C^3} \left(\Omega \cdot cm^2\right). \tag{1}$$

Where μ_n, ε_s, and E_C are the electron mobility, the permittivity of a semiconductor material, and the critical electric field, respectively. The relationship was derived using a 1D Poisson theory, and for many years, when applied to silicon, the relationship was known as 'the limit of silicon'.

While the theory was correct for a MOSFET design, it was wrong to infer that it could define a limit of a material. The introduction of the superjunction in the late 90s, has shown that adopting a different design based on a two-dimensional geometry with compensating n/p pillars in the drift region, the specific on-state resistance can be cut by more than order of magnitude [3]–[7]. The CoolMOS, concept, was released in 1998 [7] with the catching title 'of breaking the limit of silicon'. An early theoretical study of the superjunction, widely adopted today, concept was introduced by *Fujihira* [3] with the specific on-state resistance given by:

$$R_{sp.SJ} = \frac{4V_B}{\mu_n \varepsilon_S E_C^2} d \quad (\Omega \cdot cm^2), \tag{2}$$

where d is a cellpitch of a superjunction device. The main advantage of the use of a superjunction structure within the drift region is that the specific on-state resistance is linearly proportional to the breakdown voltage. At the same time, the superjunction has a potential for further reduction of R_{sp} by scaling down the cellpitch, d. Nevertheless, *Fujihira*'s approach does not consider the parasitic junction field effect transistor (JFET) effect, and, as a result, by decreasing the cellpitch, the specific resistance in Fujihira's model can be reduced indefinitely without any limitation. This infers that there is no 'boundary' associated with a material in particular, and the minimum achievable on-state resistance is dictated by the technological capability. As first demonstrated by Disney *et al* [8], a parasitic JFET effect exists in the superjunction structure which significantly narrows the conduction width of the on-state current, and thus leads to an increase in the specific on-state resistance. This parasitic JFET effect is prominent at higher drain voltages, but even at zero bias, a depletion region exists, given by the intrinsic potential associated with the junction between n/p pillars. In Fig. 1(a), the effective conduction path is given by $(d\text{-}W_{bi})/2$, within the drift region, where W_{bi} is the depletion region created by the built-in voltage, ψ_{bi}.

The goal of this research is to find a "true limit" and a "true figure of merit" for a superjunction MOSFET, and to understand what parameters of the material contribute to the ultimate limit of the superjunction. For this, a new approach for a superjunction MOSFET is developed to take into account the parasitic JFET of the superjunction. The specific on-state resistance is defined as the inverse of the slope in the current-

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voltage output characteristics at zero bias. As per previous studies, the contributions of the channel and substrate resistances are neglected. Under the consideration of zero-bias depletion width in the superjunction, the minimum resistance is calculated and a new figure of merit for the superjunction MOSFET is established. This is exemplified for silicon and 4H-silicon-carbide (SiC) devices. As shown in Fig. 1(b), assuming the p-type gate is grounded, the SJ structure can be regarded as a grounded gate JFET. The gate of the JFET is connected to the source (See Fig. 1(c)), and the channel of the JFET is normally open. The depletion of the JFET (superjunction) is determined by two factors: 1) the built-in potential between the p-type gate (p-pillar) and the n-drift (n-pillar), 2) the voltage applied to the drain.

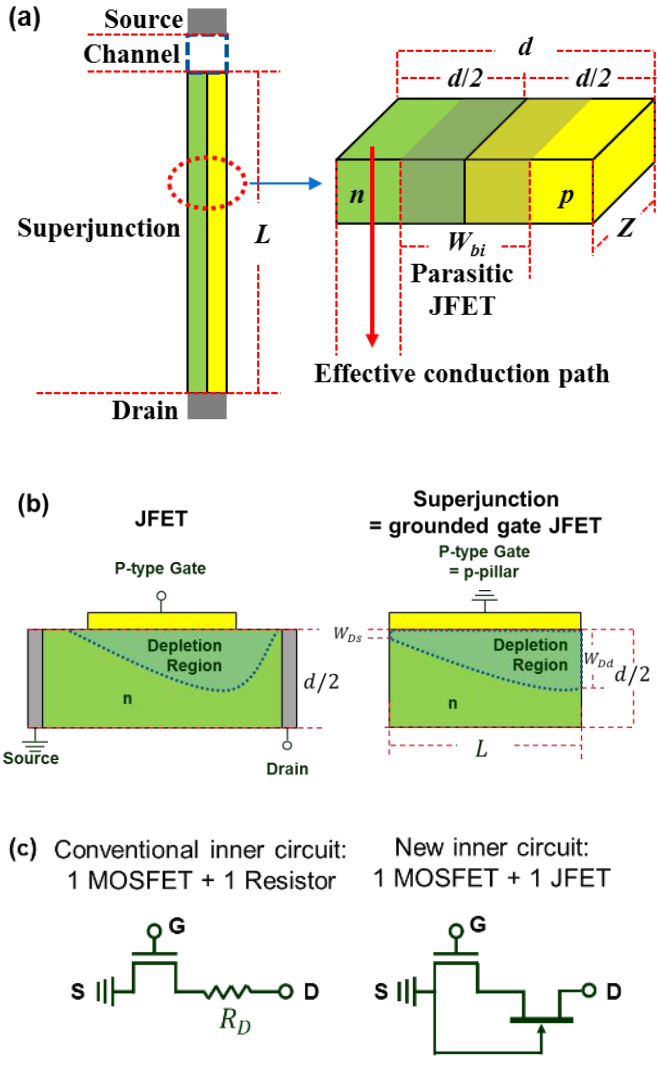

Fig.1. Illustration of (a) the zero-bias parasitic JFET in a superjunction MOSFET, (b) the pillars of a superjunction as a grounded gate JFET, and (c) a new inner circuit model for a superjunction MOSFET

II. JFET Model of Superjunction MOSFET

It should be noted that as shown in Fig. 1(a), the p-pillar and the n-pillar have the same width, $d/2$, and the same dopant concentration, N_D (for charge balance). When the p-pillar is in the grounded state, the required voltage to fully deplete both n-pillar and p-pillar can be defined by solving one-dimensional Poisson equation:

$$\psi_p = \frac{qN_D d^2}{4\varepsilon_S} \ (V). \tag{3}$$

By applying a drain bias, V_{DS}, on the drain, the depletion width, W_{Ds}, and, W_{Dd}, can be expressed as the following simple depletion equations [9]:

$$W_{Ds} = \sqrt{\frac{\varepsilon_S \psi_{bi}}{qN_D}} = \frac{d}{2}\sqrt{\frac{\psi_{bi}}{\psi_p}} = \frac{d}{2}u_s \ (cm), \tag{4}$$

$$W_{Dd} = \sqrt{\frac{\varepsilon_S (\psi_{bi} + V_{DS})}{qN_D}} = \frac{d}{2}\sqrt{\frac{\psi_{bi} + V_{DS}}{\psi_p}} = \frac{d}{2}u_d \quad (cm), \tag{5}$$

where q and ψ_{bi} are unit charge and built-in potential between the p-pillar and the n-pillar, respectively. By using the total sheet charge, $Q_n(x)$, in the n-pillar,

$$Q_n(x) = qN_D(a - W_D) \quad (cm^{-2}), \tag{6}$$

the drain current can be expressed as,

$$I_D(x) = ZQ_n(x)v(x) \quad (A), \tag{7}$$

where x, Z, W_D and $v(x)$ are, the lateral dimension from source to drain, the depth of pillar into the paper (the third dimension), a depletion width at a specific bias, and the velocity of the majority carrier. By integrating the current in equation (7) from left (0) to right (L) end, the drain current yields

$$I_D(x) = \frac{Z}{L}\int_0^L Q_n(x)v(x)dx \quad (A), \tag{8}$$

where L is the length of the superjunction pillar as shown in Fig .1. Since the differential form of the depletion width with respect to the applied voltage, V, has the following relationship,

$$\frac{dW_D}{dV} = \frac{\varepsilon_S}{2qN_D W_D} \quad (cm/V). \tag{9}$$

By inserting equation (9), and $v(x)=\mu_n dV/dx$ into equation (8), the drain current with respect to the applied drain bias, V_{DS}, leads to the following result:

$$I_D = \frac{2Z\mu_n q^2 {N_D}^2}{\varepsilon_S L}\int_{W_{Ds}}^{W_{Dd}} \left(\frac{d}{2} - W_D\right)W_D dW_D \ (A), \tag{10}$$

$$I_D = \frac{Z\mu_n q^2 {N_D}^2 d^3}{24\varepsilon_S L}\cdot U(V_{DS}) \quad (A), \tag{11}$$

where $U(V_{DS})$ in the second term of equation (11) is

$$U(V_{DS}) = 3\left(u_d^2 - u_s^2\right) - 2\left(u_d^3 - u_s^3\right), \tag{12}$$

The $U(V_{DS})$ in equation (11) is a V_{DS} dependent JFET function describing the parasitic JFET (or depletion) due to the built-in potential and applied drain bias. By dividing the drain voltage, V_{DS}, by the drain current in equation (9) and multiplying the cell area, dZ, the equation for specific resistance is obtained as

$$R_{sp} = \frac{V_{DS}}{I_D} \times dZ = \frac{24\varepsilon_S L}{\mu_n q^2 {N_D}^2 d^2}\cdot\frac{V_{DS}}{U(V_{DS})} \quad (\Omega \cdot cm^2). \tag{13}$$

When V_{DS} approaches to zero, R_{sp} has a minimum value because the V_{DS} dependent JFET expansion can be ignored. By applying the well-known *L'Hospital*'s rule[10] to the second term of equation (13), $V_{DS}/U(V_{DS})$ can be written as

$$\lim_{V_{DS}\to 0}\frac{V_{DS}}{U(V_{DS})}=\frac{1}{3}\frac{\psi_p\sqrt{\psi_p}}{\sqrt{\psi_p}-\sqrt{\psi_{bi}}}\quad(V)\,. \tag{14}$$

Inserting the pinch-off potential of the pillar in equation (3) into the first term of (13), and (14) into the second term of (13), the R_{sp} at V_{DS}= *0 V* finally leads to

$$R_{sp}=\frac{2L}{q\mu_n N_D}\cdot\left(\frac{\sqrt{\psi_p}}{\sqrt{\psi_p}-\sqrt{\psi_{bi}}}\right)\quad(\Omega\cdot cm^2)\,. \tag{15}$$

The first term of equation (15) is an ideal specific resistance of a superjunction structure with a conductance of $q\mu_n N_D$, and the second term is the JFET function when V_{DS}= *0 V*. In other words, cellpitch, d, and zero-bias depletion width, W_{bi}, are proportional to square root of ψ_p and ψ_{bi}, and, therefore, equation (15) can also be described in terms of the dimensional terms, d, and W_{bi}:

$$R_{sp}=\frac{2L}{q\mu_n N_D}\cdot\left(\frac{d}{d-W_{bi}}\right)\quad(\Omega\cdot cm^2)\,. \tag{16}$$

Intuitively, equation (16) can be proved with a simple observation. As shown in Fig. 1, the real resistance should be multiplied by the ratio of ideal conduction width, $d/2$, and the effective conduction width, $(d\text{-}W_{bi})/2$. This means that the JFET approach is quite reasonable when describing the on-state R_{sp} of a superjunction MOSFET. Equation (16) gives us an insight that the R_{sp} will not be decreased without limit by scaling down the cellpitch, d, because the built-in depletion width, W_{bi}, in the denominator will have a value comparable with, d. Further, by replacing the first term in equation (16) with *Fujihira*'s ideal model in equation (2), equation (15) can be transformed to the following equation (17):

$$R_{sp}=\frac{4V_B}{\mu_n\varepsilon_S E_C^2}d\cdot\left(\frac{\sqrt{\psi_p}}{\sqrt{\psi_p}-\sqrt{\psi_{bi}}}\right)(\Omega\cdot cm^2)\,. \tag{17}$$

It should be noted that, as shown by *Fujihira*, the breakdown voltage, V_B, has a relationship, V_B= $E_C L/2$.

III. Comparison of Analytical Model with Simulation

In equation (16), the doping concentration, N_D that gives an optimum trade-off between R_{sp} and V_B has been identified by *Fujihira*, is given by the following relationship [3]:

$$N_D=\frac{\varepsilon_S E_C}{qd}\quad(cm^{-3})\,. \tag{18}$$

According to *Baliga* the critical field [2], E_C has a mild dependence on the doping concentration, N_D, as follows for Si:

$$E_C(Si)=4.0\times10^3\cdot N_D^{1/8}\quad(V/cm)\,, \tag{19-1}$$

and, for 4H-SiC:

$$E_C(SiC)=3.3\times10^4\cdot N_D^{1/8}\quad(V/cm)\,. \tag{19-2}$$

By inserting equation (19-1) and (19-2) into equation (18), the doping concentration can be expressed as a function of cellpitch, d: for Si,

$$N_D(Si)=C_{N.Si}\cdot d^{-8/7}=7.88\cdot10^{11}\cdot d^{-8/7}\ (cm^{-3})\,, \tag{20-1}$$

and, for 4H-SiC,

$$N_D(SiC)=C_{N.SiC}\cdot d^{-8/7}=7.13\cdot10^{12}\cdot d^{-8/7}\ (cm^{-3})\,. \tag{20-2}$$

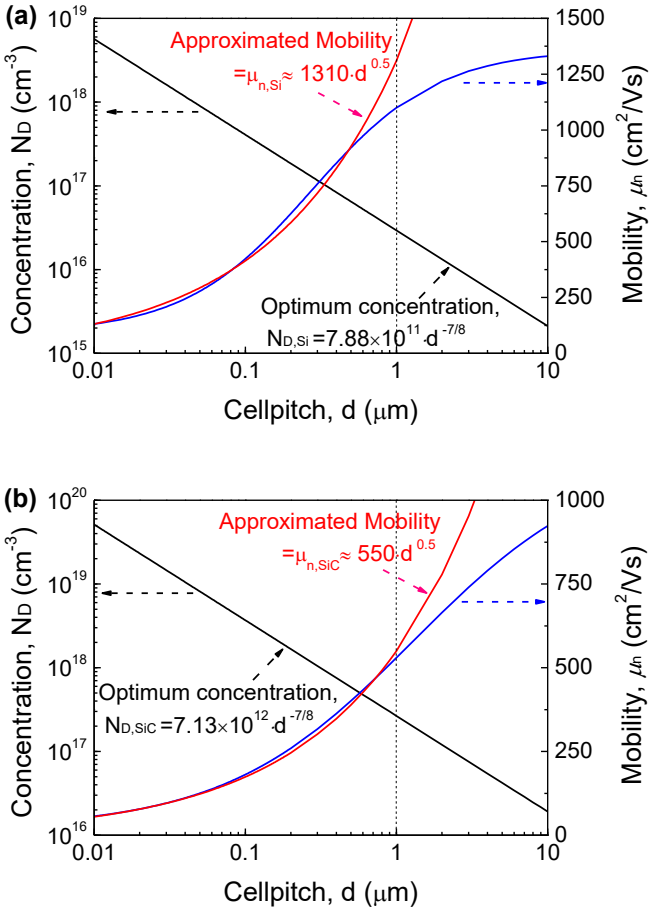

Fig. 2. Value of optimum concentration (black line), mobility (blue line), and approximated mobility below 1 μm (red line) with respect to the cellpitch for Si (a), and SiC (b).

The optimum concentration of 4H-SiC is around 9 times higher than that of silicon, and, as the cellpitch, d, is decreased, the concentration becomes higher. Once an optimum concentration is given, the N_D dependent mobility, μ_n, can be defined at each cellpitch using previously measured data[11], [12] obtained, see Fig. 2 (blue line). Additionally, both the pinch-off potential, ψ_p, and built-in potential, ψ_{bi}, at a given cellpitch can be determined by using the values of optimum concentration given by equation (20).

Fig. 3 shows the results of the analytical model given by equation (15) and simulation result for Si and SiC at L= *40 μm*.

Both the analytical model and the simulation results show the same trend and nearly the same R_{sp} for the entire range of the cellpitch. Initially, R_{sp} of both Si and SiC devices decrease linearly because the zero-bias depletion width, W_{bi}, is negligible compared to the cellpitch, d. However, as the cellpitch diminishes below 1 μm, the rate of decrease of the R_{sp} becomes slower owing to the relatively increased JFET width, and, finally, both R_{sp} reach minimum values at 0.18 μm ($N_D = 2.08\times10^{17}\ cm^{-3}$) for Si and 0.05 μm ($N_D = 7.47\times10^{18}\ cm^{-3}$) for SiC, respectively. Inconsistent to the previous ideal model given by equation (2), further decrease of the cellpitch leads to a rapid increase of R_{sp} owing to the significantly increased JFET width. It should be noted that the length of the pillar, L, is not a function of the cellpitch, d, i.e., L does not contribute to the optimum cellpitch point of R_{sp}.

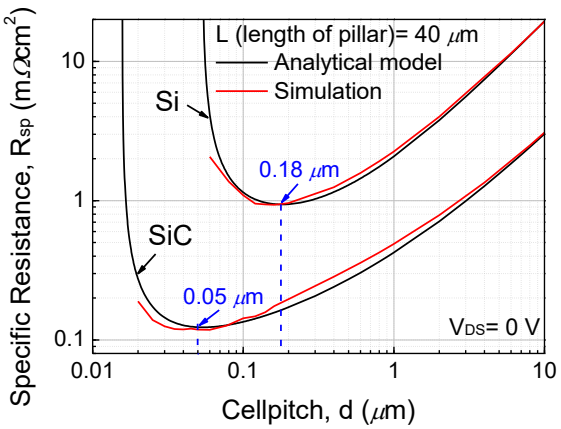

Fig. 3. Calculation of the analytical model in equation (15) with respect the cellpitch (black line), and the simulation result (red line) for Si and 4H-SiC. Length of pillar, $L = 40\ \mu m$.

For a practical on-state operation, with increasing the drain voltage, the R_{sp} increases because the JFET region in the superjunction expands and thus narrowing the conduction path (n-pillar) [8]. At the same time, the electron mobility decreases (electron velocity increases) and, therefore, a V_{DS} dependent mobility model should be employed. Referring to equation (13), an empirical model for electron mobility $\mu_n(V_{DS}, N_D)$ can be expressed as following equation:

$$\mu_n(V_{DS},N_D)=\frac{\mu_{n0}}{\left(1+\left(\frac{V_{DS}}{E_C L}\right)^{\frac{1}{m}}\right)^{3m}},\ m=1.73\ . \qquad (21\text{-}1)$$

Where μ_{n0} is an impurity concentration dependent mobility when $V_{DS} = 0$, and μ_{n0} can be referred from Baliga's study [2]:

$$\mu_{n0}(Si)=\frac{5.10\times10^{18}+92N_D^{0.91}}{3.75\times10^{15}+N_D^{0.91}}, \qquad (21\text{-}2)$$

$$\mu_{n0}(4H-SiC)=\frac{4.05\times10^{13}+20N_D^{0.61}}{3.55\times10^{10}+N_D^{0.61}}\ . \qquad (21\text{-}3)$$

Inserting the V_{DS} dependent mobility model given by (21-1) into equation (13), the R_{sp} with respect to V_{DS} can be plotted in Fig. 4. It should be noted that the mobility model in equation (21-1) assumes an average of the electron mobility throughout the entire n-pillar. In reality, when a value of the drain bias is applied during on-state, the lower part of the pillar sustains a higher portion of the applied voltage than the upper part of the pillar because the JFET width of the lower part is wider than that of the upper part. Therefore, the value of the mobility of the lower part of the pillar should be lower than that of the upper part of the pillar. This effect is however taken into account by using a simplified model with an average value of the mobility.

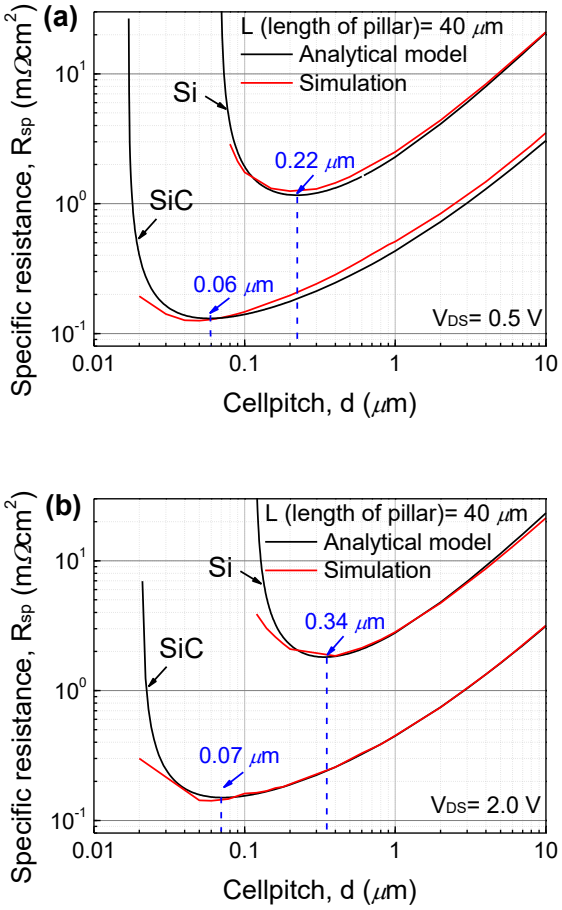

Fig. 4. Calculation of the analytical model in equation (13) with respect the cellpitch (black line), and the simulation result (red line) for Si and 4H-SiC. (a) $V_{DS} = 0.5\ V$, (a) $V_{DS} = 2.0\ V$. Length of pillar, $L = 40\ \mu m$.

As shown in Fig. 4. The analytical model showed almost the same trend as the simulation data. As the applied drain bias increases, the value of the R_{sp} increases for the entire cellpitch owing to the expanded JFET width in the n-pillar. Additionally, as expected, the minimum cellpitch is shifted toward a higher cellpitch: for Si, 0.18 μm (0 V), 0.22 μm (0.5 V), and 0.34 μm (2.0 V), for SiC, 0.05 μm (0 V), 0.06 μm (0.5 V), and 0.37 μm (2.0 V). These results mean that there is a minimum condition when a superjunction's R_{sp} starts to increase again. This discussion will be presented in the next section. By utilizing the R_{sp} model, and the mobility model given by equation (13) and (21), practical R_{sp} and current density can be obtained at a

given drain bias.

IV. True Figure of Merit for Superjunction

The last step of this research is finding a new figure of merit which can describe the minimum R_{sp} as found in Fig. 3. In equation (15), except for q and L, all of the parameters can be expressed as a function of cellpitch, d. Especially, below 1 μm, as shown in Fig. 2, the electron mobility, μ_n, is approximately dependent on a square root of d: for Si,

$$\mu_n(Si) \cong C_{\mu.Si} \cdot d^{1/2} = 1310 \cdot d^{1/2} \quad (cm^2/(V \cdot s)), \qquad (22\text{-}1)$$

and, for SiC,

$$\mu_n(SiC) \cong C_{\mu.SiC} \cdot d^{1/2} = 550 \cdot d^{1/2} \quad (cm^2/(V \cdot s)). \qquad (22\text{-}2)$$

Pinch-off potential, ψ_p, also can be expressed in terms of d, by combining equation (3) with (20-1) for Si,

$$\psi_{p.Si} = C_{\psi.Si} \cdot d^{6/7} = 3.07 \times 10^4 \cdot d^{6/7} \quad (V), \qquad (23\text{-}1)$$

and by combining equation (3) with (20-2) for SiC,

$$\psi_{p.SiC} = C_{\psi.SiC} \cdot d^{6/7} = 3.34 \times 10^5 \cdot d^{6/7} \quad (V). \qquad (23\text{-}2)$$

By inserting the optimum concentration, N_D, given by equation (20), the electron mobility, μ_n, (22) and the pinch-off potential, ψ_p, (23) into equation (15), the R_{sp} can be expressed as a function of d:

$$R_{sp} = \frac{2L}{q}\left(\frac{1}{C_\mu d^{1/2} \cdot C_N d^{-8/7}} \cdot \frac{\sqrt{C_\psi d^{6/7}}}{\sqrt{C_\psi d^{6/7}} - \sqrt{\psi_{bi}}}\right) = \frac{2L}{q} \cdot \Psi(d)$$

$$(\Omega \cdot cm^2). \qquad (24)$$

It should be noted that, since the minimum R_{sp} is presented at high impurity concentration, the built-in potential, ψ_{bi}, can be assumed to be near the potential of the semiconductor's bandgap, E_g/q, where E_g is the energy bandgap of a material. When the differential form, $\partial\ \Psi(d)/\ \partial d$, in Equation (24) is equal to zero, $\Psi(d)$ has a minimum value and the condition of this is as follows:

$$\sqrt{\frac{\psi_{bi}}{\psi_p}} = \frac{W_{bi}}{d} = \frac{3}{5}, \qquad (25)$$

where W_{bi} is a built-in depletion width of a superjunction or the width of the parasitic JFET as shown in Fig. 1(a). When the width of parasitic JFET, W_{bi}, occupies 60 % of the cellpitch, d, the superjunction MOSFET reaches a minimum R_{sp} and further expansion of the JFET rather increases R_{sp}. Additionally, inserting the pinch-off potential relationship in equation (3), the optimum concentration relationship in equation (18) into equation (25), and assuming $\psi_{bi} = E_g/q$, the optimum cellpitch, can be expressed by the material parameters:

$$d_{OP} = \frac{50}{9}\frac{E_g}{qE_c} \quad (cm). \qquad (26)$$

This relationship indicates the optimum cellpitch, d_{OP}, moves to a relatively lower value when the used material has a relatively higher bandgap. In a more quantitative perspective, according to *Hudgins*'s study [13], a semiconductors' critical electric field with an indirect bandgap showed the relationship , $E_C \propto E_g^{2.0}$, and, therefore, the optimum cellpitch should be shifted at least by the reciprocal amount of the bandgap:

$$d_{OP} \propto \frac{1}{E_g}. \qquad (27)$$

By inserting the minimum JFET condition in equation (25) and the optimum cellpitch in equation (26) into equation (17), a new specific resistance for a superjunction MOSFET is defined:

$$R_{sp} = \frac{500}{9}\frac{E_g}{q\mu_n \varepsilon_S E_C^3} V_B \quad (\Omega \cdot cm^2). \qquad (28)$$

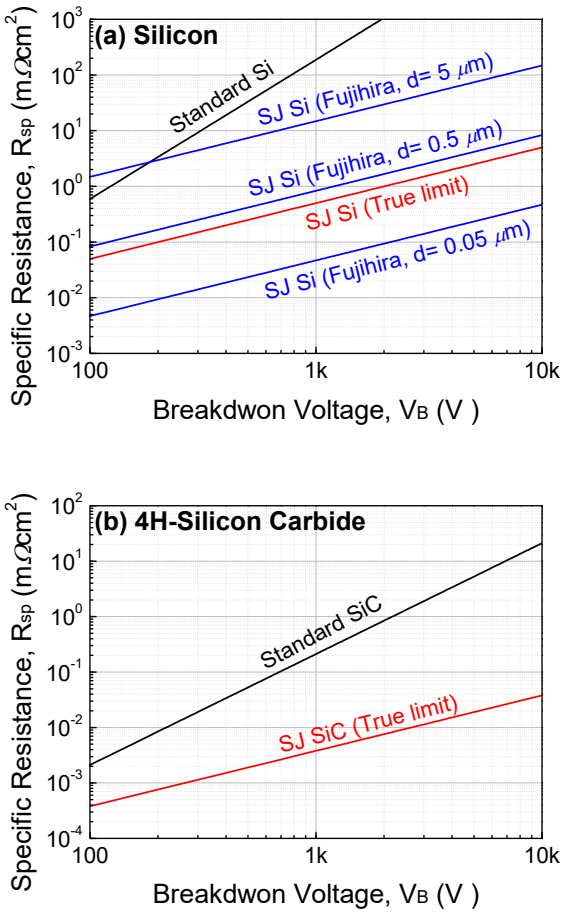

Fig. 5. Specific resistance versus breakdown voltage for power MOSFETs, (a) Si MOSFET: standard (black line), Redrawn Fujihira's ideal superjunction (blue line) [3], and true limit of superjunction (red line), (b) 4H-SiC MOSFET: Standard (black line), and true limit of superjunction (red line)

As with the original ideal model given in equation (2), the real R_{sp} is linearly proportional to V_B. However, owing to the zero-bias depletion in the superjunction, the unconfined dimensional factor, d, is replaced by E_g/qE_C. As a result, the on-state resistance is proportional to $V_B E_g/\mu_n \varepsilon_s E_C^3$ rather than $V_B d/\mu_n \varepsilon_s E_C^2$. Additionally, by applying *Hudgins*'s relationship [13], $E_C \propto E_g^{2.0}$, it can be found that the R_{sp} of the superjunction MOSFET is inversely proportional to E_g^5:

$$R_{sp} \propto \frac{V_B}{\mu_n \varepsilon_S E_g^5} . \quad (29)$$

or is inversely proportional to $E_c^{2.5}$:

$$R_{sp} \propto \frac{V_B}{\mu_n \varepsilon_S E_c^{2.5}} \quad (30)$$

The value of R_{sp} with respect to a given V_B is calculated by substituting the optimum values for each parameter in equation (28). For Si,

$$R_{sp.Si} = 4.99 \times 10^{-4} \cdot V_B \quad (m\Omega \cdot cm^2) , \quad (31\text{-}1)$$

where E_g= 1.12 (eV) [13], μ_n= 592 (cm^2/Vs), E_C= 5.86×10^5 (V/cm), ε_{Si}= 1.03×10^{-12} (F/cm) [12]. For example, a commercial silicon power MOSFET with 600 V rating never falls below 0.3 $m\Omega cm^2$. In the case of 4H-SiC,

$$R_{sp.siC} = 3.79 \times 10^{-6} \cdot V_B \quad (m\Omega \cdot cm^2) , \quad (31\text{-}2)$$

where E_g= 3.25 (eV) [13], μ_n= 130 (cm^2/Vs), E_C= 7.54×10^6 (V/cm), ε_{SiC}= 8.55×10^{-13} (F/cm) [12].

Based on the above values, a SiC power device can have around 130 times lower R_{sp} than a Si device at the optimum conditions. However, one should point out that technological limitations may limit the ultimate reduction in the SiC on-state resistance as the pillars require very heavy doping, N_D= 7.47×10^{18} cm^{-3} and the minimum pillar width is only 50 nm. We have also made the assumptions that no quantum effects apply, and this is justified by the relatively large dimensions considered (quantum effects are more prominent at sub 10 nm levels). Table 1 shows the 'ideal' on-state resistances as derived by *Baliga* [1], [2], *Fujihira* [3] and in this study (*Kang* and *Udrea*). This is applied to both silicon and silicon carbide. *Baliga*'s ideal on-state resistance, based on a standard MOSFET, is only material dependent and results in a correct estimation for a standard power MOSFET but cannot be applied to superjunctions and therefore cannot result in a meaningful 'limit of silicon'. *Fujihira*'s on-state resistance applied to superjunctions is more realistic as an ideal limit for a given material, but it is important to state that it does not take into account the JFET effect and moreover, it cannot be applied to very narrow geometries, as for such geometries the effect of the built-in voltage (or the applied on-state voltage) cannot be neglected. Furthermore, *Fujihira*'s on-state resistance is not only material dependent but also geometry dependent (cellpitch). The on-state resistance calculated by *Fujihira* can be used only at relatively large cellpitches (e.g. greater than 0.9 μm for silicon and greater than 0.25 μm for SiC). In this study, we demonstrate that the ultimate (for the ideal) minimum on-state resistance is not geometry (or technology) dependent but only material dependent. The study takes into account the JFET effect created by the built-in potential between the superjunction pillars and it shows that there is a minimum cellpitch beyond which the on-state resistance can no longer be decreased. The minimum cellpitch depends on the material and is inversely proportional to the bandgap. The study has also been extended to take into account the increase in the on-state voltage (the drain-source voltage) on the JFET effect and consequently on the specific on-state resistance.

It should be however pointed out that today the on-state resistance is still limited by the available technology and superjunctions with submicron cellpitches are yet to be manufactured. For example, the lowest reported on-state resistance for a 650 V silicon superjunction device is 7.8 $m\Omega cm^2$ [14]. This was achieved with a cell pitch of approximately d= 1.5 μm. The latest commercial CoolMOS™, C7, device has a 10 $m\Omega cm^2$ [6], [15].

Table 2 shows a comparison of the Figures of merit (FOMs) for unipolar power devices. *Baliga*'s FOM (BFOM) [1], [2], *Fujihira*'s FOM (FFOM) [3] and the FOM derived from this study (new FOM) are applied to different materials and scaled versus silicon. BFOM is proportional with the E_c^3, FFOM with E_c^2 while the new FOM with $E_c^{2.5}$. The new FOM, based on a 2D superjunction design which accounts for the parasitic JEFT effect, appears to be placed in between the two previously derived FOMs. The new FOM is expressed as a function of the critical electric field but can be directly expressed as function of the bandgap of the material. In particular, the latter expression of the new FOM gives a straight meaningful comparison of the wide bandgap materials with a reference to silicon.

Table 1 Ideal on-state resistance for power MOSFET given by *Baliga*, *Fujihira*, and this research

		Baliga	***Fujihira***	***Kang* and *Udrea* *(this work)***
Si	R_{sp} $(m\Omega \cdot cm^2)$	$5.93 \times 10^{-6} \cdot V_B^{2.5}$	$1.98 \times 10^2 \cdot d^{5/4} \cdot V_B$	$4.99 \times 10^{-4} \cdot V_B$
	@600 V	52.3	0.50 (d= 0.5 μm), 0.028 (d= 0.05 μm)	0.30
	@1200 V	295.8	1.00 (d= 0.5 μm), 0.056 (d= 0.05 μm)	0.60
4H-SiC	R_{sp} $(m\Omega \cdot cm^2)$	$5.55 \times 10^{-9} \cdot V_B^{2.5}$	-	$3.79 \times 10^{-6} \cdot V_B$
	@600 V	0.05		0.002
	@1200 V	0.28		0.005

Table 2 Figure of merit (FOM) for specific resistance of power MOSFET given by Baliga, Fujihira, and this research

Material	$\mu_n\left(cm^2/V\cdot s\right)$	ε	$E_C\left(MV/cm\right)$	***Baliga*** $\mu_n\cdot\varepsilon_S\cdot E_C^3$	***Fujihira*** $\mu_n\cdot\varepsilon_S\cdot E_C^2$	***Kang* and *Udrea* *(this work)*** $\mu_n\cdot\varepsilon_S\cdot E_C^{2.5}$
Si	1350	11.8	0.3	1	1	1
4H-SiC	720	10	2	134	20	52
h-GaN	900	9	3.3	677	62	204
β-Ga_2O_3	300	10	8	3571	134	692
AlN	1100	8.7	11.7	35636	914	5706
Diamond	1900	5.5	5.6	4267	229	988

It is also worthwhile noting that in order to improve the performance of a classical power MOSFET, field plates (FP) have been used in the drift region of a power MOSFET [16]–[18]. Saito compared a SJ with a FP MOSFET and found that the theoretical limits for both SJ and FP are the same [18]. It is worth to note that a FP design is advantageous for a low voltage application (100 ~ 200 V) while the SJ design is more suitable for higher voltage when considering a combination of ease of manufacturing and energy efficiency. Whereas the analysis in this paper is based on a flat vertical electric field and a charge balance in the pillars, Saito's paper assumed a vertically bended electric field and a charge imbalance condition [19]. In particular, when there is a gradual charge imbalance from the bottom to the top of the pillars, the vertical electric field of the superjunction has an arch profile. Maximum electric field (breakdown) occurs in the middle of the pillars for a charge balance case. Saito analysed the decrease in the breakdown for the amount of the bending of the vertical electric field and suggested an optimum condition for a superjunction design [19]. A simple model for the effect of the charge imbalance on the breakdown voltage was provided in a previous publication using a charge superposition principle, but the research did not deal with the minimum on-state resistance or defining FOMs [20].

V. Conclusions

A new method for determining the specific on-state resistance of a superjunction MOSFET which accounts for the parasitic JFET was introduced. The analytical theory developed here is backed up by extensive numerical simulations. The study generates a new 'ideal' minimum on-state resistance function of the breakdown voltage. This can be applied to different materials for unipolar power devices such as silicon or SiC. We have proven that there is a minimum cellpitch in superjunctions below which the on-state resistance can no longer decrease. This is in contrast with the widely used theory of superjunction proposed by *Fujihira*. The minimum cellpitch is shown to be 0.18 μm for Si and 0.05 μm for 4H-SiC. For example, when applied to a 600V breakdown voltage, these give a minimum possible specific on-state resistances of the drift region of 0.30 $m\Omega cm^2$ for Si and 2.28 $\mu\Omega cm^2$ for SiC. Furthermore, a new figure of merit for unipolar devices was defined and applied to different materials. This new FOM which takes into account a superjunction design and the effect of the built-in potential shows a dependence with the electric field to the power of 2.5, (or bandgap to the power of 5) which is placed between the more traditional *Baliga*'s Figure of Merit (BFOM) and that derived by *Fujihira* for superjunctions (FFOM).

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