True random number generation by variability of resistive switching in oxide-based devices

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Abstract—**Scalable, low-power random number generator (RNG) blocks are essential for encryption in today's communication systems. To allow for true RNG, a system must display an inherently-random physical phenomenon, such as the timing of individual fluctuations in random telegraph noise (RTN) or the random trapping/detrapping phenomena in dielectrics. In this work, a true RNG based on set variability in a resistive switching memory (RRAM) is demonstrated. The RNG relies on a single RRAM device, which is repeatedly programmed at a constant voltage close to the nominal set voltage. Due to the statistical variability of the set voltage, set transition takes place only in 50% of the applied pulses, thus resulting in a bimodal distribution of resistance. The bimodal distribution of analog resistance is finally converted into a 0/1 distribution of output voltage values through digital regeneration with a CMOS inverter.**

Index Terms—**Nonvolatile memory, resistive-switching memory (RRAM), random number generation, memory reliability.**

I. INTRODUCTION

The random number generator (RNG) finds today its main application in data encryption for secure communication systems to prevent data theft. While pseudo-RNG may be easily predictable, a true RNG relies instead on a local physical phenomenon that is totally random, thus cannot be replicated or predicted externally. The search for a true RNG with scalable size, low power and insensitiveness to external parameters, such as temperature, is a key effort for the development of encryption systems.

Several concepts for true RNG were previously proposed [1-6]. These include the thermal noise in electronic circuit[1] and the random telegraph noise (RTN) in nanodevices, such as dielectric layers [2] or resistive switching memory (RRAM) [3]. RTN, in fact, is a physically random process, relying on the statistical probability to overcome a barrier for the transition from one state (*e.g.*, electron trapped in a local defect) to another (*e.g.*, empty defect). By probing the voltage across the device or the current flowing in it at periodic timing, *e.g.*, through a clock signal, a random sequence of high/low values can be obtained, which thus serves as the generated random bits. The RTN source, however, is difficult

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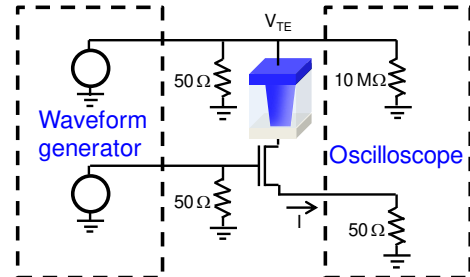
Fig. 1. Illustrative scheme for the 1T1R structure of the cell and for the measurement setup.

to activate and control. For instance, although both low-resistance state (LRS) and high resistance state (HRS) of RRAM often display RTN [7-8], the amplitude, average frequency and stability of the RTN source cannot be predicted. For instance, it was shown that, although the RTN amplitude correlates with the LRS resistance in RRAM devices, the statistical distribution of amplitude values is relatively broad [9]. Also, it was recently shown that RTN in HRS can be unstable, namely the RTN is randomly activated or deactivated without predictability [10]. Most recently, it was shown that switching variability in spin-transfer-torque (STT) magnetic memory (MRAM) could be used as true RNG [4]. The RNG concept is a random write operation in the device by applying a current for which the switching probability is 50%. In this way, the final state would be HRS in 50% of the cases, and LRS in the other 50%. Unfortunately, the resistance window of STT MRAM is quite limited, making the sensing of the random bit quite challenging. Switching variability in RRAM was also used to generate random bits for stochastic computing, where any number (*e.g.*, 0.4) can be represented by a sequence of random bits representing 0 and 1 (*e.g.*, 60% of 0 and 40% of 1) [5,6]. This highlights the potential of RRAM devices for true RNG.

In this work, we propose a physical RNG based on the switching variability in a single RRAM device[10-14]. The device is initially programmed in HRS, then a random set operation is carried out by applying a voltage in correspondence of the 0.5 probability for switching. This results in a bimodal distribution of resistance, where half of the states are in HRS and the other half are in LRS. The analog distribution of resistance is regenerated by a CMOS inverter stage. The manuscript is organized as follows: First, we discuss the switching process in our RRAM devices and
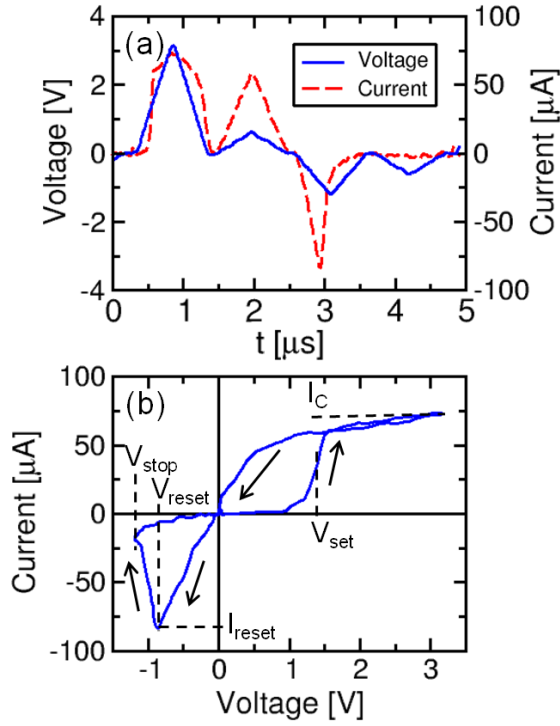
Fig. 2. Waveforms of TE voltage and current during a set/reset sequence (a) and corresponding measured I-V curves (b). The figure also shows the main parameters, namely the set voltage V_{set}, defined as the voltage marking the current crossing 40 µA, the compliance current I_C = 75 µA, the reset voltage V_{reset} marking the first decrease of current, the corresponding reset current I_{reset} and the peak voltage of the reset pulse V_{stop}.

we illustrate the stochastic switching phenomena through experiments. Then we present the RNG concept, defining the resistance window, the contrast and the switching probability which form the basis for the RNG. The calibration and regeneration methods for the RNG are finally discussed.

II. EXPERIMENTAL SAMPLE AND CHARACTERISTICS

Fig. 1 shows the measurement setup for the switching and RNG process. The device consists of a RRAM with AlO_x switching layer, TaN bottom electrode and Cu-containing top electrode. An integrated transistor was connected to the RRAM device to form a one-transistor/one-resistor (1T1R) structure, allowing for controllable switching at low current(< 75µA) and short pulse width (1 µs)[15, 16]. The RRAM device was initially formed by applying a DC sweep around 3 V. After forming, the devices shows resistive switching, where switching to the LRS is achieved by applying a positive set pulse, while switching to the HRS is achieved by a negative reset pulse [17]. During the set process, the gate voltage of the transistor is set to a relatively low value to limit the current passing through the device to a compliance current I_C, thus allowing a careful control of the resistance in the set state [19, 20]. The gate is instead biased to a relatively large value during the reset pulse, to minimize the series resistance of the select transistor. The gate and top-electrode (TE) voltages were controlled by a waveform generator, while the TE potential V and the current I where sensed by the oscilloscope as shown in Fig. 1.
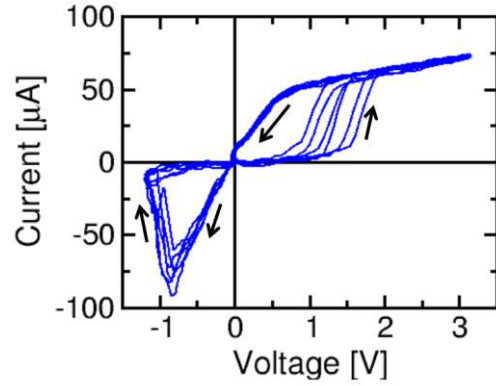

Fig. 3. Measured I-V curves for 6 repeated cycles on the same 1T1R structure. Note the stochastic switching phenomena, where all switching parameters, including the resistance in LRS and HRS, V_{set}, V_{reset} and I_{reset}, are affected by statistical fluctuations from cycle to cycle.

Fig. 2a shows the measured V and I during a typical set/reset experiment driven by triangular pulses of width t_P = 1 µs. Each set/reset cycle include 4 pulses for set, positive read, reset and negative read, respectively, with a separation of 100 ns from one pulse to the next one. The maximum voltage was 3.1 V for set, -1.2 V for reset, and ±0.6 V for read. Positive and negative read was used for set and reset state, respectively, to avoid any possible read disturb. Note the sharp increase of the current during the set pulse, which marks the set transition to the LRS, and the comparably sharp decay of the current during the reset pulse, evidencing the reset transition to HRS. From the measured voltage and current in Fig. 2a, the I-V curve of the 1T1R structure could be drawn as shown in Fig. 2b. Here, the set and reset processes can be clearly seen at positive and negative voltages, respectively. Set transition takes place at a positive voltage V_{set} of about 1 V, while reset transition occurs at a minimum voltage V_{reset} (about -0.9 V) and a maximum current I_{reset} (about 75µA). A compliance current I_C = 75 µA was used, resulting in a LRS resistance R of about 10 kΩ. The maximum voltage in the reset pulse was V_{stop} = -1.2 V, resulting in a HRS resistance of about 300 kΩ.

III. SWITCHING VARIABILITY

Fig. 3 shows measured I-V curves on the same 1T1R sample, repeated for 6 successive set/reset cycles. All the switching parameters appear to statistically fluctuate from cycle to cycle, which was explained by the random formation and disruption of the microscopic conductive filament (CF) in the RRAM device [11-15]. Generally, the HRS is most affected by switching variability: this is because the applied negative voltage results in a partial depletion of defects from the CF, generally in a region close to the bottom electrode [21]. Electrical conduction in the depleted gap is generally due to Poole-Frenkel conduction, where electrons hop over energy barriers from trap to trap in response to the electric field [22]. Any variation in the conduction path and in the energy barrier impacts exponentially the resistance in the hopping process, therefore the statistical variations of HRS resistance are relatively large. On the other hand, resistance fluctuations in
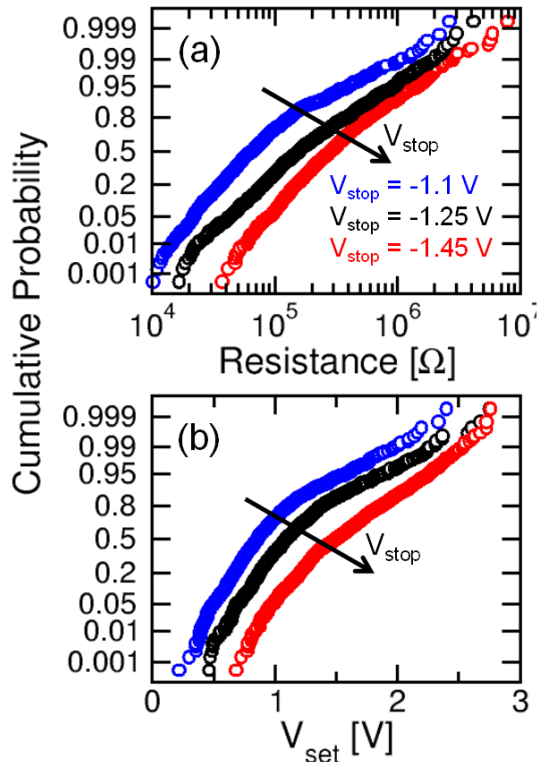
Fig. 4. Cumulative distributions of the HRS resistance measured at V_{read} = -0.6 V (a) and of V_{set} (b) at variable V_{stop}, namely V_{stop} = -1.1 V, -1.25 V and-1.45 V. As V_{stop} increases, both the resistance and V_{set} increase due to the increasing length of the depleted gap in the CF.
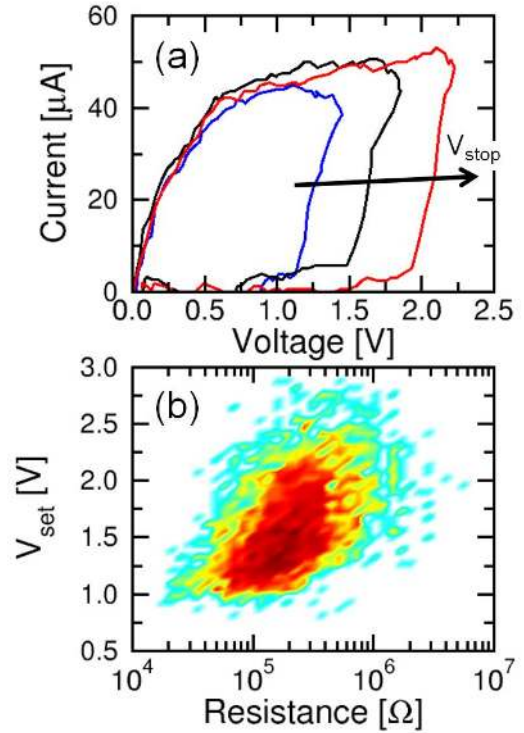

Fig. 5. Measured I-V curves showing the set transition at positive voltage for increasing V_{stop} in the preceding reset process (a) and scatter plot of a V_{set} as a function of HRS resistance collected over 5000 set/reset cycles (b).

the LRS are generally due to geometrical variations in the CF cross section, which affect LRS resistance only linearly [11,12].

Fig. 4 shows the cumulative distributions of HRS resistance measured at -0.6 V(a) and V_{set} (b) for variable V_{stop}, which was increased from -1.1 to -1.45 V. As V_{stop} increases, both R and V_{set} increase as a result of the increase of the length of the depleted gap. To further evidence the controllability of R and V_{set} of the HRS by V_{stop}, Fig. 5ashows the I-V curves for the set process after reset at increasing V_{stop}, using the same values of V_{stop} in Fig. 4. The increase of V_{set} with R in the HRS was explained by the increase of the voltage drop across the depleted gap, which in turn reduces the local temperature and field in the remaining CF regions[21]. Since temperature and field are the driving forces for ion migration, a larger V_{set} is needed to initiate the set process as the gap region increases. Irrespective of the value of V_{stop}, the large variability of the reset process results in relatively broad distributions of R and V_{set}. The slope of the cumulative distributions in the Fig.4slightly increases at increasing V_{stop}, as previously indicated by experiments and simulations of HfO$_x$-based RRAM [11]. This was explained by the increase of the migrated defects at increasing V_{stop}: as V_{stop} increases, more defect are displaced along the CF to open a high-resistance gap, which is responsible for the HRS resistance. Since the Poisson variability is dictated by the number of participating defects, a tighter distribution is obtained for a larger number of defects contributing to the reset process, hence at high V_{stop}

[11]. The evolution of the CF at increasing V_{stop} is reflected by both parameters R and V_{set}, which are strongly correlated as shown by the scatter plot in Fig. 5b [23].

IV. RNG METHODOLOGY

The stochastic set process can be used for true RNG as described in Fig. 6. As shown in Fig. 6a, a 4 pulse-sequence is applied to the 1T1R, including: (i) a set pulse to initialize the device in the LRS, (ii) a reset pulse with stop voltage V_{stop} to induce the transition to the HRS with a resistance distribution similar to Fig. 4a, (iii) a random set pulse with voltage V_A close to the median value of V_{set} in Fig. 4b, and (iv) a final read pulse to probe the resistance in the final state. Note, in fact, that V_A = 1.6 V, which is applied in Fig. 6for the random set pulse, corresponds to the median value of V_{set} distribution in Fig. 4b for V_{stop} = -1.45 V, thus aiming at inducing a set transition only in half of the device cycles. Fig. 6b shows the cumulative distribution of the resulting resistance measured by the read pulse in Fig. 6a: data show a bimodal distribution with 2 sub-distributions, namely an LRS sub-distribution with R of about 12 kΩ, and a HRS sub-distribution with a broad distribution of resistance above 100 kΩ. The bimodal distribution serves as a source of random bits for the true RNG. To avoid any memory effect where a RNG event might be correlated and influenced by the previous random state, the device is properly initialized through the initial set pulse which ensures a strong CF formation.
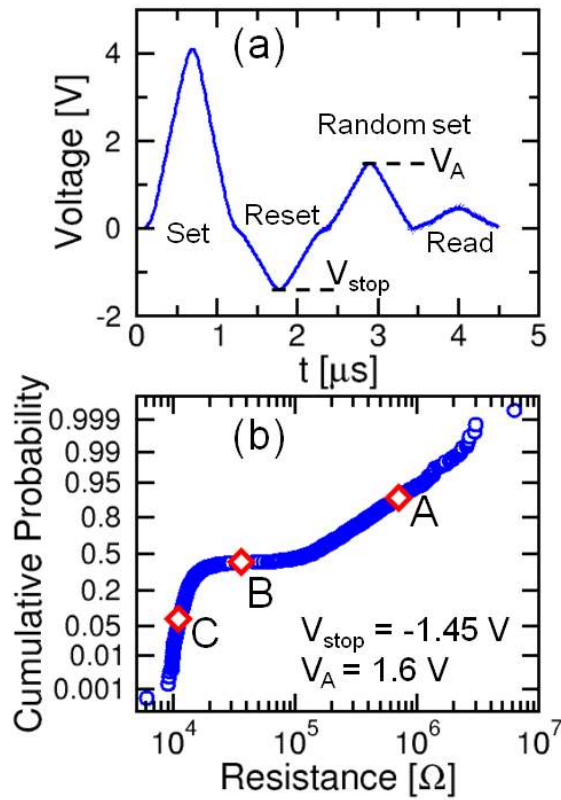
Fig. 6. Sequence of applied pulses for true RNG (a) and cumulative distribution of R obtained from 10^3 repeated RNG operations (b). The random set operations for points A, B and C highlighted in (b) are shown in Fig. 7.
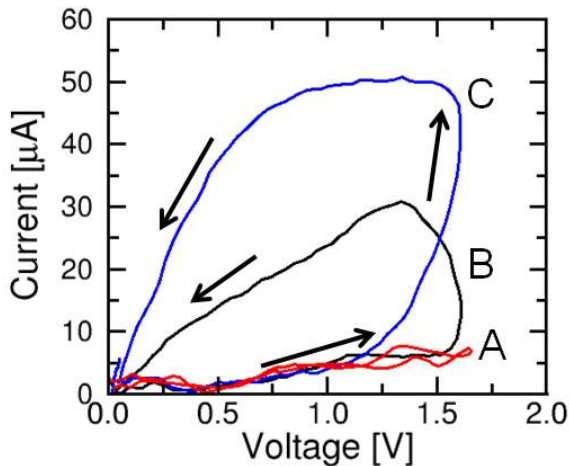

Fig. 7. Measured I-V curves during the random set process of the 1T1R corresponding to states A, B and C in the distribution of Fig. 6b.
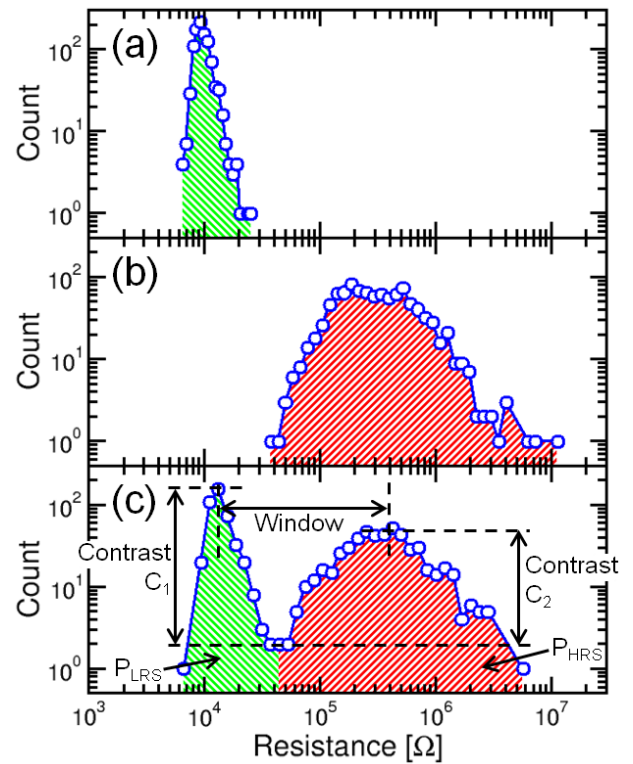

Fig. 8. Probability distribution of R measured after the set (first) pulse (a), reset (second) pulse (b)and the random set (third) pulse (c) in the sequence of Fig. 6a. The HRS and LRS sub-distributions (same data as in Fig. 6b) can be clearly seen in plot (c). The RNG figures of merit, including the sub-distribution probabilities, resistance window RW and contrasts C_1 and C_2, are defined in Fig. 8c.

To better understand the origin of the bimodal distribution, Fig. 7 shows the I-V curves for 3 random set operations, corresponding to state A, B and C in Fig. 6b. Since V_A is properly calibrated to be located at the median value of the broad V_{set} distribution, the set process takes place only for 50% of the cycles. Case A corresponds to a cycle where V_{set} was higher than V_A, as a result of reset in the previous pulse ending up in a relatively large R, hence large V_{set}. As a result, no set process takes place in this case, and R is found in the

HRS sub-distribution in Fig. 6b. On the other hand, V_{set} is smaller than V_A for case C, thus the device undergoes a set transition with the current being limited to I_C of about 50 µA thanks to the series transistor. State C is thus found in the LRS sub-distribution in Fig. 6b. Finally, an intermediate case B is also shown, corresponding to V_{set} being very close to the applied V_A: in this case, set transition takes place but only in the final stages of the triangular random-set pulse in Fig. 6a. As a result, set transition cannot be completed as in case C, and the device only reaches a resistance which is halfway between HRS and LRS. This provides the flat transition region of the bimodal distribution in Fig. 6b, between the HRS and the LRS sub-distributions. We found that the occurrence of intermediate cases of type B can be minimized by a proper shape of the random-set pulse (*e.g.*, saw-tooth shape with an abrupt drop of the voltage after the peak value V_A is reached) or by reducing the pulse width.

Fig. 8a and b show the probability distributions of R measured after the first (set) and the second (reset) pulse in Fig. 6a, while Fig. 8c shows the distribution of R measured after the random set pulse (same data as in Fig. 6b). Note that the LRS resistance distribution in Fig. 8ais extremely tight with an almost negligible relative standard deviation of 0.21, thus ensuring an optimum initialization of the RNG. The initial distribution (b) can be described by a relatively broad log-normal distribution, while the final distribution shows 2 well defined log-normal peaks, corresponding to the LRS and the HRS sub-distributions. The random LRS and HRS in the 2
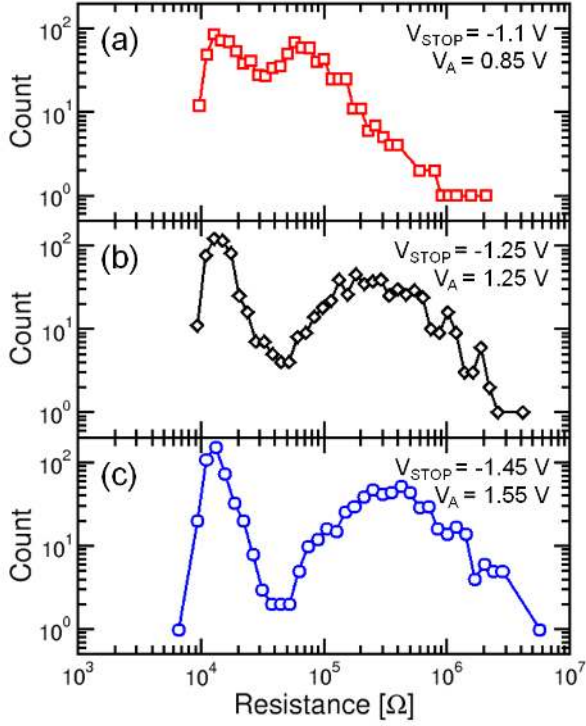
Fig. 9. Probability distributions of R measured after random set for increasing V_{stop}. The applied voltage V_A was chosen to obtain $P_{HRS} \approx P_{LRS} \approx 0.5$.
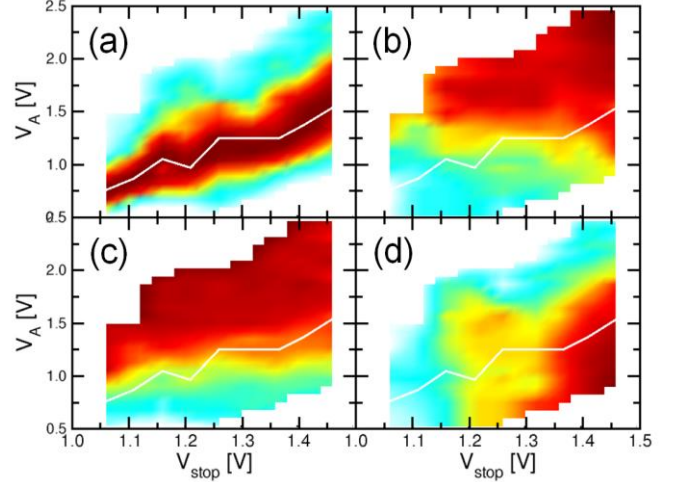

Fig. 10. Contour plot of the figure of merits, namely the probability to obtain $P_{HRS} = P_{LRS} = 0.5$, represented by $P_{50\%} = P_{HRS}P_{LRS}/0.25$ (a), the resistance window RW (b) and the contrast C_1 (c) and C_2 (d). The white line highlights the conditions to have a balanced RNG ($P_{HRS} = P_{LRS}$).

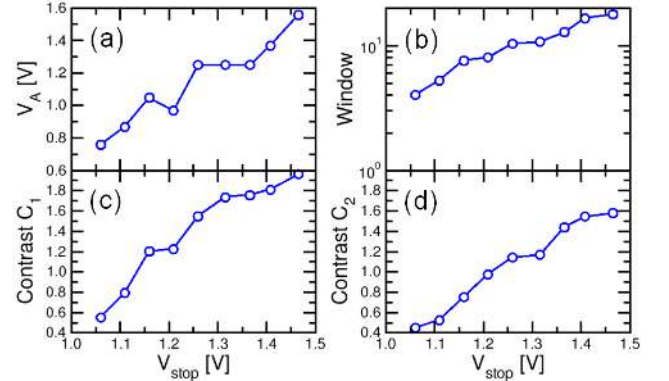
Fig. 11. Applied voltage V_A as function of V_{stop} to obtain a balanced RNG (a). Evolution of resistance window RW (b), contrast C_1 and C_2 for a balanced RNG.

sub-distributions serve as the 0 and 1 random bits of a true RNG.

For an optimized RNG, the resistance window between the 2 sub-distributions in Fig. 8c and the contrast between the peaks of the HRS and LRS sub-distributions and the intermediate region B should be as large as possible. To identify possible figures of merit for RNG optimization, Fig. 8c shows the definition of the resistance window RW, namely the ratio between the resistance at the peaks of the HRS and the LRS sub-distributions. The contrast C_1 is also defined as the ratio between the peak probability of LRS and the minimum probability in the transition region between LRS and HRS. Similarly, contrast C_2 is defined as the ratio between the peak probability of HRS sub-distribution and the minimum probability in the transition region. Finally, the total amount of HRS and LRS probabilities, namely P_{HRS} and P_{LRS} respectively, is also defined. Note that HRS and LRS probabilities satisfy the relationship $P_{HRS} + P_{LRS} = 1$.

V. RNG Optimization

To optimize the RNG process, the figures of merit in Fig. 8c can be maximized by an accurate choice of the parameters in the pulse sequence of Fig. 6a, namely the stop voltage V_{stop} and the applied voltage V_A for random set. To illustrate the impact of V_{stop} and V_A on the RNG distributions, Fig. 9 shows the probability distributions for increasing V_{stop}, namely $V_{stop} = -1.1$ V(a), $V_{stop} = -1.25$ V (b) and $V_{stop} = -1.45$ V (c). The applied voltage V_A in the figures was chosen to be close to the median distribution of V_{set}, for each value of V_{stop}, so as to satisfy the relationship $P_{HRS} \approx P_{LRS} \approx 0.5$.

Note that the LRS sub-distribution is generally peaked around 12 kΩ, since this results from the set process controlled by I_C. On the other hand, the HRS sub-distribution moves according to the value of V_{stop}, therefore the resistance window of RNG increases at increasing V_{stop}. Note that V_A also must increase with V_{stop} to ensure a 50% of random set, since V_{set} increases with V_{stop} (see Fig. 4b). Thanks to the increasing window between HRS and LRS, the contrast is also improved from (a) to (c) as V_{stop} increases. At relatively low V_{stop}, in fact, the HRS distribution has significant contribution in the intermediate range of R between the median LRS and median HRS, which thus results in a degradation of the contrast at low V_{stop} and low V_A.

To study the appropriate value of V_A to achieve the condition $P_{HRS} \approx P_{LRS} \approx 0.5$, Fig. 10a shows the contour plot of the product $P_{50\%} = P_{HRS}P_{LRS}/0.25$, which is maximum for $P_{HRS} \approx P_{LRS}$ and decreases as either P_{HRS} or P_{LRS} approach 0. The contour plot is shown as a function of V_{stop} and V_A in the x-axis and y-axis, respectively. The maximum $P_{50\%}$ is achieved along a curve where V_A increases with V_{stop}, as already expected from results in Fig. 9. Note that this curve corresponds to the
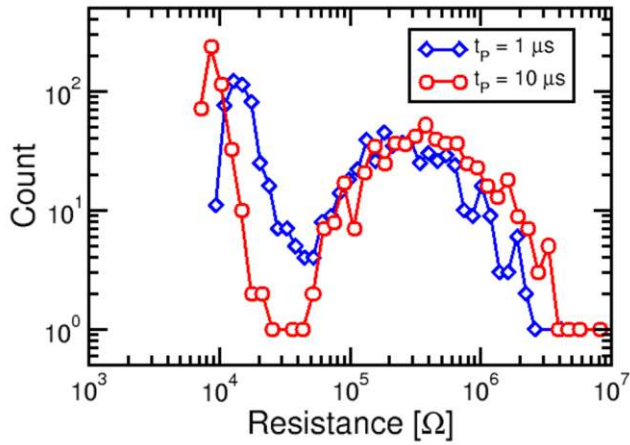
Fig. 12. Probability distribution of R measured after random set for increasing pulse-width t_P.

correlation between the median of V_{set} and V_{stop}, obtained from V_{set} distributions at variable V_{stop} as those shown in Fig. 4b. The curve of maximum $P_{50\%}$ defines the appropriate values of V_A for RNG at any given value of V_{stop}. This curve will thus be taken as a reference line for RNG optimization.

Fig. 10b shows the resistance window between the peaks of LRS and HRS sub-distributions as defined in Fig. 8c. The window increases with V_A, while is negligibly dependent on V_{stop}. In fact, while V_{stop} controls the initial resistance of the HRS (Fig. 8b), it is V_A that dictates the portion of HRS distribution that undergoes set transitions after the random set pulse. The larger V_A, the larger the amount of HRS that is converted into LRS sub-distribution. Since the random set operation selects HRS levels at relatively low resistance, increasing V_A results in an increase of the resistance of HRS sub-distribution, thus increasing the resistance window.

Fig. 10c and d show the contour plot of contrast C_1 and C_2, respectively. Contrast C_1 between the LRS sub-distribution peak and the inter-distribution valley is mainly controlled by V_A: in fact, as V_A increases, the window increases (Fig. 10b), thus increasing the depth of the valley between the sub-distributions. On the other hand, contrast C_2 between the valley and the HRS peak is controlled by both V_{stop} and V_A. This is because the initial HRS distribution shifts to higher resistance at increasing V_{stop}. Also, a large V_A reduces the amount of cells in the HRS sub-distributions, thus reducing its peak and the contrast C_2. Note that both contrasts C_1 and C_2 are key parameters to define the quality of the RNG. As the contrasts increase, the bimodal character of the resistance distribution becomes increasingly well defined, thus approaching an ideal RNG behavior.

The curve of balanced RNG ($P_{HRS} = P_{LRS}$) is shown in all contour plots in Fig. 10 and in Fig. 11a. From the intersection between the contour plots and the balanced RNG line, one can obtain the evolution of window, C_1 and C_2 with V_{stop}, as shown in Fig. 11b, c and d, respectively. In general, these results indicate that optimum bimodal distributions are obtained for large V_{stop}. This can be understood by the role of V_{stop} in increasing the resistance window between LRS and HRS. The large the initial HRS, the larger the window between HRS and LRS sub-distributions after random set. A
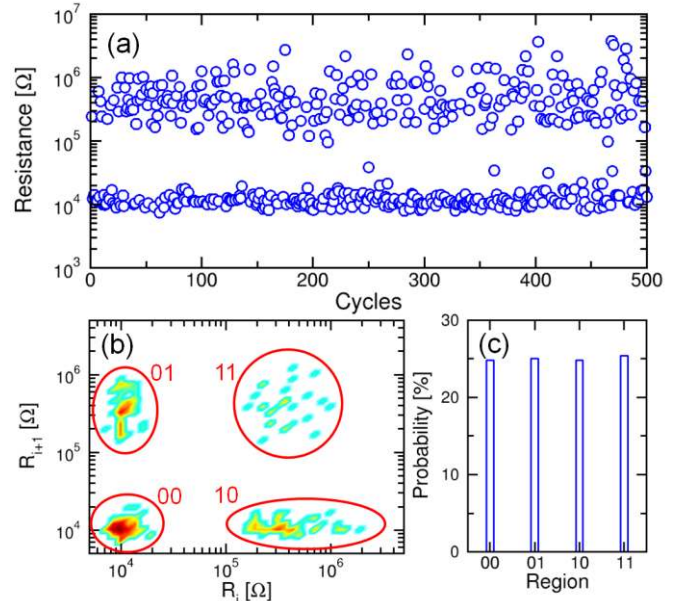

Fig. 13. Measured R after random set for 500 cycles for V_{stop} = -1.45 V and V_A = 1.6 V (a), correlation of R in cycle i+1 as a function of R in cycle i (b) and populations of the 4 regions (c) defined in b.

larger window also ensures a good contrast due to sufficiently low valley between the sub-distributions.

Results in Figs. 10 and 11 thus indicates that (i) the value of V_A to obtain $P_{HRS} = P_{LRS} = 50\%$ increases at increasing V_{stop}, and (ii) the window and contrast also increase at increasing V_{stop}. While RNG performance improves at increasing V_{stop}, the maximum V_{stop} for operating the RNG is dictated by reliability of the resistive switching device. In fact, endurance studies have indicated that a large V_{stop} increases the probability of a negative set, or breakdown, where resistance suddenly decreases during the reset under a negative voltage [23]. Since the select transistor is generally biased to high gate voltage during reset, the relatively high current limit leads to destructive set in the RRAM device. Therefore, for safe operation of the RNG circuit, the maximum value of V_{stop} should be accurately limited to avoid RRAM failure.

This RNG scheme can be further optimized in terms of time and power consumption. Fig. 6a shows that the complete sequence of set, reset, random set and read pulses to generate 1 random bit lasts about 4.5 μs. This time can be decreased by reducing the set/reset pulse-width, which was shown to be as short as below 1 ns in metal-oxide RRAM [24]. On the other hand, the resistance window and contrast can be improved by increasing the pulse widths in the random set operation. This is shown in Fig. 12, comparing the resistance distribution for pulse width t_P = 1 μs and 10 μs. the resistance window increases, since set and reset transitions become more efficient at increasing set/reset times. Also, the contrast between the two states increases, as the probability for partial set transition (case B in Fig. 7) decreases as the time increases.

To reduce the power consumption of the RNG, the peak current in set/reset processes, which is around 50 μA from Figs. 5 and 7, can also be reduced by decreasing the
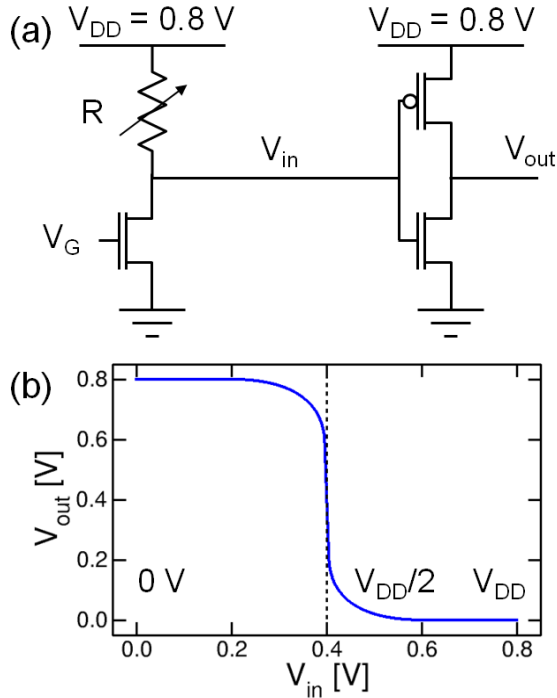
Fig. 14. Schematic of the regeneration circuit (a), including the 1T1R RRAM structure and a CMOS inverter and the V_{in}-V_{out} characteristic of the inverter (b).

compliance current during the set operation, *e.g.*, to below 10 µA [25].

VI. RNG RANDOMNESS

True random number generation requires that there is no memory effect in the physical process for bit generation. We demonstrated randomness of RNG in our RRAM circuit by verifying that there is no correlation between successive RRAM states in a sequence of generated bits. Fig. 13a shows the measured RRAM resistances in a sequence of 500 states. The sequence was obtained for $V_{stop} = -1.45V$ and $V_A = 1.6$ V, and shows a clear bimodal distribution of LRS (R ≈12 kΩ) and HRS (R ≈ 400 kΩ). Fig. 13b shows the correlation plot of R in cycle $i+1$ as a function of R in cycle i, where i ranges from 1 to 499. The correlation is shown as a contour plot of probabilities for having a given resistance R_{i+1} at cycle $i+1$ and resistance R_i at cycle i. From the correlation plot, four regions can be identified, depending on the RRAM resistance value in the 2 cycles. Region 00 corresponds to the cell consecutively showing LRS in both cycles, while region 11 identifies consecutive generation of HRS levels. Regions 01 and 10, instead, correspond to the cell changing sub-distribution from cycle i to cycle $i+1$. The populations of the four correlation regions is shown in the histogram of Fig. 13c: all regions indicate comparable values very close to 25%, demonstrating the lack of correlation between successive extractions and the true randomness of this RNG.

VII. REGENERATION CIRCUIT

Although relatively high values of contrast can be achieved in the bimodal distribution of HRS and LRS, a positive-feedback regeneration of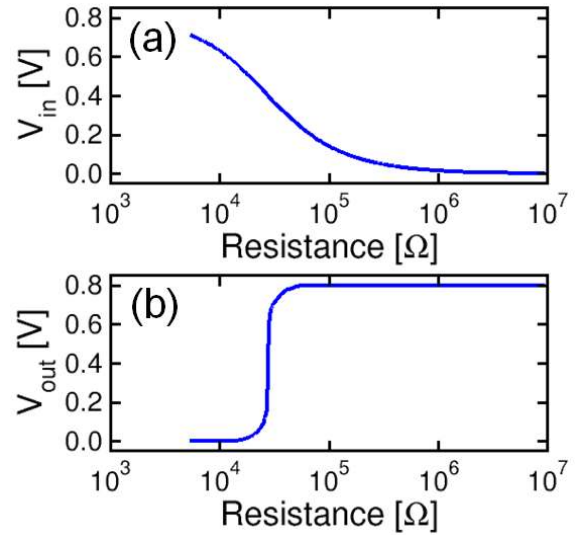 the analog values of resistance might be appropriate for an ideal RNG operation. To this purpose, Fig. 14a shows a regeneration circuit, where the first stage consists of the RNG based on the 1T1R structure, while the second stage is a CMOS inverter. Note that the relative large resistance window between set and reset allows to use a CMOS inverter rather than an analog comparator, which is instead needed for RTN-based RNG due to its smaller resistance window [3]. Fig. 14b shows the V_{in}-V_{out}

Fig. 15. Inverter voltages V_{in} (a) and V_{out} (b) as function of the RRAM resistance for $V_{DD} = 0.8$ V.
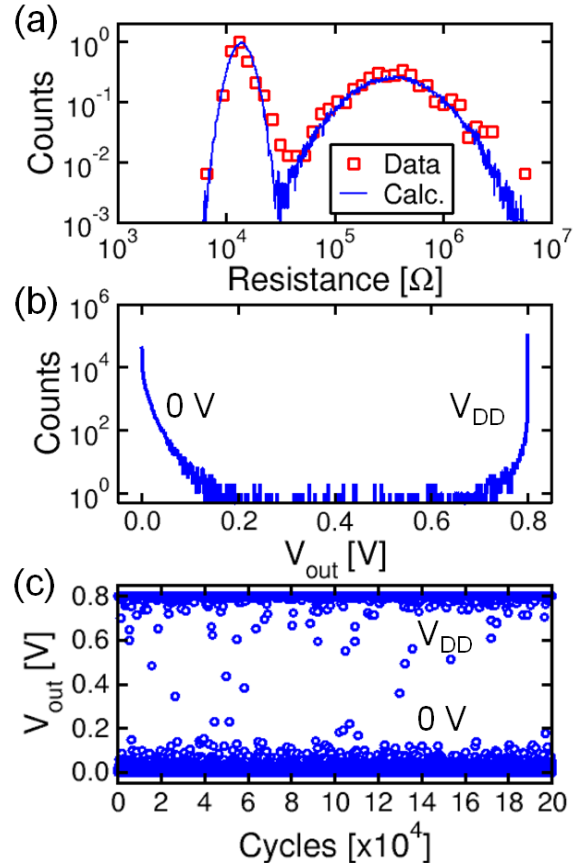

Fig. 16. Measured and simulated distribution of the RRAM resistance (a), simulated distribution of the inverter output V_{out} (b) and sequence of V_{out} for $2x10^5$ cycles.

characteristics of the CMOS inverter, displaying a threshold voltage at 0.4 V. The CMOS inverter was simulated assuming a MOSFET conductivity K = 80 μA/V^2, a threshold voltage $|V_T|$ = 0.2 V and an Early effect with λ = 0.25 V^{-1} with Multisim^{TM}. The first stage acts as a voltage divider circuit, where the analog voltage V_{in} is high or low for the RRAM resistance being low or high, respectively. The CMOS inverter allows for digital restoration through the high gain in the transition region in Fig. 14b. Fig. 15 shows the calculated V_{in} (a) and V_{out} (b) as a function of the RRAM resistance R, demonstrating analog and digital characteristics, respectively.

To further demonstrate the RNG regeneration, Fig. 16 shows simulation results of the circuit in Fig. 14a. First, we randomly generated resistance values according to the bimodal distribution shown in Fig. 16a, which is in good agreement with the experimental results. For each value of resistance, we calculated the output voltage of the regeneration circuit, resulting in the digital bimodal distribution of V_{out} in Fig. 16b. Note the very small number of counts in the intermediate region, corresponding to resistance values in the valley between the HRS and LRS sub-distributions. the number of intermediate values around V_{DD}/2 can be further suppressed by adding a third stage for digital restoration, *e.g.*, another CMOS inverter. Fig. 16c shows the sequence of V_{out}, again supporting digital RNG.

VIII. CONCLUSIONS

We presented a new RNG concepts based on switching variability in RRAM. The RNG operation relies on random set where the RRAM is driven by an applied voltage V_A very close to the median of the distribution of V_{set}. The resistance value after random set displays bimodal distribution with HRS and LRS sub-distributions. Careful adjustment of V_A allows for fine balancing of the sub-distributions, as well as for optimized window and contrast. Randomness is demonstrated by a correlation study of successive RNG cycles. Finally, a regeneration circuit is proposed to allow for ideal digital RNG.

REFERENCES

[1] G Taylor and G. Cox, "Digital Randomness," IEEE Spectrum 48, 32 (2011).

[2] R. Brederlow, R. Prakash, C. Paulus, R. Thewes, "A Low-Power True Random Number Generator using Random Telegraph Noise of Single Oxide-Traps," ISSCC Tech. Dig. 1666 (2006).

[3] C.-Y. Huang, W. C. Shen, Y.-H. Tseng, Y.-C. King, and C.-J. Lin, "A Contact-Resistive Random-Access-Memory-Based True Random Number Generator," IEEE Electron Device Lett. 33, 1108 (2012).

[4] A. Fukushima, T. Seki, K. Yakushiji, H. Kubota, H. Imamura, S. Yuasa and K. Ando, "Spin dice: A scalable truly random number generator based on spintronics," Appl. Phys. Express 7, 083001 (2014).

[5] S. Gaba, P. Sheridan, J. Zhou, S. Choi and W. Lu, "Stochastic memristive devices for computing and neuromorphic applications," Nanoscale 5, 5872-5878 (2013).

[6] S.Gaba, P. Knag, Z. Zhang, W. Lu, "Memristive Devices for Stochastic Computing," Proc. IEEE ISCAS 2592-2595 (2014).

[7] D. Ielmini, F. Nardi and C. Cagli, "Resistance-dependent amplitude of random telegraph signal noise in resistive switching memories," Appl. Phys. Lett. 96, 053503 (2010).

[8] D. Veksler, G. Bersuker, B. Chakrabarti, E. Vogel, S. Deora, K. Matthews, D. C. Gilmer, H.-F. Li, S. Gausepohl, P. D. Kirsch, "Methodology for the statistical evaluation of the effect of random telegraph noise (RTN) on RRAM characteristics," IEDM Tech. Dig. 219 (2012).

[9] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical fluctuations in HfO$_x$ resistive-switching memory (RRAM): Part II – Random telegraph noise," IEEE Trans. Electron Devices 61, 2920-2927 (2014).

[10] S. Ambrogio, S. Balatti, V. McCaffrey, D. Wang and D. Ielmini, "Impact of low-frequency noise on read distributions of resistive switching memory (RRAM)," IEDM Tech. Dig. Paper 14.4 (2014).

[11] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical fluctuations in HfO$_x$ resistive-switching memory (RRAM): Part I – Set/Reset variability," IEEE Trans. Electron Devices 61, 2912-2919 (2014).

[12] S. Balatti, S. Ambrogio, D. C. Gilmer, and D. Ielmini, "Set variability and failure induced by complementary switching in bipolar RRAM," IEEE Electron Device Lett. 34, 861-863 (2013).

[13] X. Guan, S. Yu, and H.-S. P. Wong, "On the switching parameter variation of metal-oxide RRAM—Part I: Physical modeling and simulation methodology," IEEE Trans. Electron Devices, vol. 59, no. 4, pp. 1172–1182, Apr. 2012.

[14] A. Fantini, D. J. Wouters, R. Degraeve, L. Goux, L. Pantisano, G. Kar, Y.-Y. Chen, B. Govoreanu, J. A. Kittl, L. Altimime, and M. Jurczak, "Intrinsic switching behavior in HfO$_2$ RRAM by fast electrical measurements on novel 2R test structures," in Proc. IEEE-Int. Memory Workshop, May 2012, pp. 1–4.

[15] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang and H.-S. P. Wong, "Stochastic learning in oxide binary synaptic device for neuromorphic computing," Front. Neurosci. 7:186 (2015).

[16] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng,C. H. Lin, F. Chen, C. H. Lien, and M.-J. Tsai, "Low power and high speedbipolar switching with a thin reactive Ti buffer layer in robust HfO2 based RRAM," in IEDM Tech. Dig. 297–300 (2008).

[17] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki,and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiO$_x$ brought about by reducing a parasitic capacitance," Appl. Phys. Lett. 93, 033506(2008).

[18] H.-S. Philip Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal–Oxide RRAM," Proc. IEEE 100, 1951 (2012).

[19] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," IEEE Trans. Electron Devices 58, 4309-4317 (2011).

[20] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM – Part I: Experimental study," IEEE Trans. Electron Devices 59, 2461–2467 (2012).

[21] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM – Part II: Modeling," IEEE Trans. Electron Devices 59, 2468–2475 (2012).

[22] D. Ielmini, C. Cagli and F. Nardi, "Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories," Nanotechnology 22, 254022 (2011).

[23] S. Balatti, S. Ambrogio, Z.-Q. Wang, A. Calderoni, N. Ramaswamy and D. Ielmini, "Pulsed cycling operation and endurance failure of metal-oxide resistive RAM," IEDM Tech. Dig. 359-362 (2014).

[24] M. D. Pickett and R. S. Williams, "Sub-100 fJ and sub-nano second thermally driven threshold switching in niobium oxide cross-point nanodevices," Nanotechnology, vol. 23, p. 215202 (2012).

[25] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, D. J. Wouters, "Control of filament size and reduction of reset current below 10 μA in NiO resistance switching memories," Solid State Electronics 58, 42-47 (2011).