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Tunnel FET Analog Benchmarking and Circuit Design

HAO LU[1], PAOLO PALETTI[1], WENJUN LI[1], PATRICK FAY[1] (Fellow, IEEE), TROND YTTERDAL[2] (Senior Member, IEEE), AND ALAN SEABAUGH[1] (Fellow, IEEE)

[1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA
[2]Department of Electronic Systems, Norwegian University of Science and Technology, 7491 Trondheim, Norway

CORRESPONDING AUTHOR: T. YTTERDAL (trond.ytterdal@ntnu.no).

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ABSTRACT A platform for benchmarking tunnel field-effect transistors (TFETs) for analog applications is presented and used to compare selected TFETs to FinFET technology at the 14-nm node. This benchmarking is enabled by the development of a universal TFET SPICE model and a parameter extraction procedure based on data from physics-based device simulators. Analog figures of merit are computed versus current density to compare TFETs with CMOS for low-power analog applications to reveal promising directions for the system development. To illustrate the design space enabled by TFETs featuring sub-60-mV/decade subthreshold swing, two example circuits including a picopower common-source amplifier and an ultralow-voltage ring oscillator are demonstrated.

INDEX TERMS Analog circuit, benchmarking, compact model, steep subthreshold swing (SS), tunnel field-effect transistor (TFET), ultralow-voltage circuit.

I. INTRODUCTION

Benchmarking of emerging devices for digital applications has shown the tunnel field-effect transistor (TFET) to be one of the leading options for low power beyond-CMOS transistors [1]–[3]. Unlike conventional MOSFETs where the subthreshold current-governing mechanism is thermionic emission above a potential barrier, resulting in the well-known 60-mV/decade subthreshold swing (SS) limit at room temperature, TFETs rely on band-to-band tunneling (BTBT) through a potential barrier [4], [5]. By a combination of gate modulation of the tunneling barrier thickness and density-of-state switching of available states to tunnel into, SS steeper than 60 mV/decade can be achieved, leading to significant reduction of supply voltage operations at the device level and substantial benefits in energy savings from a system-level perspective [2].

A plethora of different device concepts and material systems have been intensively investigated by means of either technology computer-aided design (TCAD) or full quantum simulation studies, gauging TFETs' performance against state-of-the-art CMOS technologies and highlighting TFETs' superior capabilities. Nevertheless, experimental demonstrations have generally lagged the expectations, struggling to achieve simultaneously sub-60-mV/decade SS and 1–10-μA/μm ON-current levels (see [6] for an extensive but by no means exhaustive list and comparison between the proposed and experimentally demonstrated TFETs). However, this trend has been recently reversed [7]: III–V vertical heterojunction nanowire TFETs integrated on Si substrates have been experimentally demonstrated with $SS_{min} = 48$ mV/decade, $I_{60} = 0.31$ μA/μm, and $I_{ON} > 10$ μA/μm, indicating that III–V technologies have reached the necessary level of sophistication in terms of, e.g., material growth, tunneling junction abruptness, and low trap density at the high-k/semiconductor interface, required for such a challenging device. This has validated the potential of this class of steep-slope devices for low-power logic purposes, and analog applications are being explored too [8]–[10].

While benchmarking of steep devices for digital applications has advanced, analog benchmarking has received less attention. Sedighi *et al.* [9] provided a systematic comparison between CMOS and an InAs homojunction TFET and a GaSb-InAs heterojunction TFET (HTFET) by comparing dc characteristics such as subthreshold slope SS, OFF current I_{OFF}, threshold voltage V_{TH}, transconductance g_m, output conductance g_{ds}, intrinsic gain g_m/g_{ds}, cutoff frequency f_T, and equivalent ON-resistance R_{ON}. Analog circuit building blocks were examined, such as operational transconductance

amplifiers, current mirrors, and track-and-hold circuits, to explore how TFETs can enhance the performance or change the topology of the analog circuits. Track-and-hold circuits as well as comparators were also explored by Settino *et al.* [10] employing an InAs/AlGaSb nanowire HTFET virtual technology taking into account the nonsymmetrical behavior between n- and p-type devices.

Asbeck *et al.* [8] focused on the performance boost that TFETs can provide in the realm of low-power microwave and millimeter-wave circuits. (A GaSb/InAs HTFET was chosen as the representative device for this paper.) Due to the TFETs' higher nonlinearity and greater values of g_m at low drain current biases (relative to Si and III–V MOSFETs), it is shown that key building blocks such as rectifiers, detectors, mixers, low-noise amplifiers, and oscillators can benefit substantially from the simple replacement of CMOS transistors with steep-slope devices in conventional circuits [8]. In addition, circuit design centered around the unique characteristics of TFETs may lead to further improvements and optimizations, opening new avenues for extreme low-power systems that are out-of-reach for conventional CMOS technologies.

In this paper, a platform for benchmarking TFETs for analog applications is presented that enables exploration of the design space for TFETs versus FinFET technology at the 14-nm node. This benchmarking is enabled by the development of a universal charge conserving TFET SPICE model, which is used to model device characteristics obtained from the physics-based device simulators [11]–[13]. Both InAs- and GaN-based TFET models are used in this paper to represent the capabilities of future TFET technologies.

In Section II, analog figures of merit (FOMs) are computed versus current density to compare TFETs with CMOS for low-power analog applications and to reveal promising future directions for circuit and system development. In Section III, the design of two common circuit building blocks, including a picopower common-source amplifier and an ultralow-voltage ring oscillator, is explored. Applications of these circuit building blocks include ultralow-power operational amplifiers and receivers, low-power rectifiers for energy scavenging, and microwave/millimeter-wave detectors by taking advantage of the unique and distinct attributes of TFETs.

II. ANALOG BENCHMARKING

A. BENCHMARKED TECHNOLOGIES AND DEVICE MODELS

A commercially available 14-nm n-FinFET (gate length $L_G = 20$ nm) [14] is benchmarked against comparable 14-nm node InAs- [15] and GaN-based TFETs [16] with gate lengths of 20 nm. Two TFET material systems are selected to give a range of projected characteristics in the comparisons. The first is an InAs double-gate (DG) n-TFET with a homojunction p-i-n structure as has been previously considered [15], [17]. The narrow bandgap of InAs leads to ambipolar transfer characteristics with strong electron and hole branches. The second system is the GaN/InN/GaN DG n-TFET, which utilizes a heterojunction source and drain with tunneling through the narrow gap InN. The large GaN bandgap almost completely suppresses the ambipolar current. The GaN/InN/GaN TFET provides a current drive comparable to the InAs TFET and a much larger I_{ON}/I_{OFF} ratio. The steeper subthreshold slope of GaN/InN/GaN TFET allows the threshold voltage to be reduced to well below 0.1 V, which enables a lower supply voltage.

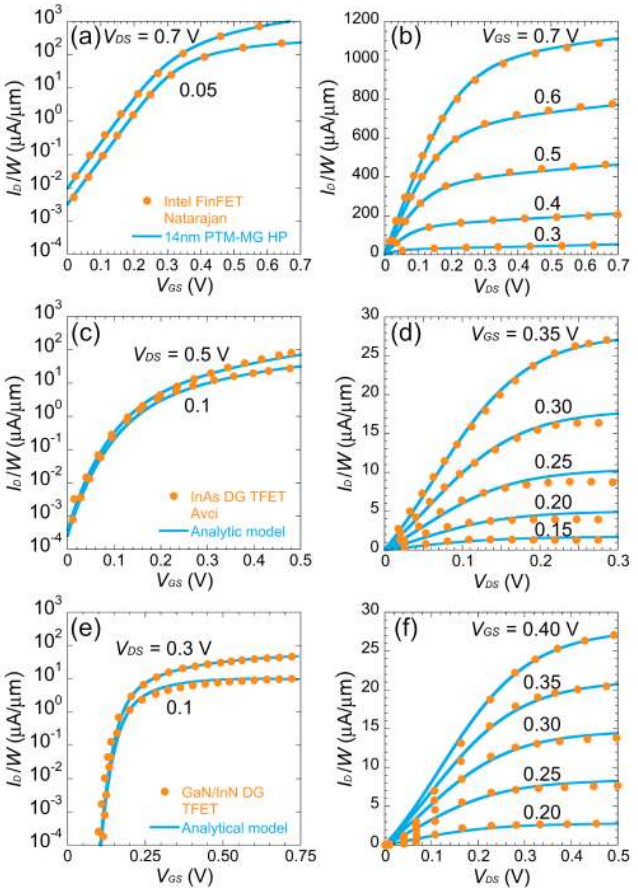

FIGURE 1. Transfer and output characteristics of the benchmarked technologies. Published [14] and simulated (a) transfer and (b) output characteristics of the 14-nm FinFET technology. The SPICE model, 14-nm PTM-MG HP [18], is calibrated against data in [14]. (c) Transfer and (d) output characteristics of 14-nm InAs DG TFET from Avci *et al.* [15] modeled in [11]. TCAD simulated and modeled (e) transfer and (f) output characteristics of sidewall DG GaN/InN/GaN TFET from simulations by Li *et al.* [16].

The 14-nm FinFET model is obtained by calibrating the 14-nm high-performance multigate predictive technology model (PTM-MG HP) [18] to data published in [14]. The resulting transfer and output characteristics are shown in Fig. 1(a) and (b). In short, the CMOS technology is modeled using the PTM SPICE model calibrated to measurements, while, on the other hand, the TFETs are modeled using TFET SPICE models [11]–[13], [19]–[21] calibrated to physics-based simulations.

The TFET model captures the unique features of TFETs including gate-bias-dependent SS and superlinear current onset. The model is widely applicable across materials systems and device geometries and includes all four quadrants of the current–voltage characteristics including the ambipolar current and the negative differential resistance of the source Esaki tunnel junction.

The model includes gate tunneling current and a continuous model for the stored charge in the channel, from which the capacitances are derived. Finally, a noise model is now also a part of the description [13]. The complete model is coded in Verilog-A and used to model both the InAs p-i-n TFET used by Avci *et al.* [15] and the p-GaN/InN/n-GaN from Li *et al.* [16]. The transfer and output characteristics for these DG TFETs are shown in Fig. 1(c)–(f).

The model and the simulation results are generally in good agreement, as shown in Fig. 1. In the case of the InAs TFET, the equation set is able to reproduce effectively the superlinear current onset at low V_{DS} [see Fig. 1(d)] with just slight overestimation of the saturation current for intermediate V_{GS}. For the GaN TFET, the saturation current region is well represented, but the model is not fully representative at low V_{DS}. For this reason, in the design of the ultralow-voltage ring oscillator of Section III-B biased at V_{DS} below 10 mV, the parameter set is revised to improve the fit at low V_{DS}.

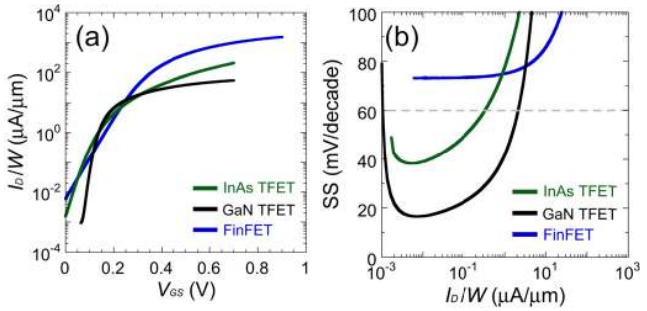

FIGURE 2. Comparisons of (a) drain current density I_D/W and (b) SS of FinFET, InAs TFET, and GaN/InN/GaN TFET. A drain–source voltage of 0.35 V was used for all calculations.

Fig. 2 shows the comparison of the transfer characteristics and SS of the FinFET to the TFETs at $V_{DS} = V_{DD}/2$ ($V_{DD} = 0.7$ V) because often in analog circuits, at least one p-type and one n-type transistors are stacked between the supply rails. Compared to the FinFET, the TFETs exhibit smaller SS, but also smaller I_{ON}. The GaN TFET shows SS $<$ 60 mV/decade up to 2 μA/μm, one decade higher than the InAs TFET. SS is a strong function of the gate-to-source bias for TFETs: SS_{min} reads ~16 and 38 mV/decade for the GaN and InAs TFETs, respectively, at current densities on the order of 6 nA/μm. At lower current densities, parasitic current paths, i.e., gate-leakage currents controlled by the gate-to-drain voltage V_{GD}, produce a degradation of SS, which is a function of the device structure and geometry [13]. At larger current densities, I_D/W is dominated by the source-to-channel tunneling current and therefore controlled by the interplay of the gate dependence on the tunneling window and the maximum electric field at the junction [12]. On the other hand, SS for FinFETs remains roughly constant for the entire subthreshold regime. This has a significant impact for analog design purposes as it will become clear in Section III.

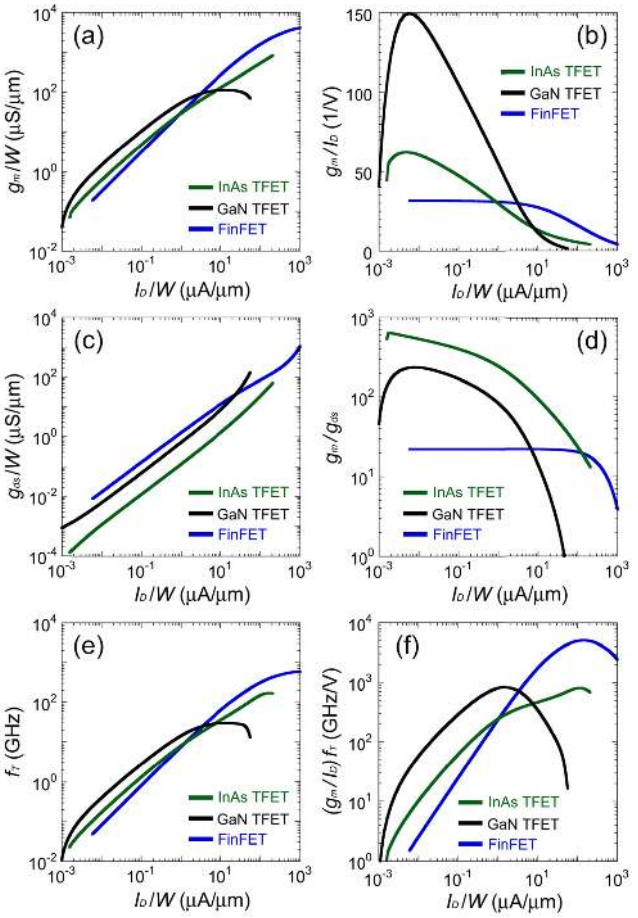

FIGURE 3. Comparisons of analog FOMs (a) g_m/W, (b) g_m/I_D, (c) g_{ds}/W, (d) g_m/g_{ds}, (e) f_T, and (f) $(g_m/I_D)f_T$ for FinFET, InAs, and GaN/InN TFETs. A drain–source voltage of 0.35 V was used for all calculations.

B. ANALOG FIGURES OF MERIT

In Fig. 3, the three technologies are compared in terms of important analog FOMs including g_m/W, g_m/I_D, g_{ds}/W, g_m/g_{ds}, f_T, and $(g_m/I_D)f_T$. The cutoff frequency f_T is approximated using $f_T = g_m/[2\pi(C_{GS}+C_{GD})]$ [8]. A $V_{DS} = 0.35$ V is used for all the calculations unless otherwise stated.

Fig. 3(a) shows the benefit of higher values of transconductance per unit width (g_m/W) for TFETs with respect to FinFETs in the entire subthreshold regime and up to μA/μm drain current density levels. The transconductance generation efficiency (g_m/I_D) is plotted in Fig. 3(b). In the subthreshold region, g_m/I_D can be formulated in terms of SS as in [8] and [22]

$$\frac{g_m}{I_D} = \frac{\ln(10)}{\mathrm{SS}}. \tag{1}$$

For a conventional MOSFET, the turn-ON mechanism is thermionic emission and, consequently, SS $>$ 60 mV/decade at room temperature, which translates into a g_m/I_D $<$ 38.5 V^{-1}. On the other hand, the BTBT of cold carriers in a TFET does not suffer the same limitations imposed by the Boltzmann tyranny. As a result, much larger transconductance efficiency values are predicted, as high as 150 V^{-1} for the GaN TFET, representing a 4$\times$ improvement against CMOS at drain current densities in the range of 10 nA/μm. The TFET exhibits a strong bias dependence of the g_m/I_D ratio (as a function of both V_{GS} and V_{DS}) in comparison to CMOS and this strong bias dependence introduces nonlinearity. The g_m/I_D peaks in the subthreshold region and remains larger than CMOS for current densities up to $\sim$1–10 μA/μm, as shown in Fig. 3(b).

For analog applications, the output conductance g_{ds} [see Fig. 3(c)] is of paramount importance, since it contributes directly to the intrinsic small-signal voltage gain g_m/g_{ds}, as shown in Fig. 3(d). Owing to TFETs' superior immunity to short-channel effects (i.e., the drain voltage has little impact on the tunnel junction potential at the source side), g_{ds}/W is found to be significantly smaller with respect to the MOSFET—a 10$\times$ decrease for the InAs TFET—over a wide range of drain current densities. The combined effect of a larger g_m in the subthreshold regime due to low SS and a smaller g_{ds} for TFETs compared to FinFETs translates into a substantial increase in the g_m/g_{ds} ratio, up to 10$\times$ and 30$\times$ at its peak for the GaN and InAs TFETs, respectively [see Fig. 3(d)]. For the FinFET in the subthreshold regime, g_m/I_D $\sim$ 31.4 V^{-1} and g_{ds}/I_D $\sim$ 1.4 V^{-1}, therefore the intrinsic small-signal voltage gain $g_m/g_{ds} \approx 22.4$ and roughly constant for over four decades and starts to roll-off only for current densities $>$100 μA/μm.

The simulated values of f_T [see Fig. 3(e)] indicate an advantage for TFETs over FinFETs as a direct results of higher g_m and moderately small C_{GS} and C_{GD} capacitances [13]. The product of the transconductance efficiency and the cutoff frequency $(g_m/I_D)f_T$ is reported in Fig. 3(f) as an additional FOM for comparing the three technologies. This FOM stems from a tradeoff between dc and high-frequency performance frequently encountered in analog circuit design [23], and in the whole subthreshold region, for current densities below $\sim$1 μA/μm, TFETs are predicted to exceed CMOS's performance thanks to their larger g_m.

Summarizing Fig. 3, it is observed that TFETs outperform the FinFET for all the FOMs considered in the subthreshold and near-threshold regions, while at higher current densities, CMOS's performance is superior. This motivates the exploration of TFETs for ultralow-power analog applications.

For analog circuits, the noise properties of the devices are very important. Since the drain current in TFETs is controlled by tunneling, the white drain current noise is shot noise with a noise current spectral density of $I^2_{n,D} = 2qI_D$ A^2/Hz. Fig. 4 shows the transistor input-referred noise voltages $V_{n,in}$ of the three different technologies versus drain current density, where also for the FinFET case, only white noise was

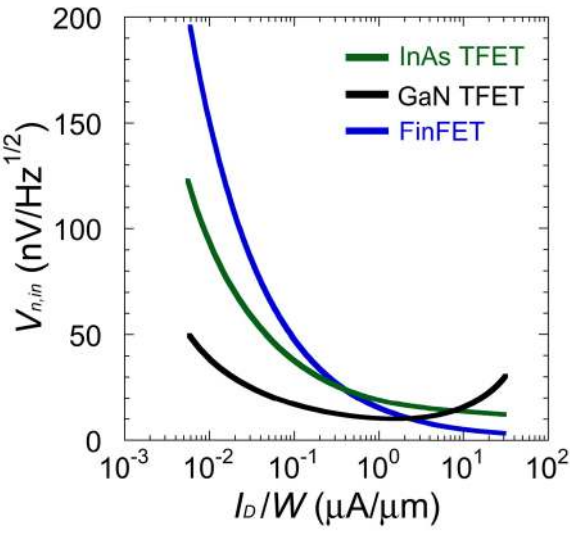

FIGURE 4. Comparisons of input-referred noise $V_{n,in}$ of 14-nm FinFET, InAs, and GaN/InN TFET. The gate width was 1 μm for all devices, and V_{DS} = 0.35 V.

accounted for in the comparison, i.e., flicker noise was not considered in this benchmarking. (A fixed gate width of $W = 1$ μm and $V_{DS} = 0.35$ V was set for all devices.) Proceeding in this manner, $V^2_{n,in}$ for the TFET reads $2qI_D/g^2_m$ and similarly for the FinFET in which case the noise current spectral density $I^2_{n,D}$ is determined by the interplay of shot noise in the subthreshold regime and thermal noise above threshold. Thus, the larger g_m of the FET over the FinFET in the subthreshold regime is reflected in better noise performance for a given drain current density, resulting in a 4$\times$ reduction of $V_{n,in}$ in deep subthreshold and superior capabilities up to approximately 2-μA/μm current density levels for the GaN TFET with respect to the FinFET. These advantages allow further reduction of power supply voltage and open up a design space for TFETs in low-power and low-voltage analog circuit design that is beyond the reach of CMOS.

III. EXAMPLE TFET CIRCUIT DESIGN

A. PICOPOWER COMMON-SOURCE AMPLIFIER

As a key building block of ultralow-power analog circuits, a common-source amplifier is designed in the three benchmarked technologies for a target unity-gain frequency of 10 MHz. The circuit, shown in Fig. 5, consists of one n-channel transistor M_1 and one p-channel transistor M_2 which acts as a load. The supply voltage is set at $V_{DD} = 0.7$ V, under the absolute maximum V_{DD} for the FinFET technology of 0.8 V; the load capacitances $C_L = 0.5$ fF. The g_m/I_D method has been employed as per standard subthreshold CMOS circuit design guidelines (see [24] for a thorough illustration of the method as applied to TFETs).

The key results are summarized in Table 1. The TFETs' strength over CMOS is the capability to operate in the subthreshold regime with larger g_m/I_D ratio, which translates into increased low-frequency gain (A_0), up to almost

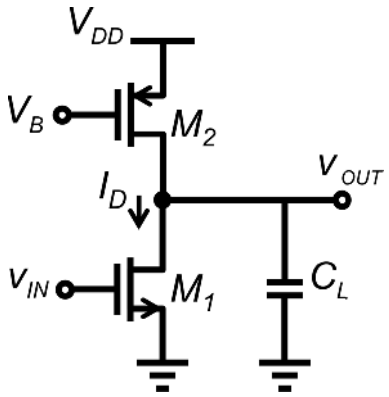

FIGURE 5. **Circuit schematic of a common-source amplifier with active load.**

TABLE 1. **Performance metrics.**

Performance	FinFET	InAs TFET	GaN TFET
I_D (pA)	1071	703	238
P (pW)	750	492	167
W (nm)	46	326	27
A_0 (dB)	20.9	49.6	40.8
f_{UG} (MHz)	10	10	10.2
$V_{n,in}$ (μV/Hz$^{1/2}$)	7.2	0.54	0.38
$f_{UG}A_0/P$	0.15	6.16	6.76
$f_{UG}A_0/(V_{n,in}P)$	0.0205	11.5	18

30× higher than FinFETs, together with a power consumption (P) of less than 200 pW at the same $V_{\rm DD}$ (compared to over 1 nW for the CMOS version). The FinFET-based circuit exhibits a higher input-referred noise performance ($V_{n,\rm in}$). The most significant features are condensed into two circuit FOMs that are based on device analog FOMs discussed in Section II. The first circuit FOM is defined as $f_{\rm UG}A_0/P$ and is related to device FOMs as follows:

$$\text{FOM} = \frac{f_{\rm UG}A_0}{P} \approx \frac{g_m}{2\pi C_L}\frac{g_m}{2g_{\rm ds}}\frac{1}{V_{\rm DD}I_D} = K\frac{g_m}{I_D}\frac{g_m}{g_{\rm ds}}. \quad (2)$$

The second circuit FOM takes into account the noise performance of the devices by also dividing by the input-referred noise voltage, which results in $f_{\rm UG}A_0/(V_{n,\rm in}P)$. The FOMs are predicting a substantial increase of performance with TFETs against CMOS FinFETs for ultralow-power applications.

B. ULTRALOW-VOLTAGE RING OSCILLATOR

It has been observed from TCAD simulations of GaN TFET structures that the superlinear current onset at low drain–source voltages of TFETs enables intrinsic gain larger than one for very low drain–source voltages when the threshold voltage is close to zero. Thus, operation in the superlinear region enables TFET circuits to operate with gain at ultralow supply voltages. In Fig. 6, the intrinsic gain of different devices is plotted versus $V_{\rm DS}$ for $V_{\rm GS}$ close to zero. As can be observed from the plot, the TFET intrinsic gain is larger than one even at a drain–source voltage of only 4 mV. Thus, this technology has a potential for supporting circuits powered at voltages below 10 mV.

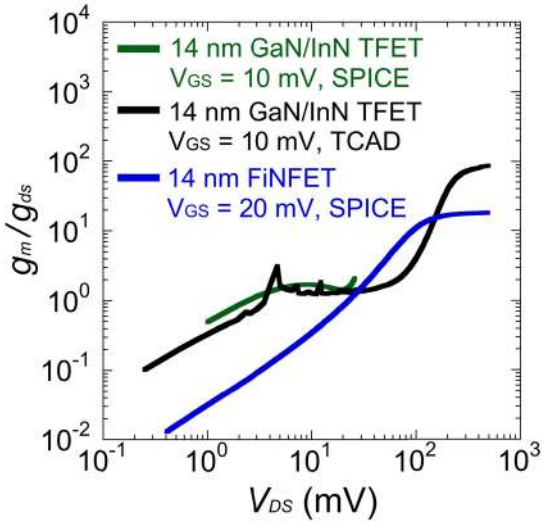

FIGURE 6. **Intrinsic gain of the benchmarking devices versus $V_{\rm DS}$ at ultralow $V_{\rm GS}$. The TFET data in black were obtained from TCAD simulations. The noise in the black line is due to numerical differentiation to obtain g_m and $g_{\rm ds}$.**

To illustrate this potential, a new model parameter set was extracted based on TCAD simulations at ultralow voltages, from 0 to 30 mV (green curve in Fig. 6), and a nine-stage ring oscillator was designed for a supply voltage of 8 mV and simulated in the Spectre simulator from Cadence [25] using the Verilog-A implementation of the model with the new model parameter set. Each stage of the ring oscillator consists of a standard inverter utilizing one n-TFET and one p-TFET, as shown in Fig. 7(a). Fig. 7(b) shows the simulated transfer curve of the inverter at $V_{\rm DD} = 8$ mV. Also included is the magnitude of the gain of the inverter ($|dV_{\rm out}/dV_{\rm in}|$) versus the input voltage which shows that the maximum magnitude of the gain is larger than 1.

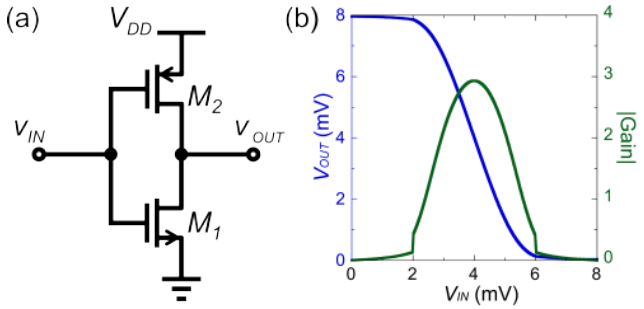

FIGURE 7. **(a) TFET inverter used in the ring oscillator. The gate width is 100 nm for both transistors. (b) TFET inverter transfer curve (blue) and the magnitude of the gain (green) at $V_{\rm DD} = 8$ mV.**

The simulated output waveform of the ring oscillator is shown in Fig. 8. The oscillation frequency was 6.7 kHz, and

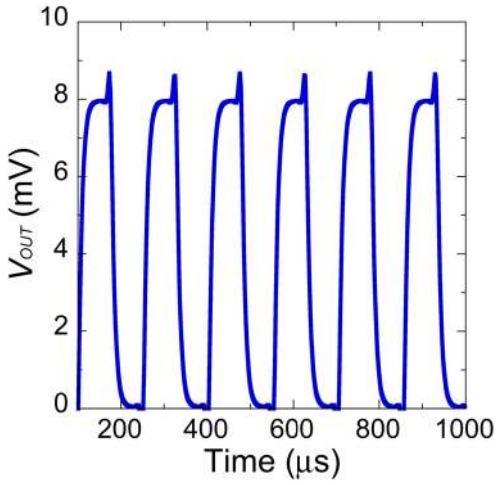

FIGURE 8. Output waveform of a nine-stage ring oscillator running at supply voltage of only 8 mV.

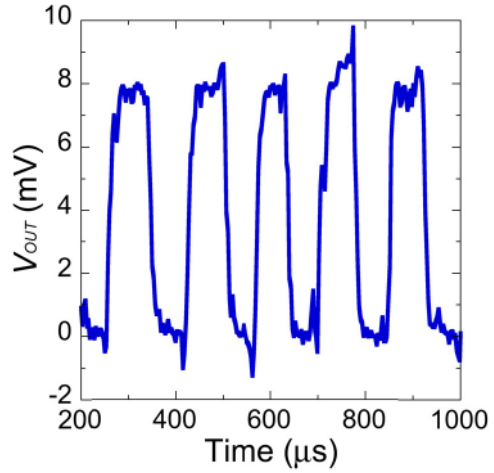

FIGURE 9. Output waveform of the nine-stage ring oscillator with device shot noise enabled.

the power consumption was 1.5 fW. This result highlights the potential for extreme voltage scalability offered by TFETs.

TABLE 2. Ring oscillator jitter.

V_{DD}	Jitter
8 mV	57 µs
16 mV	0.4 µs

Device noise was not included in the simulation in Fig. 8. To investigate the effect of noise, shot noise was enabled for all transistors and simulations of the ring oscillator at two supply voltages were performed. An example output waveform of the ring oscillator with noise is depicted in Fig. 9. The standard deviation of period jitter was extracted and is tabulated in Table 2. As expected, the jitter decreases as the supply voltage is increased.

IV. CONCLUSION

TFETs outperform CMOS at the 14-nm node in the subthreshold and near-threshold regions for analog applications. By making use of the larger g_m/I_D ratio in the subthreshold regime, the TFET amplifier achieves a voltage gain larger than 40 dB with a power consumption of less than 200 pW, well beyond the capabilities of CMOS. A nine-stage ring oscillator is shown to operate at a supply voltage as low as 8 mV while consuming only 1.5 fW, making it ideal for applications utilizing energy harvesting.

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HAO LU, photograph and biography not available at the time of publication.

PAOLO PALETTI received the M.Sc. degree in electronics engineering from the University of Pisa, Pisa, Italy, in 2013, and the M.Sc. degree in electrical engineering from the University of Notre Dame, Notre Dame, IN, USA, in 2016, where he is currently a graduate student with Prof. A. Seabaugh's group.

In 2014, he was a Research Assistant with the Nanoscale Device Simulation Laboratory, Information Engineering Department, University of Pisa. He joined the University of Notre Dame in 2014. His current research interests include the development of novel energy-efficient devices based on low-dimensional materials.

WENJUN LI, photograph and biography not available at the time of publication.

PATRICK FAY (M'91–SM'02–F'16) received the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 1996.

He is a Professor with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN, USA, where he has been on the faculty since 1997. He has authored or co-authored over 250 journal papers and conference proceedings. His current research interests include the design, fabrication, and characterization of compound semiconductor-based microwave, millimeter-wave, terahertz electronic devices and circuits, the experimental study of high-speed devices and circuits based on high electron mobility transistors, heterojunction bipolar transistors, resonant tunnel diodes, and heterostructure backward tunnel diodes in the arsenide, phosphide, antimonide, nitride III–V material systems, high-speed compound semiconductor p-i-n and metal-semiconductor-metal photodetectors, monolithically integrated optoelectronic circuits for fiber optic telecommunications applications, and the development and use of micromachining techniques for the fabrication of microwave through sub-millimeter-wave components, packaging, and interconnects. He holds seven issued patents in the areas of his research.

Prof. Fay serves as an IEEE Distinguished Lecturer of the Electron Devices Society.

TROND YTTERDAL (M'95–SM'00) received the M.Sc. and Ph.D. degrees in electrical engineering from the Norwegian Institute of Technology, Trondheim, Norway, in 1990 and 1995, respectively.

He was a Research Associate with the Department of Electrical Engineering, University of Virginia, Charlottesville, VA, USA, from 1995 to 1996, and a Research Scientist with the Electrical, Computer and Systems Engineering Department, Rensselaer Polytechnic Institute, Troy, NY, USA, from 1996 to 1997. From 1997 to 2001, he was a Senior ASIC Designer at Nordic Semiconductor, Trondheim, Norway. Since 2001, he has been on the faculty of the Norwegian University of Science and Technology, where he is currently a Professor with the Department of Electronics and Telecommunications. His current research interests include the design of analog integrated circuits, behavioral modeling and simulation of mixed-signal systems, modeling of nanoscale transistors, and novel device structures for application in circuit simulators. He has authored and/or co-authored over 200 scientific papers in international journals and conference proceedings. He is a co-author of the books *Semiconductor Device Modeling for VLSI* (Prentice Hall, 1993), the *Introduction to Device Modeling and Circuit Simulation* (Wiley, 1998) and *Device Modeling for Analog and RF CMOS Circuit Design* (Wiley, 2003). He has been a contributor to several other books published internationally. He is also a Co-Developer of the circuit simulator AIM-Spice.

Prof. Ytterdal is a member of the Norwegian Academy of Technological Sciences.

ALAN SEABAUGH (S'78–M'79–SM'92–F'03) received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, VA, USA, in 1985.

He was with the National Bureau of Standards, Gaithersburg, MD, USA, from 1979 to 1986, the Texas Instruments Central Research Laboratory, Dallas, TX, USA, from 1986 to 1997, and Raytheon, Dallas, from 1997 to 1999. He joined the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN, USA, in 1999, where he is a Frank Freimann Professor of electrical engineering.