Twisted Differential Line Structure on High-Speed Printed Circuit Boards to Reduce Crosstalk and Radiated Emission

Dong Gun Kam, Heeseok Lee, and Joungho Kim

***Abstract*—Differential signaling has become a popular choice for high-speed digital interconnection schemes on printed circuit boards (PCBs), offering superior immunity to crosstalk and external noise. However, conventional differential lines on PCBs still have unsolved problems, such as crosstalk and radiated emission. When more than two differential pairs run in parallel, a line is coupled to the line adjacent to it because all the lines are parallel in a fixed order. Accordingly, the two lines that constitute a differential pair are subject to the differential-mode crosstalk that cannot be canceled out by virtue of the differential signaling.**

To overcome this, we propose a twisted differential line (TDL) structure on a high-speed multilayer PCB by using a concept similar to a twisted pair in a cable interconnection. It has been successfully demonstrated by measurement and simulation that the TDL is subject to much lower crosstalk and achieves a 13–dB suppression of radiated emission, even when supporting a 3-Gb/s data rate.

***Index Terms*—Crosstalk, differential signaling, radiated emission, transmission line, twisted differential line, twisted pair.**

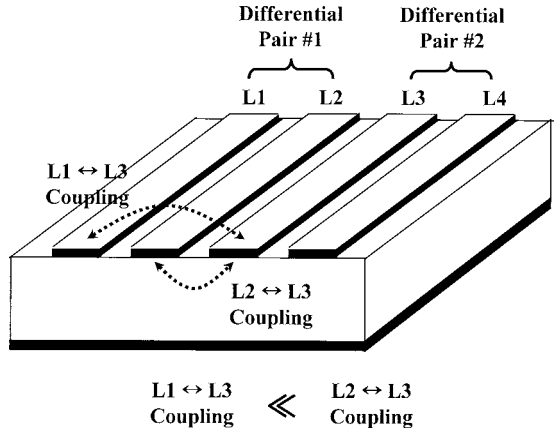

Fig. 1. Conventional coupled microstrip line (MCLIN) configuration.

I. Introduction

THE EVER-increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs, and routers, etc., is forcing the off-chip data rate into the gigabit-per-second range [1]. In the last decade, high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for integrated circuit (IC) packages and printed circuit boards (PCBs). For this reason, the off-chip data rate should move to the range of gigabit-per-second-per-pin in the near future. Indeed, the design roadmap of the Semiconductor Industry Association (SIA) forecasts that a board-level clock frequency will be over 1 GHz in 2005 [2]. In order to ensure reliable operation at such a high data rate, differential signaling has become a popular choice for multigigabit digital applications [3]. Differential signaling implies that two signal traces are generated with equal magnitudes with a 180° phase difference between the two. One benefit of the differential signaling is the suppression of radiated emissions due to the cancellation of magnetic fields resulting from opposing current flows. From a signal integrity standpoint, differential signaling has the ability to reject common-mode noise, such as crosstalk, simultaneous switching noise (SSN), and power supply and ground bounce noise [4], [5].

In order to support the differential signaling, differential lines are required. Conventional differential line structures on multilayer PCBs include coupled microstrip lines (MCLIN), coplanar strips, edge-coupled striplines, and broadside-coupled striplines [3]. However, all of these have an unsolved problem, namely, differential-mode crosstalk between neighboring differential pairs. When more than two differential pairs run in parallel, as shown in Fig. 1, a line is mainly coupled to the adjacent line because all the lines are parallel and in a fixed order. Accordingly, the two lines that constitute a differential pair are subjected to differential-mode crosstalk, which cannot be canceled out by virtue of differential signaling. As the spacing between two neighboring differential pairs is reduced and the rise times of digital signals become shorter, crosstalk becomes a more severe problem, strongly influencing the reliability and the signal integrity of the system. It generates additional delays, skews, jitters, or false switching of digital logic, degrading the noise margin and the timing margin of the system [4], [5].

To overcome this, we propose a twisted differential line (TDL) structure on a high-speed multilayer PCB. It has been successfully demonstrated by measurement and simulation that the TDL is subject to much lower crosstalk and achieves a 13–dB suppression of radiated emission when supporting a 3-Gb/s data rate.

Manuscript received April 23, 2003; revised Jauary 14, 2004. This work was supported by Center for Electronic Packaging Materials of Korea Science and Engineering Foundation.

The authors are with the Terahertz Interconnection and Package Laboratory, Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: kamdong@ieee.org; teralab@ee.kaist.ac.kr; joungho@ee.kaist.ac.kr).

Digital Object Identifier 10.1109/TADVP.2004.831838

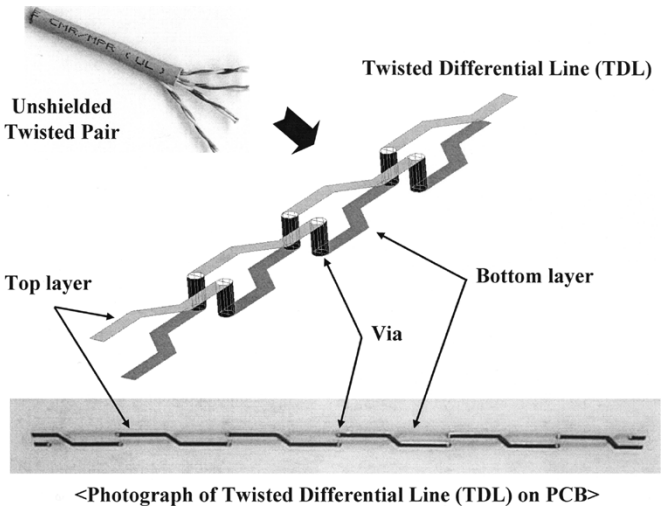

Fig. 2. Schematic of the proposed twisted differential line (TDL) structure.

II. Proposed Twisted Differential Line Structure

As is well known in the field of cable interconnection, a twisted pair provides a simple means of reducing the susceptibility to external noise [4]. Because the signal and return wires are intertwined, any external noise collected by one wire is also collected by the other wire. Therefore, a differential receiver can be directly used at a receiving end to filter out the common signal in both wires. It is also well known that the reduced loop area formed by the signal and return wires of a twisted pair greatly minimizes radiated emission.

Fig. 2 shows the proposed TDL structure, where the concept of the twisted pair is implemented on a high-speed multilayer PCB by using two-segmented conductor traces on a first and a second layer of the PCB, crisscrossing each other using many vias. The TDL has several advantages because of its physical configuration. First, the reduced loop area and opposing current flows formed by the TDL greatly minimize radiated emission as shown in Fig. 3(a). Second, the TDL increases the effective spacing of neighboring differential pairs as shown in Fig. 3(b). Because any two formerly nearest-neighbor lines (see Fig. 1) are periodically transposed [6], the effective spacing between the two increases, thereby reducing the average mutual capacitance and inductance. Third, a quarter of a period offset scheme on the TDL (named offset TDL) provides a balanced operation for each differential pair, thereby reducing the differential-mode crosstalk between neighboring differential pairs, as shown in Fig. 3(c) [7].

However, both the TDL and offset TDL may exhibit considerably more current crowding in the edge of conductors, similar to the edge-coupled stripline, which can lead to significant increase in loss compared to typical lines [8]. To overcome this, we also propose a vertical TDL, as shown in Fig. 4, where the two conductor traces overlap vertically, and they widen only when they are twisted by changing layers. Because the two lines are broadside-coupled, the conductor loss due to the current crowding can be reduced. Furthermore, by applying the offset scheme to the vertical TDL, we can accommodate 1.5 times more lines than those afforded by either TDL or offset TDL in the same area.

III. Propagation Characteristics

We conducted a full wave analysis on the TDL to determine its propagation characteristics. Because the TDL is a periodic structure, the finite difference time domain (FDTD) method based on periodic waveguide theory can be used [9]. According to that theorem, a unit cell analysis is sufficient for characterization of the entire structure, saving considerable computational resources. A unit cell can be defined as shown in Fig. 5. We assumed that 0.3-mm-thick FR4 substrate having a relative dielectric constant (ε_r) of 4.5 is placed between the two layers, and elsewhere, air is assumed. Applying an electric field between the two neighboring vias sets the initial condition. With a predetermined propagation constant (β), the FDTD simulation was performed to obtain an impulse response. The peak frequency of the modes corresponding to β can be obtained by the fast Fourier transform (FFT) of the impulse response. Repeating the FDTD simulation and the subsequent FFT with sweeping β gives a dispersion diagram. The first branch of the dispersion diagram is presented in Fig. 6. The interest in periodic waveguide structures arises from the two basic properties, namely 1) passband/stopband characteristics, and 2) the slow wave effect [10]. For the TDL, the simulation results show that a stopband does not appear below 25 GHz. Furthermore, it is clearly demonstrated from the linear dispersion diagram that the TDL supports quasi-TEM mode above 10 GHz. In addition, the TDL test pattern has a slow wave factor (SWF) of 2.33 because the total routing length is increased by twisting. This results in an increased time delay, which makes inroads on the timing margin for a high-speed digital system. Therefore, this should be balanced against the improvement in noise immunity.

The electromagnetic field profiles of the x–y cross section at several points on the z-axis are shown in Fig. 7. It should be noted that the propagating wave is well confined in the TDL and is circularly polarized. The TDL functions as a solenoid, one of the most efficient structures to confine electromagnetic fields, thereby prohibiting them from radiating. Furthermore, the FDTD simulation gives all of the three-dimensional components of an electromagnetic field at each lattice point of the unit cell, from which we can calculate the differential impedance of the TDL. This is easily controlled, over a wide range, by changing the number of twists and by changing the dimension of lines and vias. As long as the rise time remains at least three times bigger than the total delay through a via, the via acts as a single lumped-element reactance, that is either an incremental shunt capacitance or an incremental series inductance [11]. Since the impedance of the TDL is affected by this incremental reactance, the design of an optimized via is very important. Any three-dimensional field simulation is helpful in optimizing via from the early stage of design, thereby controlling the impedance of the TDL.

IV. Equivalent Circuit Modeling

In this section, we describe an equivalent circuit model of the TDL. The advantages of the TDL are demonstrated by quantitative comparison of its extracted model parameters with those of the MCLIN. Fig. 8 illustrates an equivalent circuit model of two coupled differential pairs per unit length. The parameters

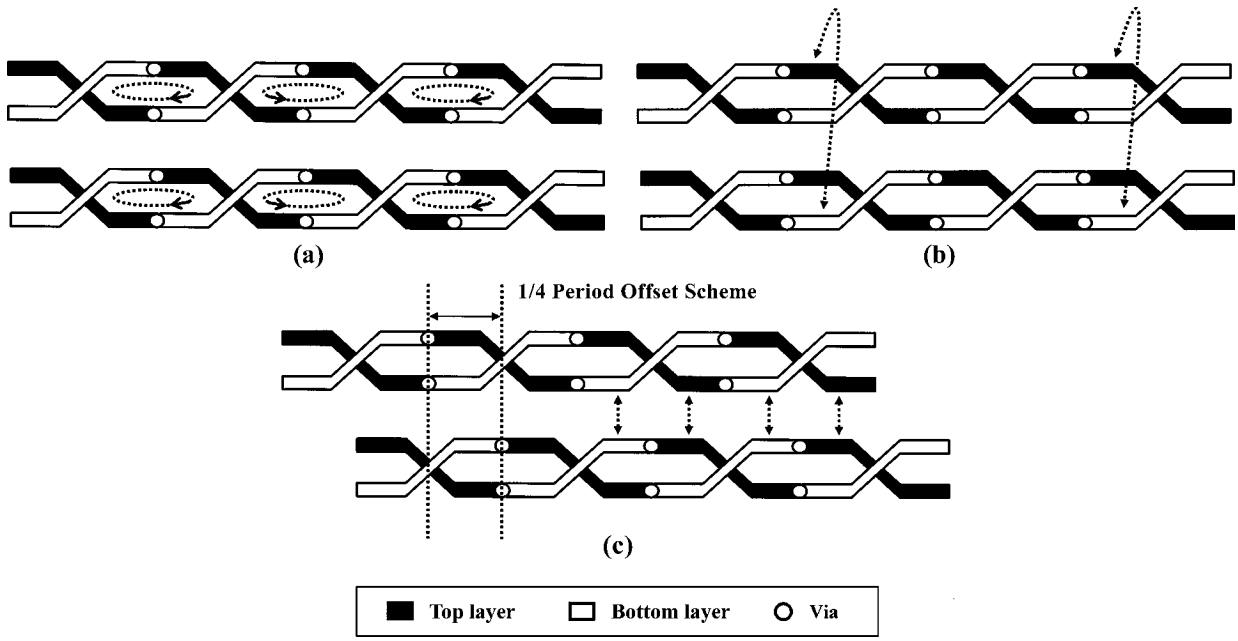

Fig. 3. Several advantages of the proposed TDL exist because of its physical configuration. (a) Reduced loop area and opposing current flows. (b) Increased effective spacing between the two formerly nearest-neighbor lines. (c) Balanced operation of each differential pair by using a quarter of a period offset scheme.

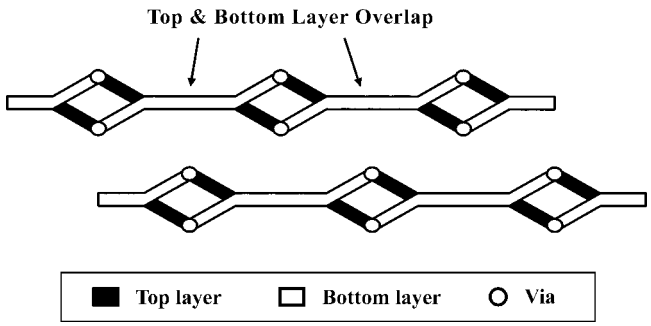

Fig. 4. Schematic of the proposed vertical TDL.

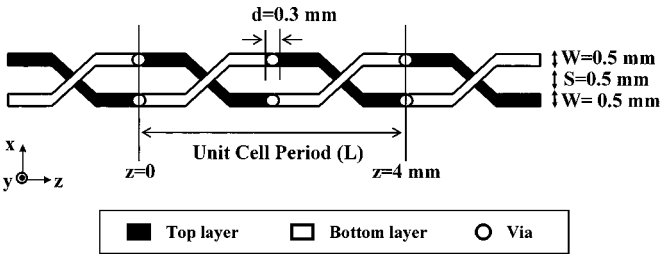

Fig. 5. Unit cell analysis of the TDL using the finite difference time domain (FDTD) method based on periodic waveguide theory.

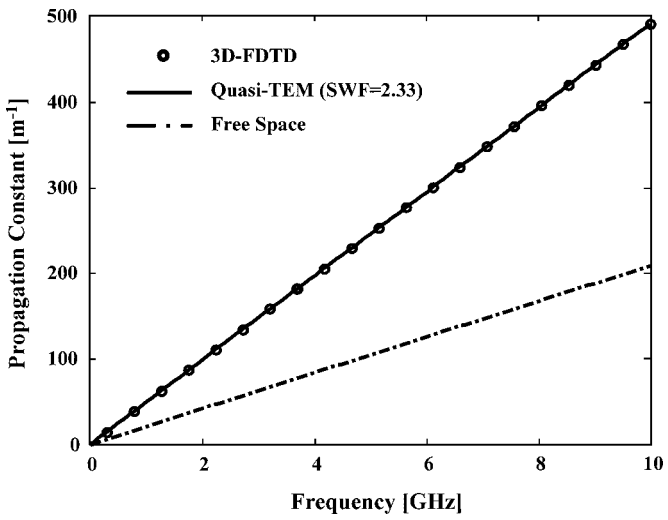

Fig. 6. First branch of the dispersion diagram of the TDL.

R_d (resistance), C_d (capacitance), and L_d (inductance) represent differential-mode signal propagation in each differential pair. Crosstalk between the two differential pairs is represented by mutual inductance between the differential pairs (L_{mdp}) and mutual capacitance between the differential pairs (C_{mdp}). Fig. 9 shows a test pattern and its corresponding model. Cascaded connection of N unit cells, where N is determined based on the line length and the highest frequency of interest, represent the complete coupled differential pairs [12]. N was chosen as 100 for modeling 100-mm-long differential pairs for frequencies up to 3 GHz.

The model parameters were extracted by scattering parameter (S-parameter) measurement and a subsequent parameter fitting process [13]. The detailed modeling procedure is summarized in Fig. 10. First, the single-ended four-port S-parameters were measured, while the other ports were terminated with 100-Ω chip resistors. After de-embedding the connector pad effect [14], they were transformed into the differential-mode two-port S-parameters based on mixed-mode S-parameter theory [15]. The differential-mode S-parameters were also calculated by circuit simulation of the equivalent circuit model. Then, the simulated S-parameters were compared with the measured S-parameters. Changing the values of the model parameters continued until the fitting process minimized the difference

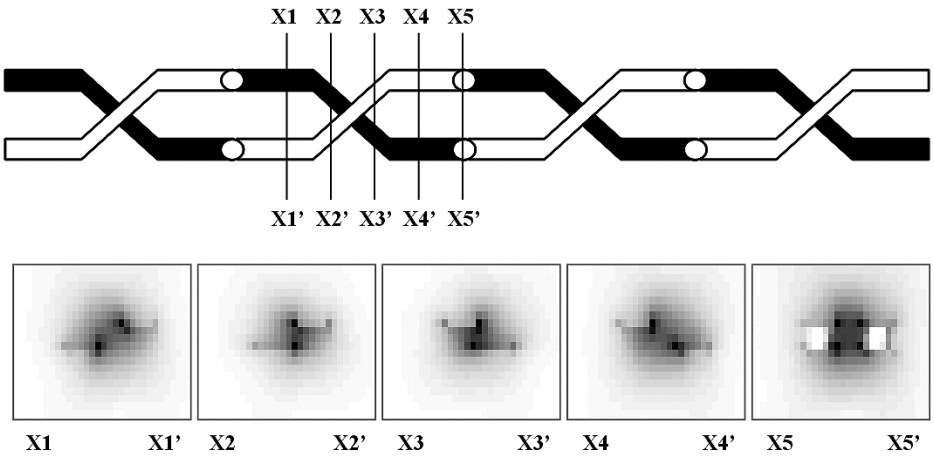

Fig. 7. Electromagnetic field profiles of the x-y cross-section.

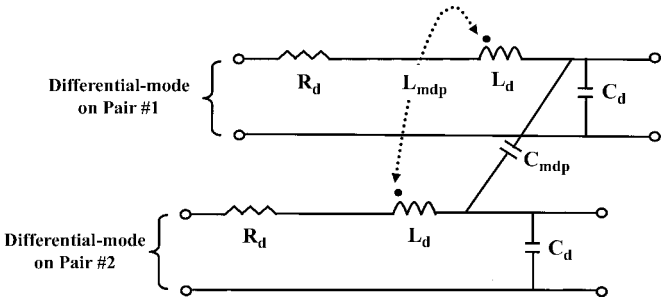

Fig. 8. Equivalent circuit model of two coupled differential pairs per unit length.

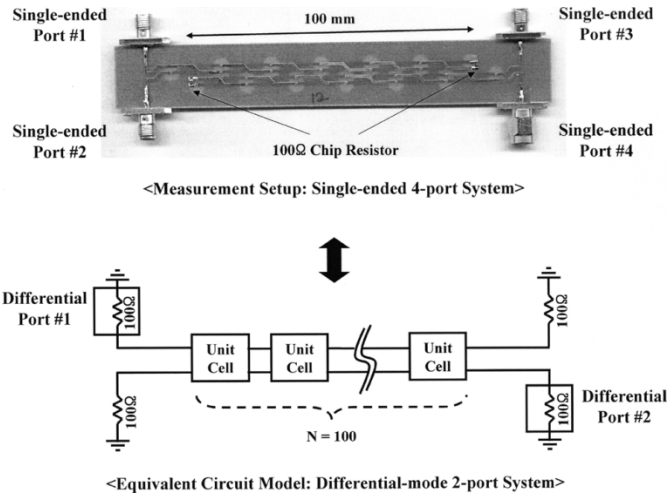

Fig. 9. Test pattern and its corresponding model.

between the two sets of parameters. Finally, the extracted model parameters were confirmed by comparing the SPICE simulation, based on the model, with time domain crosstalk measurement.

Using the modeling procedure described above, we modeled four types of differential lines: the MCLIN, TDL, offset TDL, and vertical TDL (with the offset scheme). Each of these had been designed to have the same gap between the two differential pairs and a differential impedance of 100 Ω with the assistance

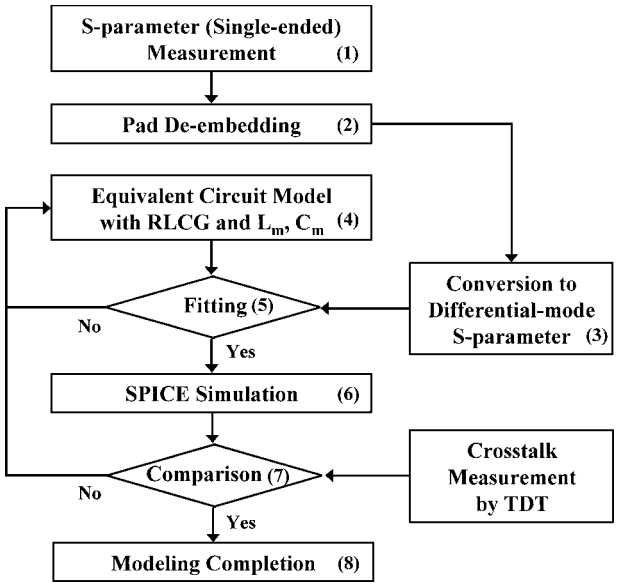

Fig. 10. Equivalent circuit modeling procedure.

of the FDTD simulation, which was confirmed by the calculated differential impedance from the measured S-parameters [16].

The extracted model parameters are listed in Table I. First, the mutual inductance (L_{mdp}) becomes considerably smaller in the TDLs, because the magnetic fields generated by two consecutive loops cancel each other. Second, the mutual capacitance (C_{mdp}) is also greatly reduced by applying the offset scheme. It enables the two lines in a differential pair to be equally influenced by adjacent lines, reducing the capacitive crosstalk between neighboring differential pairs. As a result, the mutual capacitance of the offset TDL or the vertical TDL is only approximately 10% of that of the MCLIN. Finally, as expected, the vertical TDL exhibits the smallest attenuation constant.

V. Measurement of Crosstalk, Radiated Emission, and Eye Diagram

We measured the far-end crosstalk (FEXT) voltage waveform of the four test patterns using time domain transmission (TDT) as shown in Fig. 11(a). A differential step pulse of 500 mV and

TABLE I
EXTRACTED MODEL PARAMETERS OF COUPLED DIFFERENTIAL PAIRS

	MCLIN	TDL	Offset TDL	Vertical Offset TDL
R_d [mΩ/mm]	66.6	89.6	89.6	61.3
L_d [nH/mm]	0.581	0.786	0.780	0.908
C_d [fF/mm]	59.7	75.6	75.9	89.6
Z_{diff} [Ω]	98.7	102	101	101
L_{mdp} [pH/mm]	12.4	2.30	2.17	2.09
C_{mdp} [fF/mm]	4.05	2.51	0.45	0.41
*α [x10^{-4}/mm]	3.54	4.39	4.42	3.04

*) $\alpha = \mathrm{Re}\{\sqrt{(R_d + j\omega L_d)\cdot(G_d + j\omega C_d)}\}$ @1GHz

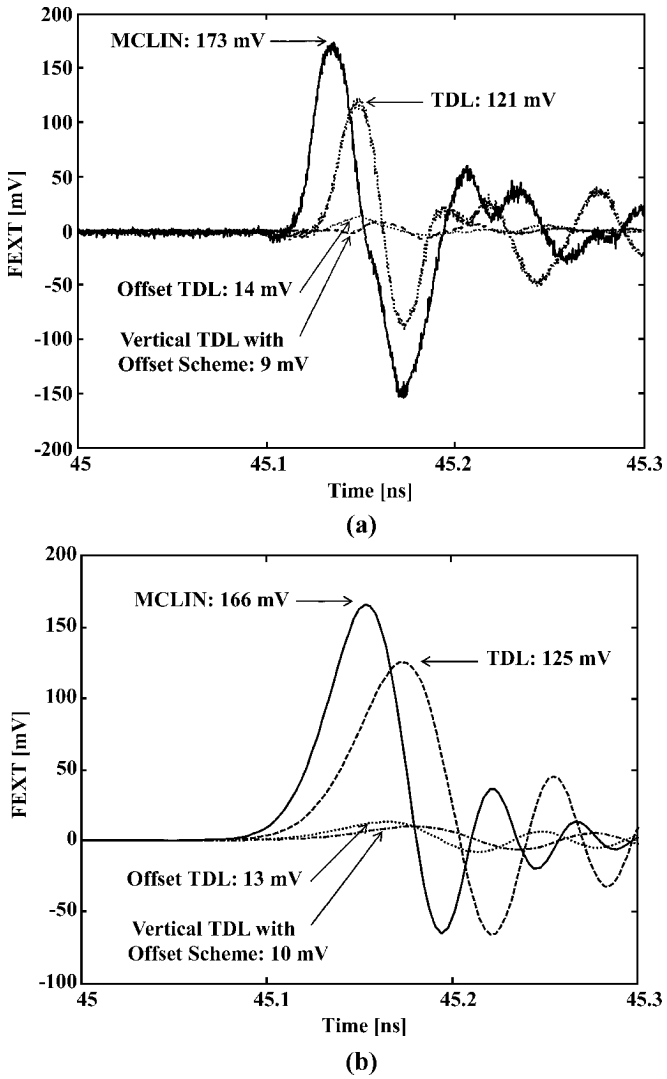

Fig. 11. (a) Measured far-end crosstalk (FEXT) voltage waveform. (b) Simulated FEXT voltage waveform.

30-ps rise time was input to one end of a differential line, and the FEXT voltage waveform was measured at the far end of the other differential line, while the remaining ports were terminated with 100-Ω chip resistors. First, the FEXT of the TDL was reduced to 121 mV, compared with the MCLIN at 173 mV,

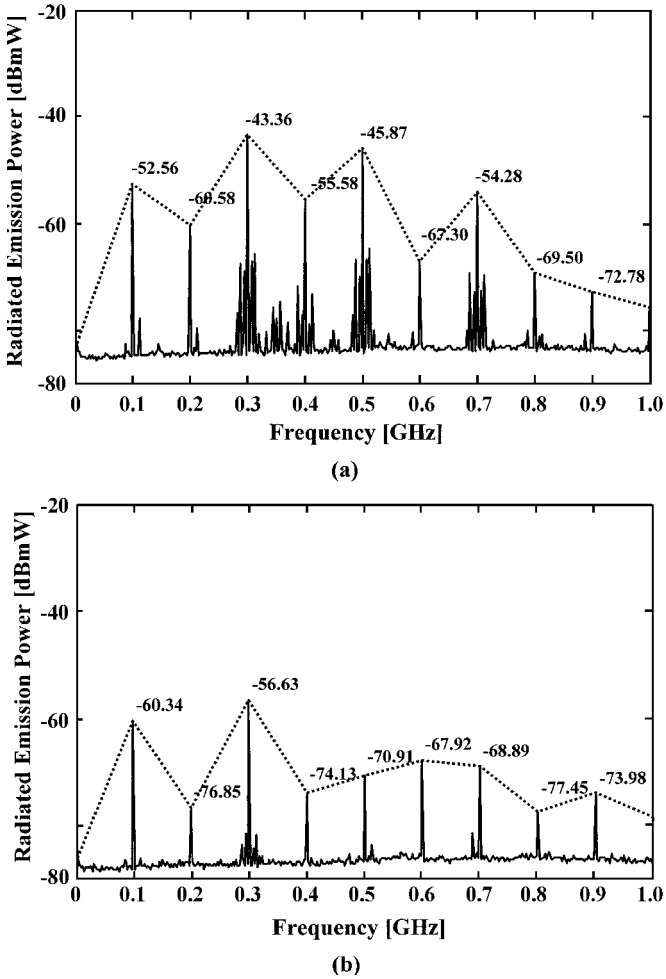

Fig. 12. Measured radiated emission spectrum, where the peak envelope is indicated by a dotted line. (a) MCLIN. (b) TDL.

by virtue of the increased effective spacing between the two differential pairs. Second, the FEXT of the offset TDL was significantly reduced to 14 mV: less than 10% of that of the MCLIN. It should be noticed that the offset scheme improves the crosstalk immunity further. Third, the vertical TDL showed a similar performance to the offset TDL. These results clearly demonstrate the validity of our design concept. Furthermore, as shown in the Fig. 11(b), the crosstalk waveform obtained by simulation based on the equivalent circuit model is in good agreement with the measured waveform.

We also measured the radiated emission spectrum in an anechoic chamber, as shown in Fig. 12. Because a 100-MHz digital clock was applied using a crystal oscillator, the spectrum is composed of the harmonics of 100 MHz. In order to feed the differential signals, unshielded twisted pair (UTP) cables and baluns (dc $\sim$ 600 MHz) were used. All the devices except the test pattern were well shielded, and the test differential line was terminated with a 100-Ω chip resistor. For the MCLIN, the peak was -43.36 dBmW at the third harmonic, whereas the peak was only -56.63 dBmW for the TDL. Therefore, the TDL achieved a 13-dB suppression of radiated emission compared with the MCLIN by virtue of the reduced loop area and opposing current flows.

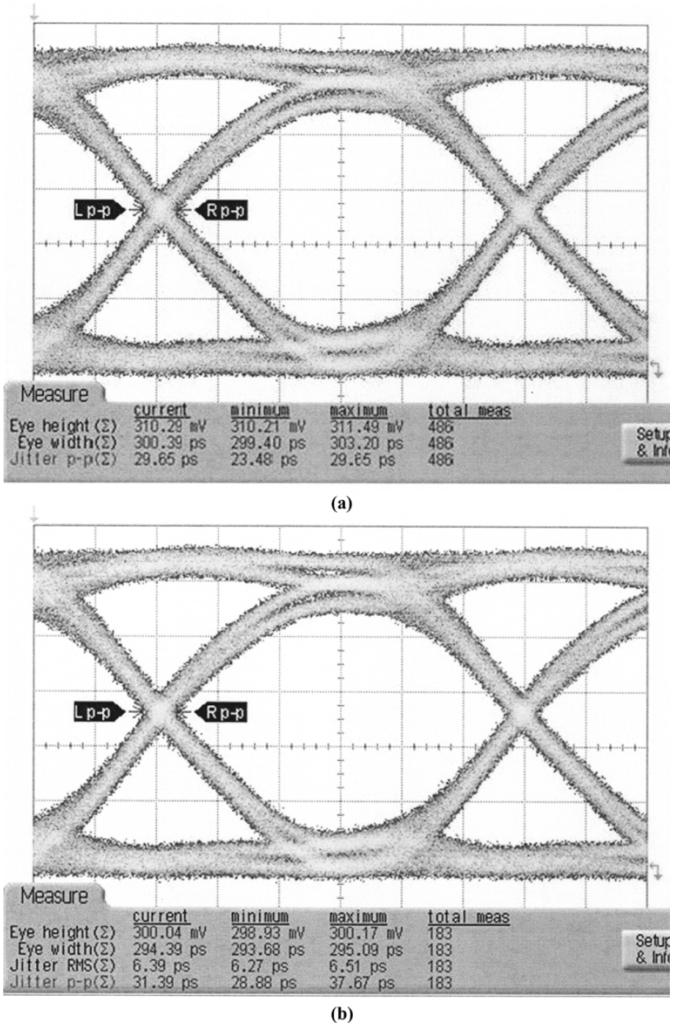

Fig. 13. Measured eye diagram. (a) MCLIN. (b) TDL.

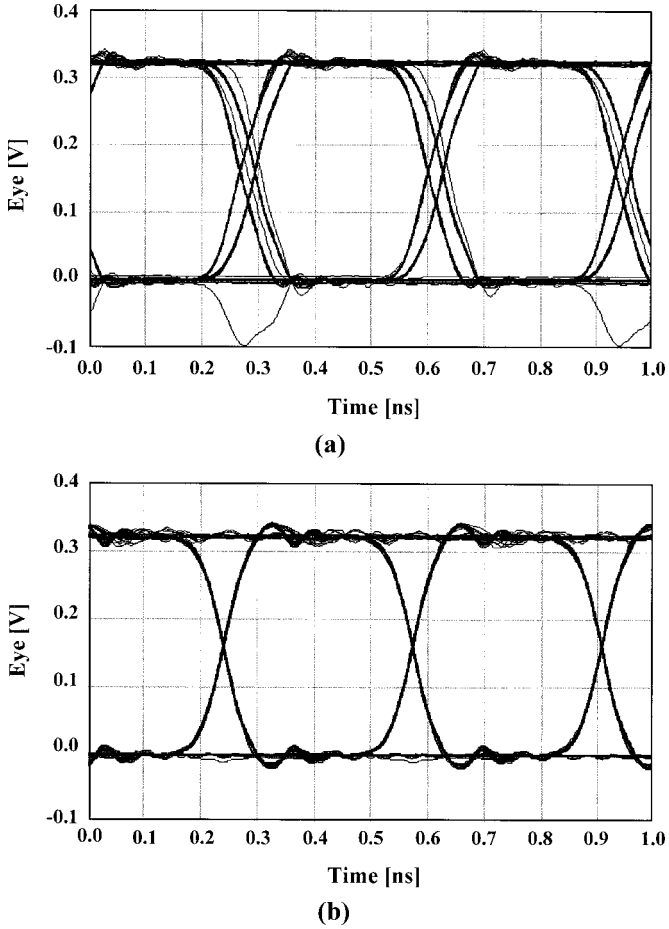

Fig. 14. Eye diagram simulation of three neighboring differential pairs. (a) MCLIN. (b) TDL.

The transmission bandwidth of the TDL was found to be maintained at a similar level to the MCLIN by the eye diagram measurement, as shown in Fig. 13. A differential 3-Gb/s $2^{31} - 1$ nonreturn-to-zero (NRZ) pseudo-random bit sequence (PRBS) was used. When a pulse pattern generator was directly connected to a digital sampling oscilloscope without passing through any test pattern, the peak-to-peak jitter at the zero-crossing point was measured at 14.83 ps, and the eye height and width were 381 mV and 312 ps, respectively. For the MCLIN, the peak-to-peak jitter, the eye height and width were 29.65 ps, 310 mV, and 300 ps, respectively. However, for the TDL, the peak-to-peak jitter, the eye height and width were 31.39 ps, 300 mV, and 294 ps, respectively. At a glance, the TDL was expected to have a much more distorted eye diagram than the MCLIN because it has many discontinuities due to vias and segmented traces. However, the intersymbol interference (ISI) [5] of the TDL is not as great as expected. The clear eye diagram of the TDL demonstrates a successful digital data transmission over 3 Gb/s.

In addition, when several differential pairs run in parallel, the transmission bandwidth is strongly affected by the crosstalk between the differential pairs as well as the ISI. Therefore, we produced an eye diagram simulation using a circuit simulator and a three-line model [5]. Assuming that three differential pairs would run in parallel, we assigned the middle differential pair as the victim. A $2^7 - 1$ NRZ PRBS was independently input to each differential pair. In order to estimate the worst case skew, every combination of the even and odd mode between the three differential pairs was taken into consideration. The model parameters extracted previously were used in the three-line model. As shown in Fig. 14, the MCLIN has the worst case skew of nearly 50 ps. However, the offset TDL has a worst case skew of less than 10 ps. Because every differential pair is well balanced by the offset scheme in the TDL, the phase velocity does not depend significantly on the pulse patterns, thereby reducing the worst case skew.

So far, we have investigated various designs of TDL structures. It was clearly demonstrated that the TDL is subject to lower crosstalk and achieves considerable suppression of radiated emission. Although the signal quality in the TDL and offset TDL seems to be degraded by more current crowding effect in the edge of conductors, the vertical TDL shows even better performance than the conventional MCLIN because the two lines of the vertical TDL are broadside-coupled. At design, optimization of the tradeoff between the transmission bandwidth and the noise immunity should be determined. The most critical design parameter is the number of twists. It was found that adding more twists increases the attenuation constant as well as the

time delay, which is mainly resulted from the increased routing length. However, the number of twists does not significantly change the crosstalk immunity. Since both L_{mdp} and C_{mdp} can be considerably reduced only if the offset scheme is adopted, moderate number of twists is preferable, which are at most less than 10 for a 100-mm-long signal link.

VI. Conclusion

Since the adoption of differential signaling, crosstalk has remained a major problem as the required data rate has continually increased. We propose a twisted differential line (TDL) on a high-speed multilayer PCB using the concept of a twisted pair in cable interconnections. The reduced crosstalk and suppressed radiated emission of the TDL is a remarkable achievement while maintaining the transmission bandwidth. Furthermore, because the lines of the TDL are tightly coupled to each other and the electromagnetic fields are well confined, the effect of the reference plane discontinuity [8] becomes minimal. Even without a ground reference plane, the TDL can support data transmission at a very high data rate.

Therefore, the proposed TDL delivers a promising solution for high-speed and high-density digital interconnection designs on PCBs in spite of the increased manufacturing cost. Although our consideration in this paper was limited to PCB-level interconnections, TDL can be readily applied to other level interconnections, including packages, connectors, and chips.

References

[1] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-um CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 706–711, 2001.

[2] The National Technology Roadmap for Semiconductors, Semiconductor Industry Associations, 2000.

[3] H. Wu, W. Beyene, N. Cheng, H. Ching-Chao, and C. Yuan, "Design and verification of differential transmission lines," in *Proc. 10th Topical Meeting Electrical Performance Electronic Packaging*, 2001, pp. 85–88.

[4] H. Ott, *Noise Reduction Techniques in Electronic Systems*. New York: Wiley, 1988.

[5] S. Hall *et al.*, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*. New York: Wiley, 2000.

[6] R. Voelker, "Transposing conductors in signal buses to reduce nearest-neighbor crosstalk," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1095–1099, May 1995.

[7] N. Kim, M. Sung, H. Kim, S. Baek, W. Ryu, J. An, and J. Kim, "Reduction of crosstalk noise in modular jack for high-speed differential signal interconnection," *IEEE Trans. Advanced Packaging*, vol. 24, pp. 260–267, Aug. 2001.

[8] P. Fornberg, M. Kanda, C. Lasek, M. Piket-May, and S. Hall, "The impact of a nonideal return path on differential signal integrity," *IEEE Trans. Electromag. Compat.*, vol. 44, pp. 11–15, Feb. 2002.

[9] H. Lee, N. Kim, and J. Kim, "Unit cell modeling of meander delay line based on finite-difference time-domain method and Floquet's theorem," in *Proc 10th Topical Meeting Electrical Performance Electronic Packaging*, 2001, pp. 193–196.

[10] R. Collin, *Foundation for Microwave Engineering*. New York: McGraw-Hill, 1996.

[11] H. Johnson and M. Graham, *High-Speed Signal Propagation—Advanced Black Magic*. Englewood Cliffs, NJ: Prentice-Hall, 2003, pp. 338–359.

[12] W. Cui, H. Shi, X. Luo, F. Sha, J. Drewniak, T. Van Doren, and T. Anderson, "Lumped-element sections for modeling coupling between high-speed digital and I/O lines," in *Proc. IEEE Int. Symp. Electromagnetic Compatibility*, 1997, pp. 260–265.

[13] M. Sung, N. Kim, J. Lee, H. Kim, B. Choi, J. Kim, J. Hong, and J. Kim, "Microwave frequency crosstalk model of redistribution line patterns on wafer level package," *IEEE Trans. Advanced Packaging*, vol. 25, pp. 265–271, May 2002.

[14] S. Ahn, J. Lee, J. Kim, W. Ryu, Y. Kim, C. Yoon, and J. Kim, "High-frequency electrical performance of a new high-density multiple line grid array (MLGA) package," in *Proc. 50th Electronic Components and Technology Conf.*, 2000, pp. 497–501.

[15] D. Bockelman and W. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1530–1539, July 1995.

[16] Y. Eo and W. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 16, pp. 555–562, Aug. 1993.

Dong Gun Kam received the B.S. degree in physics and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2000 and 2002, respectively, where he is currently pursuing the Ph.D. degree.

His research interests include signal integrity and power integrity issues in system-in-package design.

Heeseok Lee received the B.S. degree in electronic communication engineering from Hanyang University, Seoul, Korea, in 1996 and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 1998 and 2003, respectively.

In 2003, he joined System LSI Division of Samsung Electronics, Kiheung, Korea, as a Senior Research Engineer. His research interests include high-speed package interconnections and power distribution systems.

Joungho Kim received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1984 and 1986, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1993.

During his graduate study, he was involved in femtosecond time-domain optical measurement technique for high-speed device and circuit testing. In 1993, he was with Picometrix, Inc., Ann Arbor, as a Research Engineer, where he was responsible for development of picosecond sampling systems and 70-GHz photo-receivers. In 1994, he joined the Memory Division of Samsung Electronics, Kiheung, Korea, where he was engaged in gigabit-scale DRAM design. In 1996, he moved to the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, where he is currently an Associate Professor with the Electrical Engineering and Computer Science Department. Since joining KAIST, his research centers on modeling, design, and measurement of high-speed interconnections, packages, and PCBs. His research topics includes design issues of signal integrity, power/ground noise, and radiated emission in high-speed SerDes channels, system-in-packages, and multilayer PCBs. He was on sabbatical leave from 2001 to 2002 at Silicon Image Inc., Sunnyvale, CA, as a Staff Engineer. He was responsible for low-noise package design of SATA, FC, and Panel Link SerDes devices. He has authored or coauthored over 100 technical articles and numerous patents.

Dr. Kim has served as the Chair or the Co-Chair of the EDAPS workshop since 2002.