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Two-Dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs)

MINGDA (OSCAR) LI[1,3], DAVID ESSENI[2], JOSEPH J. NAHAS[1], DEBDEEP JENA[1,3,4], AND HUILI GRACE XING[1,3,4]

1 Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA
2 Department of Electrical Engineering, University of Udine, Udine 33100, Italy
3 School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA
4 Department of Materials Science and Engineering, Cornell University, Ithaca, NY 14853 USA

CORRESPONDING AUTHOR: M. LI (e-mail: ml888@cornell.edu) and H. G. XING (e-mail: grace.xing@cornel.edu)

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ABSTRACT Layered 2-D crystals embrace unique features of atomically thin bodies, dangling bond free interfaces, and step-like 2-D density of states. To exploit these features for the design of a steep slope transistor, we propose a Two-dimensional heterojunction interlayer tunneling field effect transistor (Thin-TFET), where a steep subthreshold swing (SS) of ~14 mV/dec and a high on-current of ~300 μA/μm are estimated theoretically. The SS is ultimately limited by the density of states broadening at the band edges and the on-current density is estimated based on the interlayer charge transfer time measured in recent experimental studies. To minimize supply voltage V_{DD} while simultaneously maximizing on currents, Thin-TFETs are best realized in heterostructures with near broken gap energy band alignment. Using the $WSe_2/SnSe_2$ stacked-monolayer heterostructure, a model material system with desired properties for Thin-TFETs, the performance of both *n*-type and *p*-type Thin-TFETs is theoretically evaluated. Nonideal effects such as a nonuniform van der Waals gap thickness between the two 2-D semiconductors and finite total access resistance are also studied. Finally, we present a benchmark study for digital applications, showing the Thin-TFETs may outperform CMOS and III–V TFETs in term of both switching speed and energy consumption at low-supply voltages.

INDEX TERMS Tunnel FET, 2-D crystals, transport model, steep slope, subthreshold swing (SS), layered materials, benchmarking.

I. INTRODUCTION

Tunnel Field Effect Transistors (FETs) are perceived as promising electronic switches that may enable scaling the supply voltage V_{DD} down to 0.5 V or lower by reducing the subthreshold swing (SS) below 60 mV/dec at room temperature.

To date, numerous Tunnel FETs have been demonstrated, among which heterostructures with near broken gap band alignment are favored in order to achieve sub-60 mV/dec SS and high on currents simultaneously [1]. Tunnel FETs also require a very strong gate control over the channel region to obtain sub-60 mV/dec SS values; this in turn demands ultra-thin body or nanowire structures, where size induced quantization enlarges the bandgap and impedes the realization of near broken gap alignment [2]–[4]. Layered 2D crystals, such as monolayers of transition metal dichalcogenides (TMD) MX_2 (e.g., M = Mo, W; X = S, Se, Te) and other metal chalcogenides MX_x (e.g., M = Ga, Sn; X = O, S, Se) offer a native thickness of about 0.6 nm with a variety of bandgaps and band-alignments [4], [5]. Furthermore, 2D crystals possess a sharp turn on of density of states at the band edges and have no surface dangling bonds thus potentially enabling a low interfacial density of state, which are highly desired for achieving a sharp SS [6]. Recent experimental results show that the band alignment in stacked-monolayer 2D crystal heterostructures can be tuned by an external electric field perpendicular to the heterojunction plane [7] and the charge transfer in stacked-monolayer 2D

crystal heterojunctions is reasonably fast [8]. In such a context, we propose the Two-dimensional Heterojunction Interlayer Tunneling FET (Thin-TFET) based on a vertical arrangement of 2D layered materials. In particular, we discuss both *n*-type and *p*-type Thin-TFETs employing a promising material system of 2H-WSe_2 and 1T-$SnSe_2$. Our simulations suggest that very competitive SS values and a high on-current can be achieved in the Thin-TFETs. Along with the low intrinsic gate-to-drain and gate-to-source capacitances in comparison to CMOS and p-i-n III-V TFETs benchmarked in Section III-D, the Thin-TFETs enable fast switching and low energy consumption. The effect of a non-uniform van der Waals gap thickness and the external source and drain total access resistance are also discussed. At the end of the paper, we will also share some insights on the experimental realization of Thin-TFETs derived from the ongoing investigations in our laboratory.

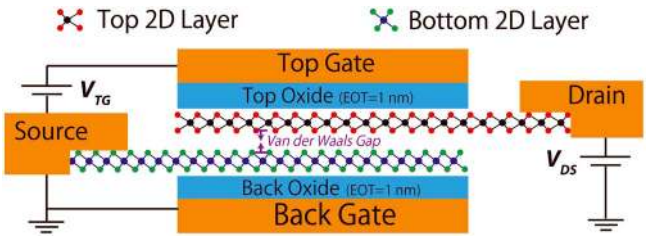

FIGURE 1. Schematic device cross section of a Thin-TFET.

II. DEVICE STRUCTURE AND MODELING APPROACH

The Thin-TFET device structure is shown in Fig. 1, where the bottom and top 2D semiconductors act as the source and the drain respectively. A van der Waals gap separates the top and bottom 2D semiconductors and the thickness of the van der Waals gap is defined as the distance from the center of the chalcogenide atom in the top 2D layer to the center of the nearest chalcogenide atom in the bottom 2D layer (see Fig. 1). The device working principle can be explained as follows: take the *p*-type Thin-TFET as the example, when the conduction band edge of the bottom 2D semiconductor E_{CB} is higher than the valence band edge of the top 2D semiconductor E_{VT} (see Fig. 2), tunneling from the bottom layer is inhibited and the device is nominally off. When a negative top gate voltage pulls E_{VT} above E_{CB} (see Fig. 3(a)), a tunneling window is opened thus current can flow.

To calculate the band alignment between E_{CB} and E_{VT} along the direction perpendicular to the 2D semiconductors we first use Gauss's law and write [9]

$$\begin{aligned} C_{TOX}V_{TOX} - C_{vdW}V_{vdW} &= e(p_T - n_T + N_T) \\ C_{BOX}V_{BOX} + C_{vdW}V_{vdW} &= e(p_B - n_B + N_B) \end{aligned} \quad (1)$$

where e is the magnitude of an electron charge, $C_{T(B)OX}$ is the capacitance per unit area of top (back) oxide, and C_{vdW} is the capacitance per unit area of the van der Waals gap. $V_{T(B)OX}$ and V_{vdW} are the corresponding potential drops. $n(p)_{T(B)}$ is the electron (hole) density in the top (bottom) 2D semiconductor layer, and N_T, N_B are the net chemical doping concentrations (donor minus acceptor) in the layers, which are set to zero in this work. The potential drops can be written in terms of the top gate V_{TG}, back gate V_{BG}, and drain-source voltage V_{DS} (which sets the split of the quasi-Fermi levels in the top and bottom semiconductor layers), and of the material properties as

$$\begin{aligned} eV_{vdW} &= eV_{DS} - e\phi_{p,B} - e\phi_{n,T} + E_{GB} + \chi_{2D,B} - \chi_{2D,T} \\ eV_{TOX} &= eV_{TG} + e\phi_{n,T} - eV_{DS} + \chi_{2D,T} - e\Phi_{M,T} \\ eV_{BOX} &= eV_{BG} - e\phi_{p,B} + E_{GB} + \chi_{2D,B} + e\Phi_{M,B} \end{aligned} \quad (2)$$

where we define $e\phi_{n,T(B)}=E_{CT(B)}-E_{FT(B)}$ and $e\phi_{p,T(B)}=E_{FT(B)}-E_{VT(B)}$, E_{GB} is the energy gap in the bottom 2D semiconductor and $E_{FT(B)}$ is the Fermi level in the top and bottom layers, $\chi_{2D,T(B)}$ is the electron affinity of the top (bottom) 2D semiconductor, and $\Phi_{M,T(B)}$ is the metal workfunction of the top (back) gate (see Fig. 2).

Using the effective mass approximation and assuming that the majority carriers of the two 2D semiconductors are at thermodynamic equilibrium with their Fermi levels [10], the carrier densities can be written as

$$n(p) = \frac{g_v m_c^* \left(m_v^*\right) k_B T}{\pi \hbar^2} \ln\left[\exp\left(-\frac{q\phi_{n,T}(\phi_{p,B})}{k_B T}\right) + 1\right] \quad (3)$$

where g_v is the valley degeneracy and $m_c^*(m_v^*)$ is the conduction (valence) band effective mass, and the rest of the parameters assume their common meanings.

By inserting Eqs. 2 and 3 in Eq. 1 we obtain two equations determining $\phi_{n,T}$, $\phi_{p,B}$ and thus the band alignment.

We calculate the tunneling current by using the transfer-Hamiltonian method [11], which was also recently revisited for resonant tunneling graphene transistors [12], [13]. We here summarize the basic equations; a more thorough discussion can be found in our earlier work [9]. The tunneling current density, J_T, is expressed as [9]:

$$\begin{aligned} J_T = {} & \frac{g_v e\,|M_{B0}|^2 A}{4\pi^3\hbar} \mathrm{e}^{-2\kappa T_{vdW}} \\ & \times \int_{\mathbf{k}_T}\int_{\mathbf{k}_B} d\mathbf{k}_T\, d\mathbf{k}_B\, S_F(q)\, S_E(E_B - E_T)\,(f_B - f_T) \end{aligned} \quad (4)$$

where κ is the decay constant of the wave-function in the van der Waals gap [12], [13], T_{vdW} is the thickness of the van der Waals gap, $\mathbf{k}_{T(B)}$, $E_{T(B)}$ and $f_{T(B)}$ are the wave-vector, the energy and Fermi occupation function in the top (bottom) 2D semiconductor and M_{B0} is the tunneling matrix element [9], which is a property of the material system and is further discussed in Section III. Equation 4 assumes that in the tunneling process electrons interact with a random scattering potential, whose spectrum is taken as $S_F(q) = \pi L_C^2/(1+\mathbf{q}^2 L_C^2/2)^{3/2}$, where $q=|\mathbf{k}_T-\mathbf{k}_B|$ and L_C is the correlation length. The scattering relaxes the momentum conservation, i.e., allowing tunneling for $\mathbf{k}_B \neq \mathbf{k}_T$. A similar $S_F(q)$ has been used to analyze the resonance linewidth in graphene tunneling transistors [13]. The S_F(q) may be representative of different scattering mechanisms that are discussed

in [9] and [13]. The energy broadening in the 2D semiconductors is described by $S_E(E)=\exp(-E^2/\sigma^2)/(\sqrt{\pi}\sigma^2)$, where σ is the energy broadening parameter [9].

Finally, after discussing the intrinsic device performance, the contact resistance is included in our model by self-consistently calculating the tunnel current density and the voltage drop on the total access resistance. The effect of the lateral resistance in the intrinsic Thin-TFET has been discussed in our prior work [14]. The key finding is that: when the tunnel current is sufficiently low ($\sim$1 μA/μm in the sub-threshold region), the tunnel junction resistance associated with the vertical current flow is much higher than the lateral resistance of the 2D semiconductor source and drain layers; as a result, the current distribution across the junction is rather uniform laterally in the sub-threshold region.

III. SIMULATION RESULTS AND DISCUSSIONS

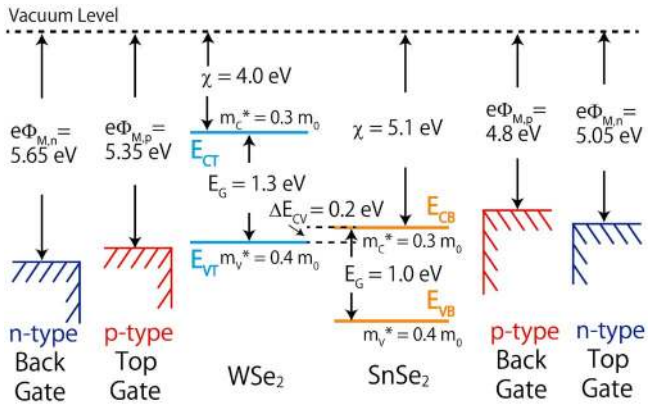

FIGURE 2. An example to realize both *n*-type and *p*-type Thin-TFETs using one pair of 2-D semiconductors (2H-WSe_2 and 1T-$SnSe_2$) with near broken gap band alignment. For the *n*-type Thin-TFET, $SnSe_2$ is the top (i.e., drain) 2-D layer and WSe_2 is the bottom (i.e., source) 2-D layer, along with the top and back gate labeled as *n*-type in blue. While for the *p*-type Thin-TFET, WSe_2 is the top (i.e., drain) 2-D layer and $SnSe_2$ is the bottom (i.e., source) 2-D layer, along with the top and back gate labeled as *p*-type in red; band gaps, electron affinities, effective masses are shown for WSe_2 and $SnSe_2$. The *n*-type and *p*-type metal work functions are tuned to give symmetric threshold voltages for the *n*-type and *p*-type Thin-TFETs.

A. MATERIAL SYSTEM AND N-TYPE & P-TYPE THIN-TFETS

Out of various 2D semiconductors studied by density function theory calculations [5] and experimental efforts, we chose the trigonal prismatic coordination monolayer (2H) WSe_2 and the octahedral coordination (CdI_2 crystal structure) monolayer (1T) $SnSe_2$ (see Fig. 2). $WSe_2/SnSe_2$ stacked-monolayer heterojunction can potentially form a near broken band alignment, which reduces the voltage drop in the van der Waals gap in the on-state condition [1]. Since there is no experimental band alignment reported for *monolayer* WSe_2 and $SnSe_2$, the band alignment of the $WSe_2/SnSe_2$ system used in this work are based on the existing experimental results of *multilayer* WSe_2 and $SnSe_2$ [15]–[17], while their approximated effective masses are based on the DFT results of monolayer WSe_2 and $SnSe_2$ [5] (see Fig. 2).

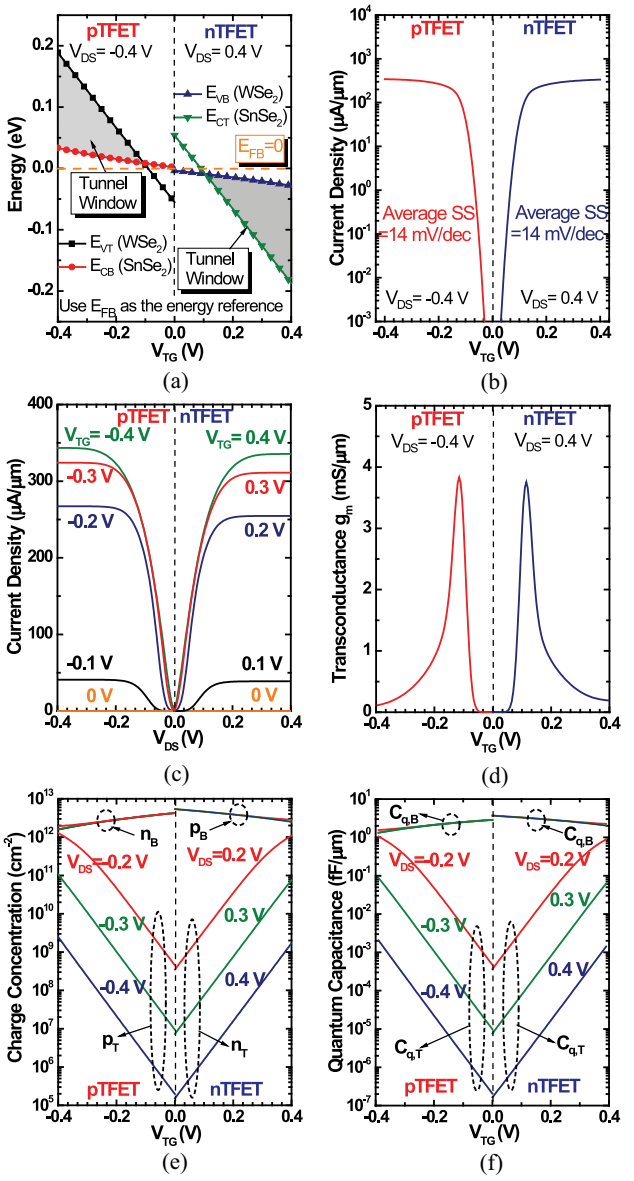

FIGURE 3. For the *n*-type and *p*-type Thin-TFETs shown in Fig. 2. (a) Band alignment versus V_{TG}. (b) Current density versus V_{TG}, the average SS is calculated from 10^{-3} μA/μm to 10 μA/μm. (c) Current density versus V_{DS} at various V_{TG}. (d) Transconductance versus V_{TG}. (e) Carrier concentration in the top and bottom 2-D layers versus V_{TG} at various V_{DS}. (f) Quantum capacitances of the top and bottom 2-D layers versus V_{TG} at various V_{DS}.

Following the complex band method [18], we assume the effective barrier height E_B of the van der Waals gap is 1 eV and the electron mass in the van der Waals gap is the free electron mass m_0, thus the decay constant is $\kappa = \sqrt{2m_0E_B/\hbar} = 5.12\ \text{nm}^{-1}$. In our model, we set the scattering correlation length L_C in $S_F(q)$ to L_C=10 nm, which is also consistent with the value employed in [13]; the energy broadening σ is set to be 10 meV. M_{B0} in Eq. 4 is directly related to the interlayer charge transfer time τ across the van der Waals gap, which can be written as [19]

$$\tau^{-1} = \frac{2\pi}{\hbar}\rho|M_{B0}|^2 e^{-2\kappa T_{vdW}} S_F(q) \qquad (5)$$

where $\rho=g_v m^*/\pi\hbar^2$ is the density of states (DOS). As can be seen from Eq. 5 and the expression of the scattering potential spectrum $S_F(q)$ (given after Eq. 4), due to scattering in our model, τ increases with increasing q, which is the magnitude of the wave-vector difference across the van der Waals gap defined as $q=|\mathbf{k}_T-\mathbf{k}_B|$. In a recent experiment, a charge transfer time of 25 fs has been observed across the van der Waals gap between a stacked-monolayer MoS_2/WS_2 heterostructure, which, according to Eq. 5, gives us M_{B0} ~0.02 eV when q=0. We recognize that the charge transfer time might be different for different 2D heterojunctions, nevertheless, this experimentally determined charge transfer time is a reasonable value to use for the first pass estimate. Thus, we choose M_{B0}=0.02 eV in all following simulations.

Throughout this work, the gate length is set to be 15 nm, the back gate and source are grounded. An effective oxide thickness (EOT) of 1 nm is used for both the top and back oxide, which gives a top (back) oxide capacitance C_{TG} (C_{BG}) of 0.518 fF/μm. The thickness of the van der Waals gap is set to 3.5 Å, unless specified otherwise. We assume the relative dielectric constant of the van der Waals gap is 1.0, therefore the van der Waals gap capacitance C_{vdW} is 0.38 fF/μm. The external total access resistances are considered after the intrinsic device performance is discussed first (Figs. 3 and 4).

The example material systems for *n*-type and *p*-type Thin-TFETs based on the stacked-monolayer WSe_2 and $SnSe_2$ are shown in Fig. 2. The metal work functions are tuned to obtain a symmetric threshold voltage for the *n*-type and the *p*-type Thin-TFET. Fig. 3(a) shows the band alignment versus V_{TG}. V_{TG} can effectively control the vertical band alignment in the device by controlling primarily the band edge of the top (i.e., drain) layer while having a weak effect on the band edge of the bottom (i.e., source) layer, so that a tunneling window is modulated. Fig. 3(b) shows I_D versus V_{TG} transfer curves with very compelling average SS of ~14 mV/dec averaged from 10^{-3} μA/μm to 10 μA/μm. The I_D versus V_{DS} family curves are shown in Fig. 3(c). I_D saturates for V_{DS} when V_{DS}>~0.2 V. The superlinear onset is also observed and the so called V_{DS} threshold voltage increases at lower V_{TG} [20]. A peak transconductances of ~4 mS/μm is observed around V_{TG}=0.12 V (Fig. 3(d)), which are much larger than ~0.8 mS/μm reported peak transconductances of 10 nm Fin-FET [21]. In Fig. 3(e), the top gate changes the carrier concentrations of the top 2D semiconductor much faster than of the bottom 2D semiconductor under different V_{DS}. The ability to efficiently change a hole (electron) concentration in the top 2D semiconductor while keeping a high electron (hole) concentration in the bottom 2D semiconductor is vital to achieve good electrostatics control of these Thin-TFETs. The quantum capacitance associated with the top and bottom semiconductor layers can be expressed as Eq. 6:

$$C_{Q,T(B)} = -\left[\frac{e\partial p_{T(B)}}{\partial \phi_{p,T(B)}} + \frac{e\partial n_{T(B)}}{\partial \phi_{n,T(B)}}\right] \quad (6)$$

The quantum capacitances are plotted in Fig. 3(f) under various bias conditions.

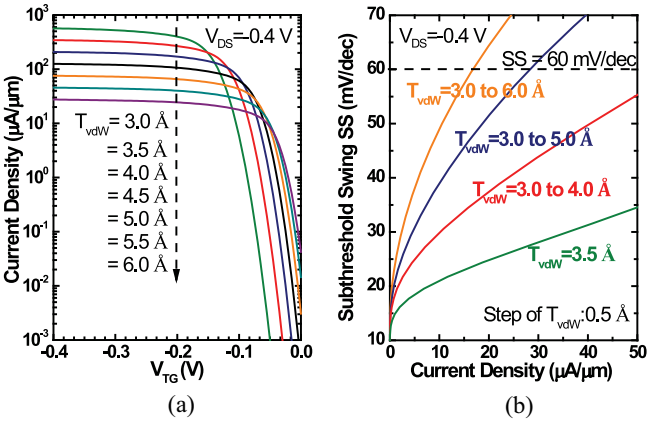

FIGURE 4. Effect of van der Waals gap thickness variation on a *p*-type Thin-TFET. (a) Tunnel current density versus V_{TG} for different van der Waals gap thicknesses T_{vdW}. (b) Differential SS versus current density assuming an evenly distributed van der Waals gap thickness T_{vdW} in the specified range.

B. EFFECTS OF NONUNIFORM VAN DER WAALS GAP THICKNESS AND ACCESS RESISTANCE

Due to the nature of van der Waals bonds, the van der Waals gap thickness is subject to intercalation of atoms/ions, interlayer rotational misalignment between 2D layers etc. For instance, in bilayer mechanically stacked Molybdenum Disulfide (MoS_2) with an interlayer twist, a maximum variation of 0.59 Å [22] was experimentally verified in the van der Waals gap thickness [22]. Surface roughening due to ripples in 2D crystals or roughness of the underlying substrates can also introduce van der Waals gap variations [23]. Meanwhile, tunneling probability is very sensitive to the tunneling distance, namely the van der Waals gap thickness in a Thin-TFET, which makes it important to investigate effects of a non-uniform van der Waals thickness. First, the Thin-TFET I-V curves are calculated by varying the van der Waals gap thickness T_{vdW} from 3.0 Å to 6.0 Å and a step of 0.5 Å (which is roughly half of the Se covalent radius [24]). The results are shown in Fig. 4(a) for a *p*-type Thin-TFET: the on current density decreases and the threshold voltage moves towards 0 when increasing the T_{vdW}. We note that, as long as the T_{vdW} is uniform, the SS remains as steep as ~14 mV/dec. However, for a non-uniform T_{vdW}, SS will degrade. To estimate its impact, an evenly distributed T_{vdW} over several ranges is used in the calculated differential SS shown in Fig. 4(b). For example, for a 2D heterojunction with an evenly distributed T_{vdW} from 3.0 Å to 5.0 Å and a step of 0.5 Å, we take the corresponding I_D-V_{TG} curve for each T_{vdW} (i.e., 3.0 Å, 3.5 Å, 4.0 Å, 4.5 Å, and 5.0 Å) shown in Fig. 4(a) and average them over the T_{vdW} range to obtain the overall I_D-V_{TG} curve for the calculation of SS. Fig. 4(b) shows that up to 1 Å variation in T_{vdW} is tolerable, resulting in a sub-60 mV/dec SS over a decent current window (up to 50 μA/μm). Depending on how Thin-TFETs are

fabricated, the T_{vdW} non-uniformity may have different distributions. Our first look at its impact in this work highlights the importance to precisely control T_{vdW}.

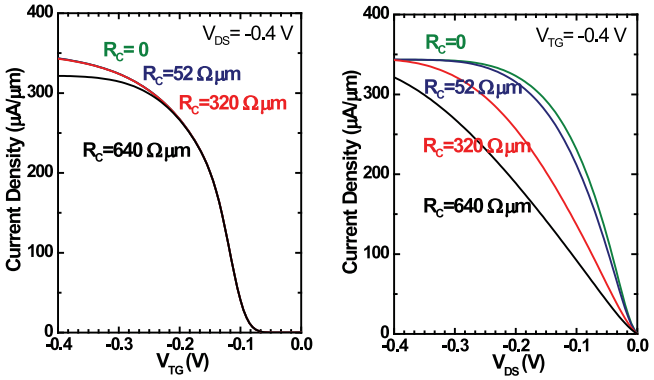

FIGURE 5. Effect of total access resistance on a *p*-type Thin-TFET. (a) I_D versus V_{TG}. (b) I_D versus V_{DS} with various total access resistance R_C values.

A finite total access resistance has a critical impact on ultrascaled transistors. To date, how to minimize the total access resistance in 2D crystal based device still remains an open question. In Fig. 5, we show its effects on Thin-TFET by assuming several values for the total access resistance R_C. At a sufficiently high $|V_{DS}|$ of 0.4 V, maximum I_D is almost the same for a R_C of up to 320 $\Omega\mu$m; a higher R_C decreases maximum I_D appreciably. Understandably, a lower R_C is necessary for a lower V_{DD}. In an ideal 2D conductor, the quantum limit of the total access resistance is inversely proportional to the square root of the carrier concentration; e.g., $\sim$52 $\Omega\mu$m for a carrier concentration of 10^{13} cm^{-2} [25]. Thus the access region of 2D semiconductors can be degenerately doped to minimize R_C.

C. CAPACITANCE EVALUATION

The gate-to-drain and gate-to-source capacitances (i.e., C_{GD}, C_{GS}) can be readily calculated from the capacitance network shown in Fig. 6.

The quantum capacitances $C_{Q,T(B)}$ of the top (bottom) 2D semiconductor are defined in Eq. 6 and indicated as the red non-linear capacitances in Fig. 6. First we define C_S as:

$$1/C_S \equiv 1/C_{vdW} + 1/(C_{Q,B} + C_{BG}) \tag{7}$$

Then, C_{GD} and C_{GS} can be written as Eqs. 8:

$$C_{GS} = \frac{C_{TG}C_S}{C_{TG} + C_{Q,T} + C_S}$$
$$C_{GD} = \frac{C_{TG}C_{Q,T}}{C_{TG} + C_{Q,T} + C_S} \tag{8}$$

Due to the symmetry in these *p*-type and *n*-type Thin-TFETs as well as the similar hole and electron effective mass in these 2D crystals, we expect similar C-V characteristics for the *p*-type and *n*-type Thin-TFETs. In Fig. 7 we plot the calculated C-V curves for the *p*-type Thin-TFETs shown in

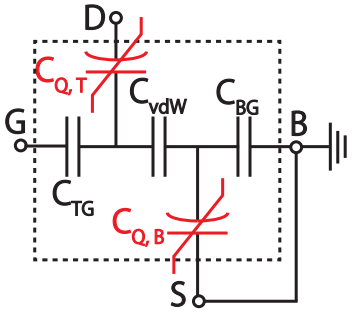

FIGURE 6. Capacitance network model of the Thin-TFET.

Fig. 2. In the linear region of the I_D-V_{DS} family of curves, C_{GD} is significant, where the drain is coupled with the top gate to modulate the tunnel current. From the linear region to the saturation region, C_{GD} drops to be near zero while C_{GS} increases to its maximum. What is worthy noting is that the magnitude of a Thin-TFET capacitance is smaller than CMOS and III-V TFET benchmarked in Section III-D for a given gate oxide EOT thus capacitances, which stem from the serially connected capacitance components as shown in Fig. 6. The capacitance model is useful for implementing the Thin-TFET into circuit simulations.

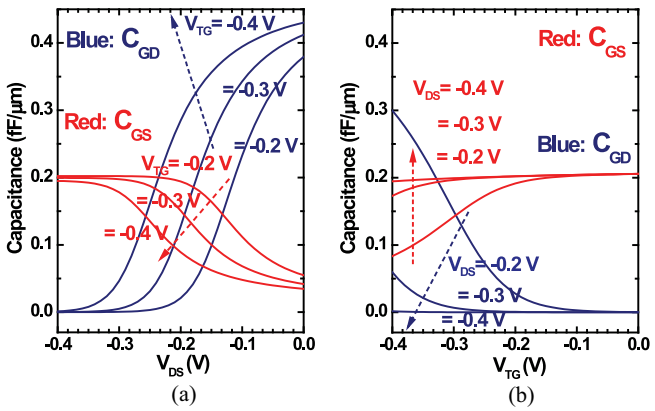

FIGURE 7. For the *p*-type Thin-TFET. (a) C_{GD} and C_{GS} versus V_{DS} at $V_{TG} = -0.2, -0.3, -0.4$ V. (b) C_{GD} and C_{GS} versus V_{TG} at $V_{DS} = -0.2, -0.3, -0.4$ V.

D. BENCHMARKING

The Semiconductor Research Corporation (SRC) Nanoelectronic Research Initiative (NRI) has supported research on beyond CMOS devices as reported by Bernstein *et al.* [26] As part of the initiative, the projected performance of the beyond-CMOS devices and the CMOS of the same technology node was compared, i.e., benchmarked. The benchmarking activity has continued by Nikonov and Young [27], [28]. Thin-TFET being proposed by us primarily under the support of SRC STARnet, we participated in the recent benchmarking using the Nikonov and Young (N&Y) methodology.

The N&Y methodology uses basic device performance parameters such as operating voltage ($V_{DD} = |V_{DS}|$), saturation current (I_{Dsat}), and average gate capacitance ($C_{G,avg}$),

to project logic switching energy and delay. The change of the net charge under the gate ($\Delta Q=q\Delta n_s$) when V_{TG} switches from 0 to V_{DD} is the sum of the change of the net charge in the top 2D semiconductor and the bottom 2D semiconductor. The average gate capacitance ($C_{G,avg}$) is defined as $\Delta Q/V_{DD}$. Here we take the *p*-type Thin-TFET as an example, I_{Dsat} and $C_{G,avg}$ are provided in Table 1 for a few V_{DD} values of 0.2, 0.3, and 0.4 V and a few total access resistance R_C values of 52 and 320 $\Omega\mu$m. The device parameters for High Performance (HP) CMOS, Low Power (LP) CMOS, InAs Homojunction TFET (HomJTFET) and InAs/GaSb Heterojunction TFET (HetJTFET) are taken from Ref. [28] and we use the same geometrical parameters for all the devices as shown in Table 1, while neglecting the contact capacitance.

The intrinsic switching delay t_{int} and the intrinsic switching energy E_{int} are calculated by [28]:

$$t_{int} = \frac{C_{G,avg}V_{DD}}{I_{Dsat}}$$
$$E_{int} = C_{G,avg}WV_{DD}^2 \quad (9)$$

In Fig. 8, we plot the projected values of t_{int} and E_{int} of the devices listed in Table 1.

TABLE 1. Benchmarking parameters.

Parameters for Thin-TFETs with various V_{DD} and R_C						
V_{DD} (V)	0.2		0.3		0.4	
R_C ($\Omega\mu$m)	52	320	52	320	52	320
I_{Dsat} (μA/μm)	263	233	325	317	349	348
ΔQ (fC/μm^2)	2.34	2.80	3.33	3.72	4.30	4.47
$\Delta n_s \times 10^{12}$(/cm^{-2})	1.46	1.75	2.08	2.32	2.69	2.79
$C_{G,avg}$ (fF/μm)	0.175	0.210	0.167	0.186	0.161	0.168
Parameters for HP/LP CMOS and HetJ/HomJ TFET [28]						
	V_{DD} (V)		I_{Dsat} (μA/μm)		$C_{G,avg}$ (fF/μm)	
HP CMOS	0.73		1805		1.29	
LP CMOS	0.3		2		1.29	
HetJTFET	0.4		500		1.04	
HomJTFET	0.2		25		1.04	
Geometrical Parameters for Benchmarking						
Half-pitch (F) (nm)	EOT (nm) (nm)		Gate Length (L) (nm)		Gate Width (W) (nm)	
15	1		15		60	

As far as the intrinsic switching energy-delay product is concerned, the Thin-TFET shows distinct energy consumption and performance advantages. For instance, Thin-TFET operation at a V_{DD} as low as 0.2 V is fast because its current is still significantly high. The most distinguishing feature of a Thin-TFET is its low intrinsic capacitance in comparison to the other devices. This advantage will be less significant when device parasitics become dominant in completed circuits.

It is observed that the Thin-TFET intrinsic switching energy-delay product moves toward the desired corner when decreasing V_{DD} from 0.4 V to 0.2 V. This is an unusual but favorable behavior for ultrascaled switches. In the case of 15 nm CMOS, I_D is roughly proportional to V_{DD}. While in the ON state of Thin-TFET, I_D has much weaker dependence on V_{TG} (see Fig. 5(a)) than CMOS, thus V_{DD} to I_D ratio actually decreases when scaling down V_{DD} from 0.4 V to 0.2 V.

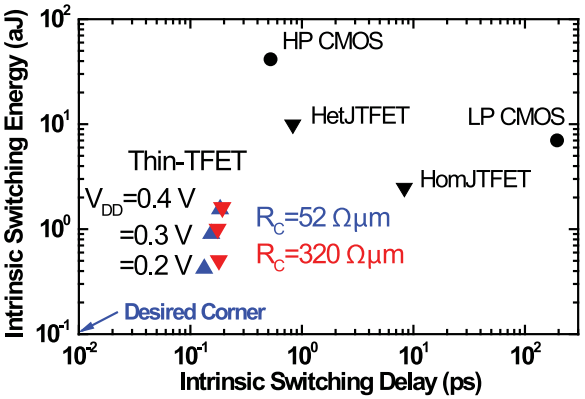

FIGURE 8. Intrinsic switching energy and delay for HP CMOS, LP CMOS, HetJTFET, HomJTFET, and Thin-TFETs with V_{DD} = 0.2, 0.3, 0.4 V, and R_C = 52, 320 $\Omega\mu$m.

Therefore, given that $C_{G,avg}$ stays roughly the same (increasing slightly with decreasing V_{DD}), the intrinsic switching time t_{int} slightly decreases when decreasing V_{DD}.

E. EXPERIMENTAL INSIGHTS

Since our proposal of Thin-TFET in 2012 [29] that is derived from our III-V TFET design [1], several key challenges have been identified along our pursuit in experimental demonstration of Thin-TFETs [30]. The foremost is the scarcity of electronic-grade layered materials and knowledge of their properties, in particular, the semiconductor heterojunctions with near broken gap alignment. The reasonably well-characterized material properties in the literature are largely based on bulk layered materials. An exponentially growing number of publications in the recent years on monolayer and few-layer materials are mainly theoretical calculations or based on exfoliation of naturally occurring crystals or synthesized by chemical vapor transport, which typically contains a few atomic percent of defects (impurities, vacancies etc). Both chemical vapor deposition and molecular beam epitaxy [31] are actively pursued by the community to grow electronic grade layered materials.

Besides lack of high quality layered materials and heterojunctions, the fabrication development of Thin-TFET is also challenging. It inherits all the fundamental fabrication challenges of a TFET including doping profile, alignment especially gate registry, gate dielectrics, ohmic contacts. Atomic layer deposition has been improved over years to achieve good quality gate dielectrics on 2D crystals [32]. Using 2D dielectrics such as hexagonal boron nitride as the gate dielectrics has also been pursued [33]. Third, low resistance ohmic contacts to 2D crystal are vital to device performance. Various techniques such as external chemical doping [34], internal chemical doping [35], electrostatic doping such as ion doping [36] and phase-engineering from the semiconductor phase to the metallic phase of a 2D crystal [37], have been implemented to reduce the contact resistances. Furthermore, Thin-TFETs demand true precision layer number control since the properties of nearly all

layered materials critically depend on the layer number when the layer number is in the range of 1-3 nm.

IV. CONCLUSION

A new tunnel transistor, Thin-TFET, has been proposed and a model material system identified. Simulations based on the transfer Hamiltonian method suggest that Thin-TFETs can achieve desired sub-threshold swing (SS) and high on-current. A uniform van der Waals gap thickness and low total access resistance are vital to optimize the Thin-TFET performance. The benchmark study shows Thin-TFETs may have distinct advantages over CMOS and III-V TFETs in term of both performance and energy consumption at low supply voltages.

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MINGDA (OSCAR) LI received the B.S. degree in microelectronics from Fudan University, Shanghai, China, and the M.S. degree in electrical engineering from the University of Notre Dame, Notre Dame, IN, USA, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree in electrical and computer engineering from Cornell University, Ithaca, NY, USA. His current research interests include tunnel field effect transistors based on 2-D materials, which includes both theoretical modeling and experimental demonstration.

DAVID ESSENI (S'98–M'00–SM'06–F'13) received the Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 1999. In 2000, he was a Visiting Scientist at Bell Laboratories, Murray Hill, NJ, USA, and in 2013, he was a Fulbright Research Scholar at the Notre Dame University, Notre Dame, IN, USA. Since 2005, he has been an Associate Professor at the University of Udine, Udine, Italy. His current research interests include the characterization, modeling, and reliability of CMOS and beyond CMOS transistors. He has served or is serving with the TPC of the IEDM, IRPS, and ESSDERC. He is an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.

JOSEPH J. NAHAS (S'62–M'69–SM'03) received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 1971. He joined the Faculty of the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN, USA, in 1971, and Bell Laboratories, Murray Hill, NJ, USA, in 1976. At Bell Laboratories, he was progressively a Technical Staff Member, a Supervisor of the Analog/Digital IC Design Group, where he was responsible for the development of the first fully functional single chip telephone. He was also the Head of the Microprocessor Design Department, in which the 32 200, CRISP, and Hobbit microprocessors were developed. In 1990, he joined the Motorola Semiconductor Product Sector (now Freescale Semiconductor), Austin, TX, USA, as a Manager of the Advanced Product Development for the High-End Microprocessor Division. At Motorola, he was the Manager of the 88 000 Microprocessor Operation, the Chief of the Semiconductor Technology Staff, and the Director of Technology Planning. In 2001, he returned to active design work, where he was a Senior Technical Staff Member and a Project Leader in the technology solutions organization with Freescale Semiconductor working on the design of magnetoresistive random access memories (MRAM). He has been an Adjunct Professor of the Computer Science and Engineering and the Electrical Engineering Departments at the University of Notre Dame, since 2008, where he worked on MRAM and other memory architectures and circuits, on circuits for implementing nanomagnetic logic, and circuits exploiting steep slope transistors. He holds 39 patents in telecommunications analog circuits and architectures, voltage references and regulators, and memory circuits and architectures. He is also a member of ACM.

DEBDEEP JENA (SM'13) received the B.Tech. degree with a major in electrical engineering and a minor in physics from the Indian Institute of Technology, Kanpur, Kanpur, India, and the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, Santa Barbara, CA, USA, in 1998 and 2003, respectively. From 2003 to 2014, he was with the Faculty of the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN, USA. He is currently a Richard Lunquist Sesquicentennial Professor of Electrical and Computer Engineering, Materials Science and Engineering at Cornell University, Ithaca, NY, USA. His current research interests include the MBE growth and device applications of quantum semiconductor heterostructures (currently, III-V nitride semiconductors), investigation of charge transport in nanostructured semiconducting materials such as graphene, nanowires, and nanocrystals, and their device applications, and in the theory of charge, heat, and spin transport in nanomaterials. He was the recipient of NSF CAREER Award, the ISCS Young Scientist Award, and the ICMBE Young Investigator Award.

HUILI GRACE XING (M'01–SM'13) received the B.S. degree in physics from Peking University, Beijing, China, the M.S. degree in material science from Lehigh University, Bethlehem, PA, USA, and the Ph.D. degree in electrical engineering from the University of California, Santa Barbara, Santa Barbara, CA, USA, in 1996, 1998, and 2003, respectively. She is currently a Richard Lunquist Sesquicentennial Professor of Electrical and Computer Engineering, Materials Science and Engineering at Cornell University, Ithaca, NY, USA. She was with the University of Notre Dame, Notre Dame, IN, USA, from 2004 to 2014. Her current research interests include the development of III-V nitride and 2-D crystal semiconductor growth, electronic, and optoelectronic devices, especially the interplay between material properties and device developments as well as high performance devices, tunnel field effect transistors, and THz applications. She was the recipient of AFOSR Young Investigator Award, the NSF CAREER Award, and the ISCS Young Scientist Award.