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Two-dimensional negative capacitance transistor with polyvinylidene fluoride-based ferroelectric polymer gating

Xudong Wang[1,2], Yan Chen[1,3], Guangjian Wu[1], Dan Li[1], Luqi Tu[1,3], Shuo Sun[1,3], Hong Shen[1,3], Tie Lin[1,3], Yongguang Xiao[2], Minghua Tang[2], Weida Hu[1,3], Lei Liao[4], Peng Zhou[5], Jinglan Sun[1,3], Xiangjian Meng[1,3], Junhao Chu[1,3] and Jianlu Wang[1,3]

Conventional field-effect transistors (FETs) are not expected to satisfy the requirements of future large integrated nanoelectronic circuits because of these circuits' ultra-high power dissipation and because the conventional FETs cannot overcome the subthreshold swing (SS) limit of 60 mV/decade. In this work, the ordinary oxide of the FET is replaced only by a ferroelectric (Fe) polymer, poly(vinylidene difluoride-trifluoroethylene) (P(VDF-TrFE)). Additionally, we employ a two-dimensional (2D) semiconductor, such as MoS_2 and $MoSe_2$, as the channel. This 2D Fe-FET achieves an ultralow SS of 24.2 mV/dec over four orders of magnitude in drain current at room temperature; this sub-60 mV/dec switching is derived from the Fe negative capacitance (NC) effect during the polarization of ferroelectric domain switching. Such 2D NC-FETs, realized by integrating of 2D semiconductors and organic ferroelectrics, provide a new approach to satisfy the requirements of next-generation low-energy-consumption integrated nanoelectronic circuits as well as the requirements of future flexible electronics.

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INTRODUCTION

The development of integrated nanoelectronic devices together with the scaling down of field-effect transistors (FETs), has rendered energy consumption a nonnegligible factor for future electronics applications. Metal–oxide–semiconductor FETs (MOSFETs), an elementary unit of integrated circuits, must be constantly improved to satisfy nanoelectronics requirements.[1,2] A key factor in this regard is the subthreshold swing (SS), which is derived from the transfer characteristics of the FET and calculated as follows,[3]

$$\begin{aligned} SS &= dV_{GS}/d(\log I_{SD}) = (dV_{GS}/d\psi_s)(d\psi_s/d(\log I_{SD})) \\ &= (1 + C_s/C_{ins})(kT/q)ln\,10, \end{aligned} \quad (1)$$

where V_{GS} is the gate voltage, I_{DS} the drain current, ψ_s the surface potential of the semiconducting channel, C_s the semiconductor capacitance, C_{ins} the gate insulator capacitance, k the Boltzmann constant, T the temperature, and q the electron unit charge. Conventional MOSFETs have a fundamental barrier due to Boltzmann statistics, which necessitate a minimum voltage of 60 mV to change the current by one order of magnitude at room temperature.[4] In recent years, numerous studies have examined various approaches to overcome this limit of 60 mV/dec.[4–8] Of these, two approaches are considered the most promising. One is the use of tunneling FET, an ambipolar device in principle that exhibits a p-type behavior with dominant hole conduction and an n-type behavior with dominant electron conduction.[4] The second is the negative capacitance FET (NC-FET), which utilizes the negative capacitance (NC) effect of ferroelectric (FE) materials,[7,8] a phenomenon wherein negative differential capacitance achieves an energy gain by changing the polarization; its physical origin has been discussed by A. K. Jonscher.[9] Especially recently, the NC effect has been increasingly investigated as it is considered one of the most promising mechanisms for overcoming the limitations of transistors.[10–14] In 2008, S. Salahuddin and S. Datta theorized a low-power nanoscale device that utilizes the ferroelectric NC effect to amplify gate voltage.[7] Continuing experiments on NC-FETs over the past 10 years have improved this device. For example, in 2008, G. A. Salvatore et al. utilized a metal–ferroelectric–insulator–semiconductor (MFIS) structure to realize a P(VDF-TrFE)-based NC-FET.[10] In 2016, J. Jo et al. achieved a P(VDF-TrFE)-based NC-FET but using a metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structure.[14] In summary, to achieve an NC-FET with an SS lower than 60 mV/dec, a composite gate dielectric is the most suitable mechanism for its structural design.

Furthermore, the semiconducting channel should be composed of a traditional semiconductor, such as silicon (Si) or germanium (Ge).[10,15] However, two-dimensional (2D) materials have been widely used in the past 10 years because of their unique physical, chemical, photoelectrical, and electrical properties.[16–19] These materials, especially 2D semiconductors, have been widely applied in FETs to substantially reduce device size and power consumption.[20–23] Thus, 2D materials are the most promising candidates for future nanoelectronic devices. For 2D FETs, however, ordinary dielectric materials, such as SiO_2, Al_2O_3, and HfO_2, are usually selected as the gate dielectric; therefore, the working principle of such 2D FETs is the same as that of a conventional FET;[21–23]

[1]National Laboratory for Infrared Physics, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, No.500 Yutian Road, 200083 Shanghai, China; [2]School of Materials Science and Engineering, Xiangtan University, 411105 Xiangtan, Hunan, China; [3]University of Chinese Academy of Sciences, No.19A Yuquan Road, 100049 Beijing, China; [4]Hunan University, School of Physics and Micro Electronics, 410082 Changsha, China and [5]Department of Microelectronics, State Key Laboratory of ASIC and System, Fudan University, 200433 Shanghai, China
Correspondence: Minghua Tang (mhtang@xtu.edu.cn) or Peng Zhou (pengzhou@fudan.edu.cn) or Jianlu Wang (jlwang@mail.sitp.ac.cn)
Xudong Wang and Yan Chen contributed equally to this work.

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accordingly, the SS limit (60 mV/dec) persists, hindering further reduction in power consumption. Therefore, the objective of this study was to incorporate ferroelectric materials possessing the NC effect in 2D materials in order to achieve a ferroelectric/2D FET (Fe2DFET) with ultralow SS and power consumption (hereafter referred to as a 2D NC-FET). Several earlier studies have reported on the combination of ferroelectrics and 2D materials, but most applications have been in memory devices and photodetectors.[18,24–28] In addition, F. A. McGuire et al. achieved an Fe2DFET with a sub-60 mV/dec SS, but their device was based on the MFMIS structure.[29] In addition to poly(vinylidene difluoride-trifluoroethylene) (P(VDF-TrFE)), hafnium zirconium oxide (HZO) has recently emerged as an environmentally friendly ferroelectric material. M. Si et al. and F. A. McGuire et al. combined HZO and molybdenum disulfide (MoS_2) to obtain the 2D NC-FETs that provide the advantages of low voltage and power consumption.[30,31] Although they selected the same materials, they obtained 2D NC-FETs with different structures, namely MFIS and MFMIS. The standard structure of NC-FETs, especially 2D NC-FETs, is not clear yet. Moreover, the interaction between ferroelectrics and 2D materials has not been adequately investigated theoretically or experimentally. These are topics that warrant comprehensive investigation.

In this work, we realize a 2D NC-FET based on the metal–ferroelectric–semiconductor (MFS) structure, in which the ordinary oxide of the FET is replaced only by a FE polymer, P(VDF-TrFE). We employ a 2D semiconductor, such as MoS_2 and molybdenum diselenide ($MoSe_2$), as the channel. This 2D NC-FET achieved an ultralow SS of 24.2 mV/dec over four orders of magnitude in drain current at ultralow drain voltage (0.1 V) and room temperature. Moreover, we comprehensively investigated the thickness of ferroelectrics in these 2D NC-FETs, and an SS of 51.2 mV/dec over one decade was obtained even when the P(VDF-TrFE) thickness was reduced to 50 nm. Furthermore, we clarify the NC effect in the developed 2D NC-FETs on the basis of the Landau theory. For comparison, we prepared MFMIS- and MFIS-based Fe2DFETs. The experimental results showed that none of the MFMIS and MFIS devices could obtain a sub-60 mV/dec SS, meaning that these two types of devices cannot fully exploit the NC effect of P(VDF-TrFE) in 2D NC-FETs. Therefore, this work presents a stable 2D NC-FET gated only by a ferroelectric polymer layer; the MFS-based 2D NC-FET not only maximizes the NC effect of P(VDF-TrFE) but also has a simplified device structure. The developed device has potential for applications in future nanoelectronic devices requiring ultralow power consumption and fast switching.

RESULTS AND DISCUSSION

NC effect is a transient and unstable phenomenon; nevertheless, its occurrence in ferroelectric materials has been verified.[7,9] The NC effect was first observed in 2014 by A. I. Khan et al. in a ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ capacitor based on the voltage pulse method.[32] The NC effect of ferroelectric materials employed as the gate dielectric in FETs should improve device performance, for example, by reducing the operating voltage and accelerating the switching rate.[7,12,33] The switching rate and power consumption of FETs depend completely on the scale of the SS used to measure the gate voltage increment required to change the drain current by one order of magnitude. SS can be calculated using equation (1), in which the term $1 + C_s/C_{ins}$ is referred to as the m factor:

$$m = 1 + C_s/C_{ins}. \quad (2)$$

In equation (1), $(kT/q) \times \ln 10$ is a constant equaling 60 mV/dec at 300 K. Thus, in a conventional FET, the SS limit is 60 mV/dec because C_S and C_{ins} are always positive, that is $m > 1$, a phenomenon known as the Boltzmann tyranny. However, when a ferroelectric material is used as the gate dielectric in FETs, C_{ins} can become negative because of its NC characteristic. Accordingly, if $C_{ins} < 0$ in equation (2), then $m < 1$, and the SS will likely be less than 60 mV/dec at room temperature.

Numerous studies have focused on optimizing the performance of NC-FETs. These studies have mostly used one of the following three device structures: (1) MFMIS, (2) MFIS, and (3) MFS.[10,12,34,35] The NC effect is a dynamic state that occurs when the polarized electric field switches from one stable state to another,[7,12,32] which renders difficult the direct measurement of the NC in a ferroelectric capacitor. Therefore, researchers usually connect a dielectric capacitor in series with a ferroelectric capacitor to neutralize this instability. In this composite configuration, the total capacitance is stable and positive and larger than the capacitance of an ordinary capacitor. Therefore, in both MFMIS and MFIS devices, the insulation layer can act as an ordinary capacitor stabilizing the NC effect of the ferroelectric layer. Specifically, in an MFMIS device, the role of the interlayer metal between the ferroelectric and insulation is mainly to eliminate the leakage current between the ferroelectric and substrate.[12] Furthermore, the interlayer metal provides an equipotential surface as a floating gate, thus enabling the treatment of the ferroelectric and the underlying MOSFET as two separate circuit entities connected by a wire.[36] Without this interlayer metal, an MFIS device can be achieved only if a ferroelectric and an insulation composite film are used as the gate dielectric. However, without the interlayer metal, the insulation in an MFIS device also serves to stabilize the NC effect of the ferroelectric material and shield against gate leakage current.[37] G. Pahwa et al. compared MFMIS-based and MFIS-based devices with theoretical models and reported that the MFIS device exhibits a higher ON current and a steeper SS than does the MFMIS device.[36]

To modulate the semiconductor channel in a conventional MFS FET, we could replace the gate dielectric with only a ferroelectric layer. As argued by S. Salahuddin and S. Datta, who first proposed the concept of NC-FET in 2008, if a ferroelectric replaced the ordinary insulator in a MOSFET, the electrostatic potential ψ_s at the ferroelectric–semiconductor interface would exceed the external gate voltage (V_{GS}) because of the NC effect of the ferroelectric;[7] in this approach, the device structure (MFS) does not change. Although diverse materials are used for the ferroelectric and channel semiconductors in NC-FETs, the devices based on these three structures, namely MFMIS, MFIS, and MFS, all have high potential to facilitate the NC effect of ferroelectric materials, effectively improving FET performance. The NC effect has been confirmed in ferroelectric materials, but the device structure of NC-FETs remains to be standardized for different materials, especially in the case of integration with 2D materials, which is a recent and growing trend. Therefore, in this study, we prepared, tested, and comprehensively investigated a large number of devices with the aforementioned three structures. The experimental results indicated that only the MFS-based device fully utilizes the NC effect of the ferroelectric materials.

Fig. 1a is a schematic of the MFS-based 2D NC-FET, in which MoS_2 is used as the semiconducting channel and P(VDF-TrFE) thin film with a molar ratio of 70%/30% is used as the ferroelectric gate dielectric. Figure 1b shows optical microscope images captured at three stages in the fabrication process. The configuration of the MFS structure was confirmed through transmission electron microscopy (TEM) (Fig. 1c). In this study, all MoS_2 films selected for fabricating the semiconducting channel were a few (approximately four) layers thick; this was confirmed through Raman spectroscopy (Fig. 1d) and atomic force microscopy (AFM) (Fig. 1e). The technological and experimental details are summarized in the "methods" section. The present section details and discusses the experimental results for the MFS-based 2D NC-FET and examines the working principle of the device and the mechanism of the NC effect on the basis of the Landau theory. We carefully studied the effect of ferroelectric thickness on device performance when using

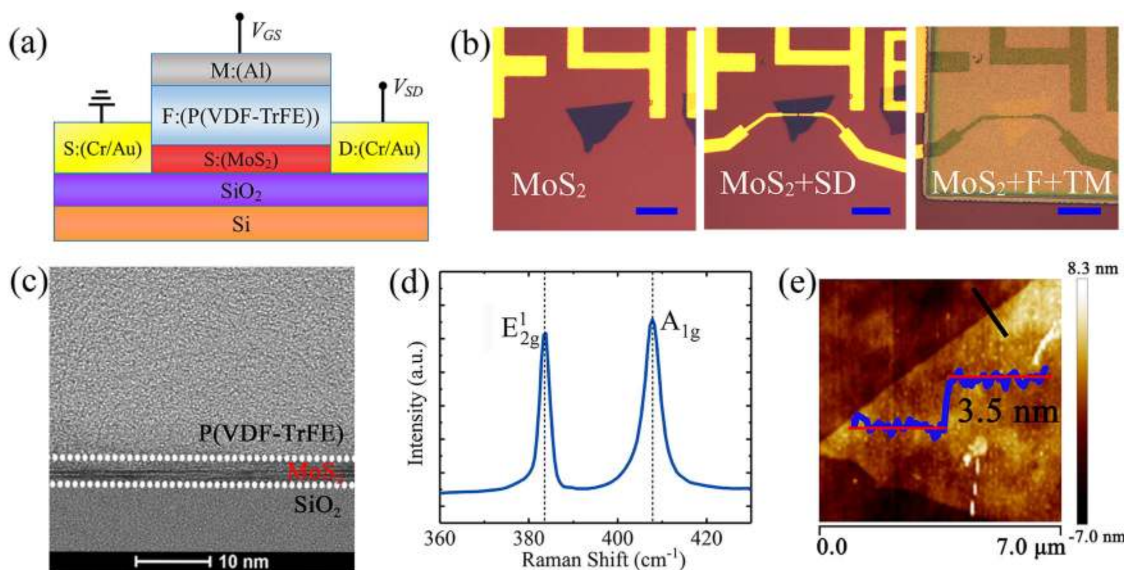

Fig. 1 **a** 2D structure schematic of a 2D NC-FET based on the MFS structure, with P(VDF-TrFE) employed as the ferroelectric layer and MoS_2 as the 2D semiconductor channel. **b** Optical microscope images of a 2D NC-FET at different process stages; all scale bars (blue) are 20 μm. **c** Cross-sectional TEM image of a 2D NC-FET showing layered MoS_2 (≈4 layers). **d** Raman spectra of MoS_2 used in this device; the two peaks at $E_{2g}{}^1 = 383.84\ cm^{-1}$ and $A_{1g} = 407.79\ cm^{-1}$ indicate the four layers. **e** AFM height image of the MoS_2. The cross-section along the black line shows a height of 3.5 nm, reflecting the four MoS_2 layers

MoS_2 as the semiconducting channel and $MoSe_2$ as the auxiliary. For comparison, MFMIS and MFIS Fe2DFETs were prepared. All measurements were conducted in an atmospheric environment and at room temperature, and all drain biases (V_{SD}) were set to 0.1 V to ensure ultralow power consumption.

For the MFS-based 2D NC-FET, we investigated the device with an MoS_2 channel, which featured strong semiconducting properties.[21] In this case, the P(VDF-TrFE) thickness was varied from 50 to 300 nm; the corresponding transfer curves are plotted in Fig. 2a, where all transfer curves are counterclockwise; an SS of 24.2 mV/dec over four orders of magnitude was achieved at the left side of the transfer curve for the 300-nm P(VDF-TrFE). Because of the direct contact between P(VDF-TrFE) and MoS_2, the carriers and the band of the MoS_2 channel can be fully controlled by the polarized electric field. Moreover, the coercive voltage is strongly correlated to and thus increases with P(VDF-TrFE) thickness.[38] Hence, the threshold voltage of the 2D NC-FET is heavily dependent on the coercive voltage of P(VDF-TrFE), and the counterclockwise hysteresis window in the transfer curves widen with increase in P(VDF-TrFE) thickness (Fig. 2a). For improved image clarity and for analysis of the SS characteristics, the left subthreshold regions of these four transfer curves are extracted and presented in Fig. 2b. Clearly, the 2D NC-FET with the 300-nm P(VDF-TrFE) achieved the lowest SS of 24.2 mV/dec over 4 decades. As the thickness of P (VDF-TrFE) decreased, its SS deteriorated; nevertheless, SS = 29.6 mV/dec over 3 decades for the 200-nm P(VDF-TrFE), SS = 33.1 mV/dec over 2 decades for the 100-nm P(VDF-TrFE), and SS = 51.2 mV/dec over 1 decade for the 50-nm P(VDF-TrFE), all of which exceeded the limit of 60 mV/dec.

The schematic of the 2D NC-FET and the corresponding voltage divider are shown in Fig. 2c. Per the Landau theory, for $BaTiO_3$, the surface potential of the semiconducting channel (ψ_s) can be amplified by the NC effect of the ferroelectric, which is larger than the external gate voltage (V_{GS}); moreover, the ψ_s/V_{GS} ratio increases with ferroelectric thickness.[7] Therefore, these sub-60 mV/dec SSs of the 2D NC-FETs can be completely attributed to the NC effect of P(VDF-TrFE). As explained earlier, the NC effect occurs when the polarization reverses, which is driven by the external gate voltage. Because the MoS_2 used in this study is an n-type semiconductor, sub-60 mV/dec SSs can be achieved on only one side (always the left side) of the transfer curves. This phenomenon can be explained on the basis of band theory.[39,40] When the P (VDF-TrFE) is polarized downward (left panel, Fig. 2d), the electrons in the MoS_2 are engaged to compensate for the polarization charges. Because the Fermi level of MoS_2 is increased to reduce the difference in the work function levels of source and drain electrodes (ψ_D), and electrons are the majority carriers in MoS_2, which maintain the drain current at a high level, MoS_2 can fully compensate the downward polarization field. In addition, the top-gate aluminum (Al) is a metal and can compensate completely for the polarization charges; this enables a steady state before reversing polarization orientation. As long as the external gate voltage does not exceed its negative coercive field, the drain current remains at a high level because the electrons in MoS_2 are bounded by the internal electric field (i.e., poling field). When the external gate voltage slightly exceeds the negative coercive voltage, the polarization direction suddenly changes from downward to upward; simultaneously, the compensation charges in the MoS_2 are instantly converted from electrons to holes. In other words, the Fermi level of MoS_2 is rapidly decreased as the polarization orientation shifts from downward to upward; in addition, and ψ_D increases, hindering the movement of electrodes, at which time the drain current abruptly alters from the ON state to the OFF state, resulting in an ultrasteep SS.

Holes, the minority carriers in MoS_2, cannot completely compensate for the upward polarized electric field (right panel, Fig. 2d). When the external gate voltage is swept from negative to positive (to less than the positive coercive voltage), the carrier concentration in the MoS_2 channel is simultaneously modulated by the external and internal electric fields, which have opposing effects: the upward internal field bounds the holes and tends to maintain the low Fermi level of MoS_2; by contrast, although the negative external gate voltage also induces holes and lowers the Fermi level of MoS_2, the hole concentration declines and the Fermi level increases as the external gate voltage changes from a negative value to zero. When the external gate voltage exceeds zero, electrons are induced in the MoS_2, and the Fermi level increases more easily, which increases the drain current; this phenomenon is completely opposite to that of the internal field. Because the hole concentration in MoS_2 is insufficient to

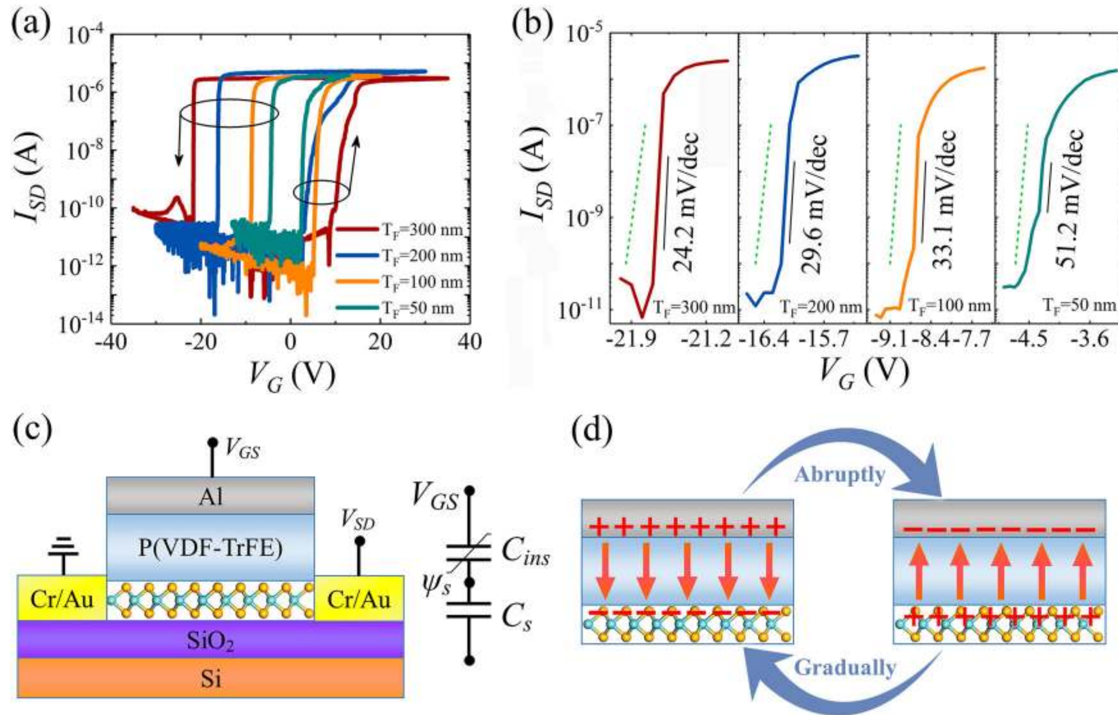

Fig. 2 **a** Transfer curves of 2D NC-FETs based on the MFS structure with MoS_2 channel and P(VDF-TrFE) of different thicknesses (50, 100, 200, and 300 nm). All transfer curves are counterclockwise, and the hysteresis window reduces with decrease in P(VDF-TrFE) thickness. In these measurements, all V_{SD} was set to 0.1 V. **b** Extracted curves of the left side of each transfer curve in **a**. The dotted green line is a datum line of the limit of SS = 60 mV/dec for a conventional MOSFET. The lowest SS = 24.2 mV/dec over 4 decades was achieved at a P(VDF-TrFE) thickness of 300 nm. For a P(VDF-TrFE) thickness of 50 nm, SS = 51.2 mV/dec over 1 decade, which is lower than 60 mV/dec. **c** Schematic of the 2D NC-FET with P(VDF-TrFE) as the gate dielectric and MoS_2 as the channel. The right panel shows the equivalent capacitive divider of the gate voltage. **d** Simplified diagram of the 2D NC-FET work processes showing cyclical switching form one state to another. P(VDF-TrFE) polarization reverses from downward to upward abruptly, but the converse change in polarization is gradual

compensate for the upward internal field, especially in the positive external gate voltage range, the drain current increases slowly as the external gate voltage is swept from zero to positive; consequently, the SS is considerably higher than 60 mV/dec. In sum, over the entire work process, the 2D NC-FET switches from the ON state to the OFF state and then back to the ON state cyclically (Fig. 2d), wherein the ON–OFF switching is abrupt and the OFF–ON switching is gradual.

For comparison, the experimental results of the MFMIS-based and MFIS-based Fe2DFETs are presented in Supplementary Information Part 1. None of the MFMIS and MFIS Fe2DFETs could obtain a sub-60 mV/dec SS. This is due to the interlayer metal and the insulator layer in these devices partly shield the polarization effect of P(VDF-TrFE) on the MoS_2 channel, and without the constraint of polarized charge on the carriers in the MoS_2 channel, the voltage amplified by the NC effect of P(VDF-TrFE) cannot act on the MoS_2 channel. Therefore, devices based on these two structures cannot be used to fabricate FETs with ultralow power consumption. Accordingly, we conclude that MFMIS and MFIS structures are unsuitable for fabricating 2D NC-FETs.

The key operating principle of 2D NC-FETs is determined by the nonlinear polarization (P)–electric field (E) relationship of the ferroelectric insulator.[41] Therefore, it is necessary to affirm whether the P(VDF-TrFE) used in the 2D NC-FET experiences the NC effect. To this end, a series of Al-P(VDF-TrFE)-Au capacitors with different P(VDF-TrFE) thicknesses were prepared and their P–V and P–E relationships were measured. The P–V curves (Fig. 3a) clarify that the coercive voltage is strongly correlated to and increases with the P(VDF-TrFE) thickness. Then, by converting the voltage into the electric field by using $E = V/t$, where t is the P(VDF-TrFE) thickness, the P–E curves can be derived (solid lines, Fig. 3b). From these experimental P–E curves, we carefully derived the P–E relationship for P(VDF-TrFE) by using the Landau–Khalatnikov (LK) equation to confirm its NC characteristic. The LK equation is the most advanced approach for modeling the dynamic characteristics of ferroelectric materials[7] and can be expressed as follows:

$$\delta(dP/dt) = -(\partial G/\partial P) \tag{3}$$

where G is Gibbs free energy, P the polarization of the ferroelectric insulator, t the thickness of the ferroelectric layer, and δ a temperature independent parameter.[42] G can be calculated as

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \tag{4}$$

where α is a temperature dependent parameter, β and γ are assumed to be independent of the temperature[42] and E is the electric field applied on the ferroelectric capacitor. The P–E relationship can be derived from equations (3) and (4):

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \delta(\mathrm{d}P/\mathrm{d}t) \tag{5}$$

From the experimental P–E curves, the material parameter α, β, and γ for P(VDF-TrFE) with different thicknesses were extracted through fitting with equation (5) (dotted line, Fig. 3b). We assumed that $\mathrm{d}P/\mathrm{d}t = 0$. The Landau coefficients for P(VDF-TrFE) with different thicknesses are displayed in Table 1. Figure 3b shows that there is a negative differential capacitance in each curve, meaning that P(VDF-TrFE) does have the NC effect. However, in the case of the Al-P(VDF-TrFE)-Au capacitor, the NC effect weakened with reduction in P(VDF-TrFE) thickness. This characteristic is consistent with the electrical results obtained for the proposed 2D NC-FETs. Hence, electrode material is a crucial parameter that must be considered in the further development of 2D NC-FETs.

The SS for all devices in all experiments were extracted and analyzed. The result show that none of the MFMIS and MFIS

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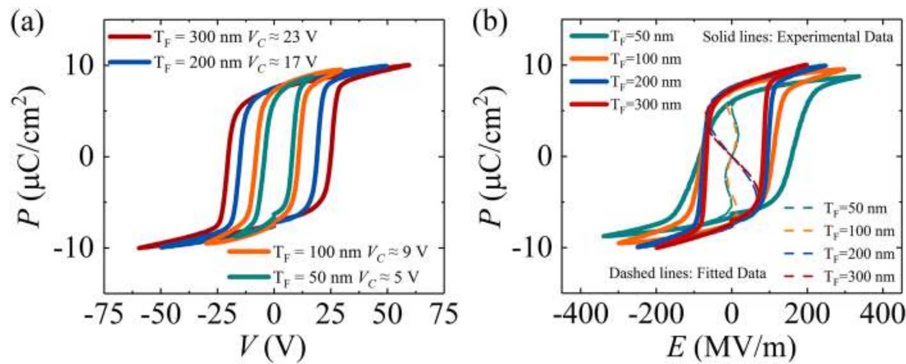

Fig. 3 **a**, Hysteresis loops of a series of Al-P(VDF-TrFE)-Au capacitors with 50, 100, 200, and 300-nm P(VDF-TrFE). The coercive voltage of P(VDF-TrFE) significantly reduces with P(VDF-TrFE) thickness, but its polarization intensity is almost constant. **b**, Polarization vs. electric filed for P(VDF-TrFE) of thickness 300, 200, 100, and 50 nm. The solid lines are experimental data and the dotted lines are calculated using the LK equation

Table 1. Landau coefficients for P(VDF-TrFE) with different thicknesses

P(VDF-TrFE) thickness (nm)	α (m/F)	β ($m^5/F/C^2$)	γ ($m^9/F/C^4$)
300	-3.8×10^{8}	1.3×10^{10}	-4.9×10^{10}
200	-2.1×10^{8}	3.9×10^{9}	1.5×10^{11}
100	4.4×10^{7}	-5.5×10^{9}	3.3×10^{11}
50	2.9×10^{7}	-3.6×10^{9}	2.6×10^{11}

devices achieved a sub-60 mV/dec SS, whereas most of the MFS devices achieved an ultralow SS much lower than 60 mV/dec. Furthermore, the 2D NC-FETs based on the MFS structure with an $MoSe_2$ channel exhibited the lowest SS of 24.3 mV/dec over 4 decades (Supplementary Information Part 2). Therefore, the NC effect of P(VDF-TrFE) manifests in MFS-based devices with a transition metal dichalcogenide channel. However, the NC effect is generally unstable unless an ordinary capacitor is connected in series.[7,32] To understand why the proposed MFS-based device can be used to fabricate a 2D NC-FET, we measured the capacitance of a series of Al-P(VDF-TrFE)-Au–based capacitors of area 1×10^4 μm^2 with different P(VDF-TrFE) thicknesses. According to the capacitance series model, the total capacitance can be expressed as

$$C^{-1}=C_i^{-1}+C_f^{-1}, \tag{6}$$

where C is the total capacitance of the entire capacitor, C_i is the interface capacitance, and C_f is the ferroelectric capacitance. The reciprocal of capacitance (C^{-1}) varies linearly with P(VDF-TrFE) thickness.[43] After linear fitting using equation (6), we found that a fixed capacitance of approximately 5.5 nF persists even when the P(VDF-TrFE) thickness is reduced to zero (Fig. 4a). Therefore, we hypothesized that a dead layer exists at the interface between Al and P(VDF-TrFE);[44–46] TEM (inset, Fig. 4a) confirmed this hypothesis: specifically, AlF_3 was found directly between Al and P(VDF-TrFE), but no contact was observed between P(VDF-TrFE) and other metals such as silver (Ag), gold (Au), and cooper (Cu).[45,47] In this case, the AlF_3 layer served as an ordinary capacitor, resulting in a stable MFS-based 2D NC-FET.

The SSs of most 2D NC-FETs based on the MFS structure were less than 60 mV/dec (Fig. 4b). Each point in Fig. 4b originates from the transfer curves shown in Supplementary Information Part 3. Moreover, Fig. 4b clarifies that the SS significantly declines as the thickness of P(VDF-TrFE) is rduced to 50 nm, because polarization intensity is independent of P(VDF-TrFE) thickness but depends on film crystallinity, which in turn is dependent on the preparation method.[38] Therefore, this reduction in SS is mainly due to technological limitations as well as the choice of the top-gate metal, which strongly influences the capacitance of the dead layer. Our group has been able to maturely prepare ultrathin P(VDF-TrFE) films with excellent ferroelectricity by using the Langmuir–Blodgett method,[48] but its integration with 2D NC-FETs requires further study. Because both the coercive voltage of P(VDF-TrFE) (Fig. 2a) and threshold voltage of 2D NC-FET (Fig. 3a) are strongly dependent on the P(VDF-TrFE) thickness. Therefore, further scaling the P(VDF-TrFE) thickness can narrow the hysteresis window and reduce the sweeping range of the gate voltage, which in turn reduces the power consumption.

In conclusion, we demonstrated an n-type NC-FET with a 2D channel whose gate dielectric is only a ferroelectric polymer film without any other complex structure. This 2D NC-FET exhibits an ultralow SS of 24.2 mV/dec over four orders of magnitude in drain current at room temperature. Sub-60 mV/dec switching was achieved for ferroelectric P(VDF-TrFE) layers of various thicknesses. Additionally, the mechanism of the NC effect of P(VDF-TrFE) was clarified using the Landau theory. This study provides a new methodology to adapt to the demands of next-generation low-energy-consumption integrated nano/flexible electronic applications.

METHODS

High-quality MoS_2 or $MoSe_2$ nanosheets were fabricated through mechanical exfoliation using bulk crystals (2D semiconductor, Inc.) and transferred to a substrate composed of heavily doped p-type Si and 280 nm SiO_2. The few-layer MoS_2 or $MoSe_2$ was screened under a microscope and its coordinates marked for electron beam exposure (EBL). Design CAD was used to draw the desired electrodes in the exposure range. Next, methyl methacrylate and poly(methyl methacrylate) were sequentially spin-coated onto the substrate. The source and drain electrodes were thus prepared using the EBL method followed by thermal evaporation and lift off. Here, Cr/Au (10 nm/50 nm) was deposited through thermal evaporation with a vacuum degree of less than 1×10^{-3} Pa to form the source and drain metal electrodes to ensure good Ohmic contact between the electrodes and the MoS_2 or $MoSe_2$ channel. Subsequently, the devices were annealed at 200 °C for 2 h in a vacuum chamber with 100 sccm argon (Ar) to remove the residual and to improve the Ohmic contact between source/drain and the MoS_2 or $MoSe_2$ channel. For MFMIS and MFIS devices, HfO_2 (10 and 15 nm) was prepared through atomic layer deposition in a vacuum chamber at 95 °C. The interlayer metal Cr/Au (8 nm/16 nm) in MFMIS devices was also fabricated through the EBL method. P(VDF-TrFE) thin film with a molar ratio of 70%/30% was dissolved in 2.5%wt diethyl carbonate. Then, P(VDF-TrFE) films were prepared through spin-coating of the substrates under atmospheric conditions. Per our experience, in the spin-coating of P(VDF-TrFE), a thickness of 50 nm per layer can be obtained at 3000 rpm in 20 s. Cyclic spin-coating yielded a P(VDF-TrFE) film with the target thickness, which was annealed at 115 °C for 10 min per layer to evaporate the solvent in an annealing furnace under atmospheric conditions. After the final layer was spin-coated, the P(VDF-TrFE) films

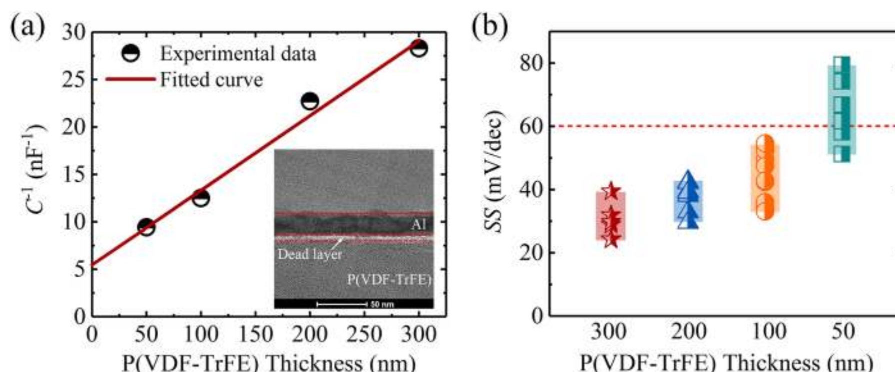

Fig. 4 **a** Linearity of the reciprocal capacitance vs. the P(VDF-TrFE) thickness. Semisolid circles show the experimental data, and the red line is the fitted curve. Inset shows a cross-sectional TEM image of the interface between Al and P(VDF-TrFE); a dead layer can be seen at the interface. Scale bar = 50 nm. **b** SS statistics for 2D NC-FET based on the MFS structure with different P(VDF-TrFE) thicknesses

were annealed at 135 °C for 4 h to enhance their crystallinity. Top-gate electrode aluminum film (Al; 35 nm) was fabricated through thermal evaporation with a vacuum degree of less than 1×10^{-4} Pa, and then patterned through negative photoresist ultraviolet photolithography and argon ion etching. Finally, the residual negative photoresist on the top gate was removed through oxygen (O_2) plasma etching.

In this work, all electric measurements were performed under ambient conditions and at room temperature. Electrical characterizations were performed using the Lake Shore probe station and an Agilent B2902A Semiconductor parameter analyzer. The hysteresis loops were measured using a Radiant Precision LC materials analyzer, and the capacitance of the Al-P(VDF-TrFE)-Au capacitor was measured using an Agilent E4980A precision LCR meter. TEM data was obtained at Dongguan Xinke Technology Research and Development Co., Ltd. Materials Science Laboratory.

Data availability

The data that support the findings of this study are available upon the request from the Corresponding Author.

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AUTHOR CONTRIBUTIONS

J.W., P.Z. and M.T. conceived and supervised the research. X.W. and Y.C. fabricated the devices and carried out the measurements. X.W., J.W., W.H., S.S., H.S., T.L., J.S. and X.M. performed the data analysis. X.W., J.W. and T.L. carried out the calculation of negative effect of P(VDF-TrFE). X.W. and J.W. co-wrote the paper. All authors discussed the results and revised the manuscript.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-017-0040-4).

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