Two-Klystron Binary Pulse Compression at SLAC*

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Abstract

The Binary Pulse Compression system installed at SLAC was tested using two klystrons, one with 10 MW and the other with 34 MW output. By compressing 560-ns klystron pulses into 70 ns, the measured BPC output was 175 MW, limited by the available power from the two klystrons. This output was used to provide 100-MW input to a 30-cell X-band structure in which a 100-MV/m gradient was obtained. This system, using the higher klystron outputs expected in the future has the potential to deliver the 350 MW needed to obtain 100 MV/m gradients in the 1.8-m NLC prototype structure. This note describes the timing, triggering, and phase coding used in the two-klystron experiment, and the expected and measured network response to three- or two-stage modulation.

INTRODUCTION

The Binary Pulse Compression (BPC) system [1] consists of a BPC network and its appropriately modulated drive. A BPC network consists of one or more stages. Each stage consists of a hybrid whose two isolated ports are used as inputs and the remaining two ports as outputs with one output port followed by a delay line. The delays decrease in a binary fashion, with the last delay equal to the output pulse width.

Because more klystrons became available, the one-klystron BPC [2] was converted into the standard two-klystron, BPC system. The systen consists of a 3-stage BPC network, followed by a combiner, with its klystron drive and its load, and is shown in Fig. 1.

If, and only if, the two input powers are equal, does a switchable π phase-shift (PSK) direct all of the input powers into one or into the other output port of each hybrid. But, as we shall now show, the deviation from this ideal is small even for large input power ratios. Using superposition and energy conservation one can show that the two output powers of a hybrid in terms of its two input powers are

$$P_{oa} = \frac{P_{ia}}{2} + \frac{P_{ib}}{2} + \sqrt{P_{ia}P_{ib}}\cos\phi \ . \tag{1}$$

$$P_{ob} = \frac{P_{ia}}{2} + \frac{P_{ib}}{2} - \sqrt{P_{ia}P_{ib}}\cos\phi \ . \tag{2}$$

Here, ϕ is the phase difference between the input fields. We adjust the phase shifters so that $\phi = 0.0°$. Then

$$P_{oa} = \left[\sqrt{\frac{P_{ia}}{2}} + \sqrt{\frac{P_{ib}}{2}}\right]^2, \quad P_{ob} = \left[\sqrt{\frac{P_{ia}}{2}} - \sqrt{\frac{P_{ib}}{2}}\right]^2 \ . \tag{3}$$
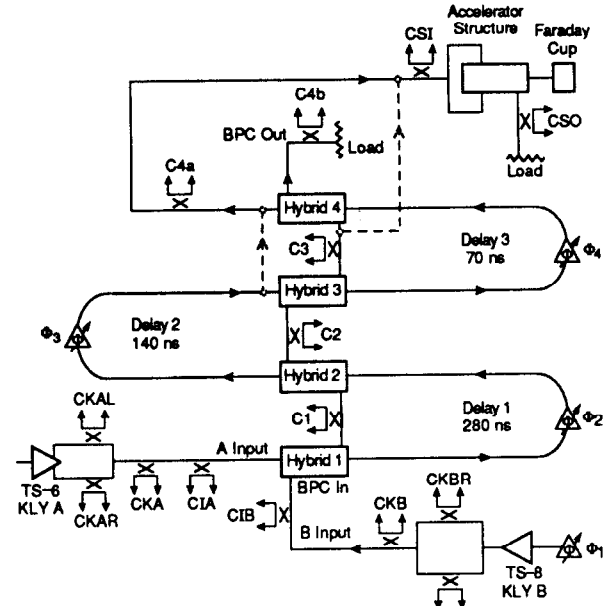

Figure 1. BPC network with its klystron drive and accelerator structure load.
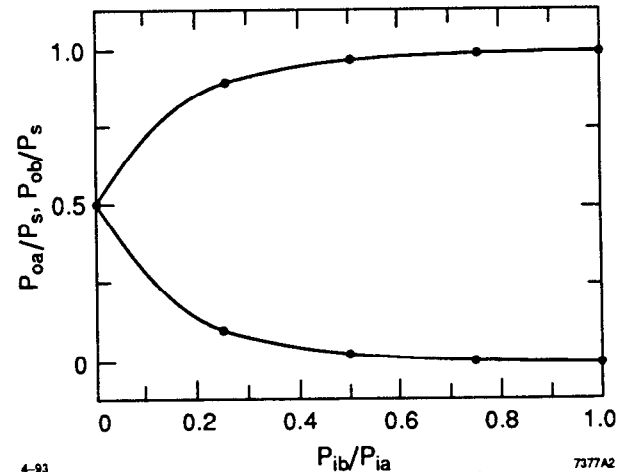

Figure 2. Normalized output powers vs. input power ratio.

Let $x = P_{ib}/P_{ia}$ and $P_s = P_{ia} + P_{ib}$, then

$$P_{oa}/P_s = \frac{[1 + \sqrt{x}]^2}{2(1 + x)}, \qquad P_{ob}/P_s = \frac{[1 - \sqrt{x}]^2}{2(1 + x)} \ . \tag{4}$$

If we switch to $\phi = 180°$, then the roles of outputs A and B are reversed. The normalized output powers as a function of the ratio of the input powers are plotted in Fig. 2. An input power ratio of 3:4, reduces the output by 0.5% and a ratio of 1:4 reduces the output by 10%.

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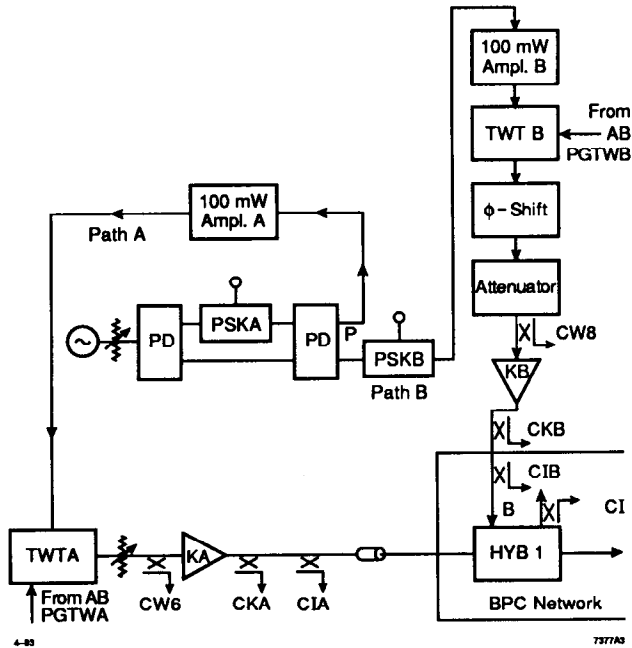
Figure 3. Two-klystron BPC drive system.

Figure 4. Timing and triggering.

Figure 5. Three-stage BPC modulation (horizontal unit = 70 ns.)

TIMING AND PHASE CODING

The Two-Klystron BPC drive system is shown in Fig. 3. The output pulses from the two klystrons and the modulation transitions must arrive simultaneously at the two inputs to hybrid 1, which are also the inputs to the BPC network. Thus the time delay of the two paths of the RF leaving the PSK modulator, path A and path B, shown in Fig. 3, must be equal. The modulation of PSK A traverses both paths, and, therefore, it was used to adjust the delay of the two paths to make then equal to each other. It was accomplished as follows. A phase transition was applied to PSK A and the detected pulse was monitored at the output C1 of hybrid 1. With klystron B turned on, the position of the phase transition, as indicated by its "marker" on the scope, was noted. Then klystron B was turned off and klystron A was turned on. Again the position of the "marker" was noted. The delay of this marker from its previous position was the delay, in the form of WR90 waveguide, added to path A. If both klystrons are on then both markers will appear and will coincide when Path A and path B time delays are equal.

The triggers and pulses for the Two-Klystron BPC were provided by the five Stanford Research System pulse generators **PGMB, PGTWB, PGC, PGMA, and PGTWA**. Their timing are shown in Fig. 4. To prevent jitter all pulse generators are triggered about 70 μs before the modulators are triggered. PGMB provides the clock pulse T_o (the big bang) and turns on modulator B. PGTWB provides the 600 ns pulse that turns on TW amplifier B. PGC outputs AB and CD provide the two 70 ns pulses for PSK A and output B provides the phase transition for PSK B. PGTWA provides the 600 ns pulse that turns on TW amplifier A. PGMA turns on modulator A.
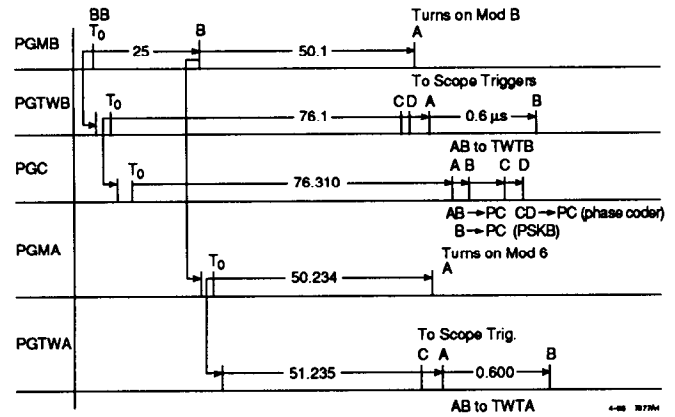
THREE-STAGE BPC

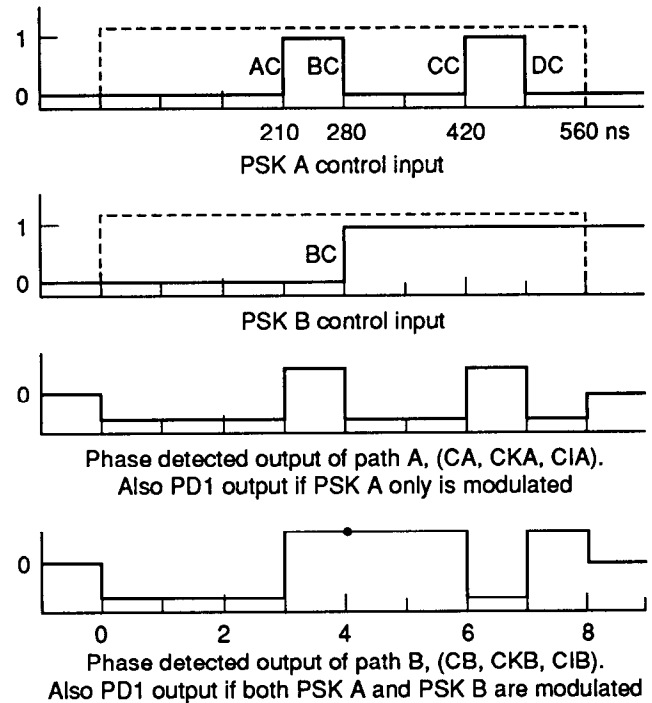The coding for a 3-stage BPC provided by the pulse generators and the resulting phase detected waveforms are shown in Figure 5. We now have a 3-stage BPC followed by a combiner. The time delay of the last delay line, and hence the duration of the output pulse, is 70 ns. The experimentally obtained outputs are shown in Fig. 6. The amplitude and phase of the combiner output pulse are shown in Fig. 7. The power was increased over several weeks, as the various compenents underwent RF proccessing, untill the 3-Stage BPC plus combiner provided $\approx$ 175 MW, 50 μs flat-top output pulse. This output was fed into the 30 cavity accelerator where it was used to study dark current in the section at up to 100 MV/m accelerating gradients. This is reported on at this conference [3].
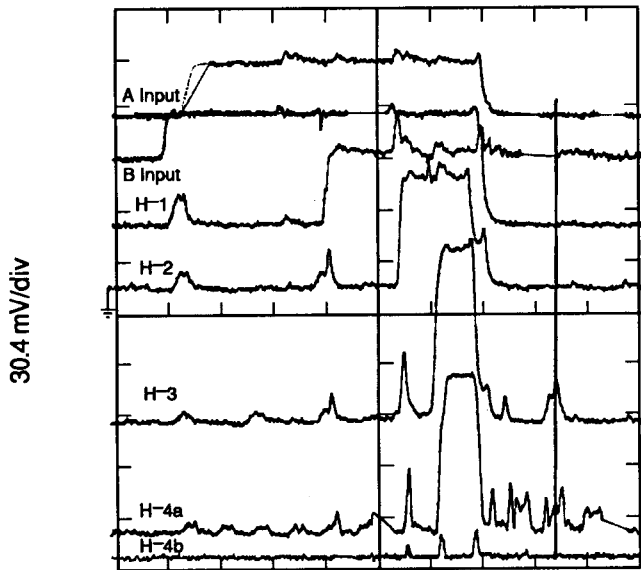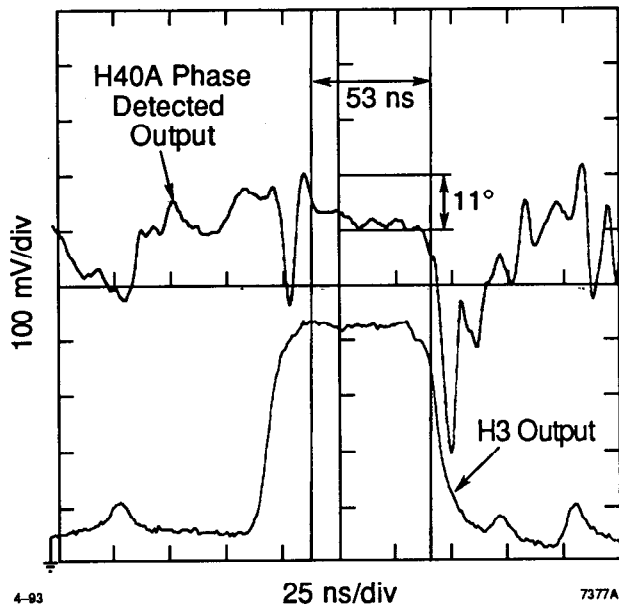
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Figure 6. 3-stage BPC outputs.

30.4 mV/div

100 ns/div

Figure 7. Amplitude and phase of the combiner output pulse.

100 mV/div

25 ns/div

H40A Phase Detected Output

53 ns

11°

H3 Output

The peak power of the 600 ns klystron output pulses was 34 MW for klystron B and 10 MW for klystron A. Thus the BPC plus combiner power gain was 175/44=4, rather than the ideal gain of 8. It is not difficult to account for the 3dB loss. The turn-around and phase-shifter loss is $0.4 \times 3 = 1.2$ dB, the hybrid loss is $0.3 \times 4 = 1.2$ dB, the total delay line loss including the loss of several WR90 stainless-steel flanges (the loss can be eliminated by copper plating them) is 0.6 dB.

TWO-STAGE MODULATION

The BPC network presents a match to the klystrons no matter what the setting of the phase shifters or the input modulation (see Fig. 1). The two-stage modulation is shown in Fig. 8. With two-stage modulation turned on,
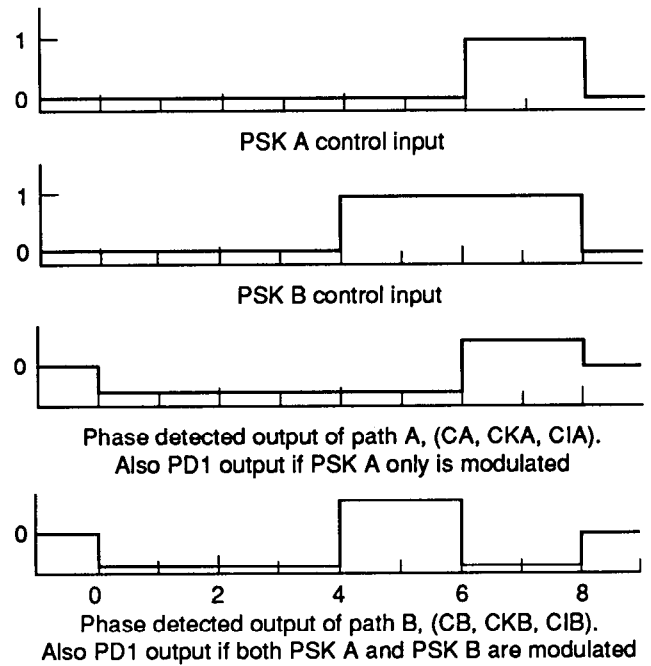

PSK A control input

PSK B control input

Phase detected output of path A, (CA, CKA, CIA).
Also PD1 output if PSK A only is modulated

Phase detected output of path B, (CB, CKB, CIB).
Also PD1 output if both PSK A and PSK B are modulated

Figure 8. Two-stage BPC modulation (horizontal unit = 70 ns).

adjust ϕ_1 to minimize H1OB during t=0 to t=4. Then adjust ϕ_2 to minimize H2OB during t=4 to t=6. During t=6 to t=8, both inputs to H3 are 4 units high and 2 units wide. Adjust ϕ_3 to combine the powers at H3OB. This output is 2 units (140 ns) wide and 8 units high pulse. Hybrid 4 divides the its input power at H4IB into two equal 4-unit high at H4OA and at H4OB. We still have a 2-stage BPC, each klystron output is quadrupled and its pulse width reduced by a factor of 4. But the combiner is neutralized by a divider. The experimentally obtained outputs are shown in Fig. 9. With some minor mecahnical modification we can send the combined 2-stage BPC outputs directly into the bunker to the accelerator section input, as indicated in Fig. 1.

POWERS FOR SLAC EXPERIMENTAL SECTIONS

Table 1 lists the requirements needed to attain accelerating gradients of $G_r = 100$ MV/m in the SLAC experimental accelerator sections. The third and fourth lines list the required pulse widths and peak powers into the SLAC experimental accelerator sections. The bottom line lists the power/klystron needed to achieve this. A 0.5 dB attenuation from Klystron output to BPC input was assumed. Assuming that our present klystrons can deliver a 34 MW- 600 ns pulses, a gradient of 100 MV/m in the 75 cm section is attainable. With the 3-stage BPC, 70 ns output pulse, the required power/klystron to attain 100 MV/m in the 180 cm section is 55 MW, but the section will be only half full. With 34 MW, and a 3-stage BPC the gradient attainable in the 180 cm section
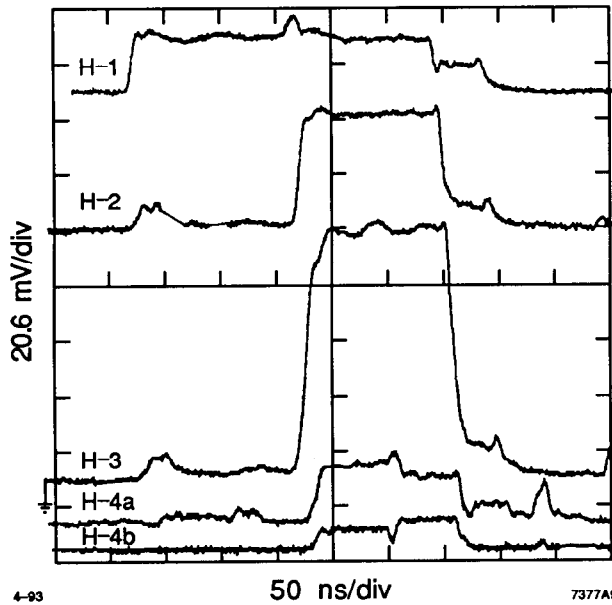
Figure 9. Two-stage BPC outputs.

Table I. Peak powers for 100 MV/m gradient in the SLAC experimental accelerator sections

Structure Length	30 cm	75 cm	180 cm	180 cm
Structure Fill Time	50 ns	50 ns	100	100 ns
Input Pulse Width	70 ns	70 ns	70 ns	140 ns
Structure Input Power	100 MW	220 MW	350 MW	350 MW
Atten. BPC Output to Struc. Input	1.76 dB	0.5 dB	0.5 dB	0.5 dB
Combiner Output	150 MW	224 MW	389 MW	389 MW
Power Gain	4	4	4	3 (2 stage)
Sum of BPC Input Powers	37.5 MW	61 MW	97.2	129 MW
Sum of Kly. Output Powers	42 MW	68 MW	109 MW	144 MW
Power/Klystron	21 MW	34 MW	55 MW	72 MW

$G_r = \sqrt{34/55} \times 100 = 79$ MV/m. With the 2-stage BPC, 140 ns pulse, $G_r = \sqrt{34/72} \times 100 = 69$ MV/m.

COMPARISON WITH SLED-II

The power gain P_g and compression efficiency η vs compression factor C_f are plotted in Figure 10 for SLED-II [2]. The coupling reflection was optimized at each C_f. Also plotted is the power gain an ideal BPC. For the SLAC
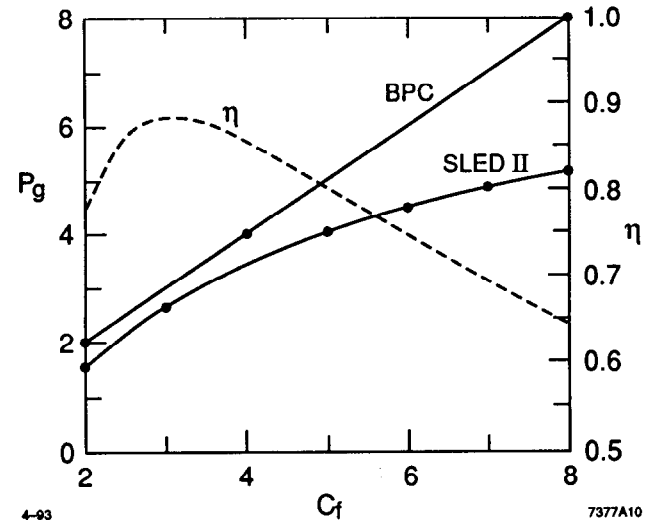

Figure 10. Power gain P_g and efficiency η vs. compression factor C_f.

3-stage BPC, the measured combined power divided by the power per klystron was 8. It probably can be increased to 10 with minor modifications. A klystron output pulse width of 600 ns means an 8:1 compression factor for a 70 ns structure input pulse, and 5:1 for a 140 ns structure input pulse. We see that the ideal SLED-II power gain is about half the actual BPC power gain. Hence, for the same klystron power and pulse width, the gradients attainable with SLED-II are about $1/\sqrt{2}$ that of the BPC. Of course, one can combine the outputs of two klystrons and reach the same gradient as with the BPC. But this would require the installation of another high power hybrid. With the BPC, the combiner is allready in place.

The delay line time delays are $T_d = (C_f + 1)T_p$ for the BPC and $T_d = T_p$ for SLED-II. For $C_f = 2$, the BPC requires half the SLED-II delay line length per klystron, and its efficiency is 100% rather than the 78% for SLED-II. The required line that transmits power to the second accelerator section can be made part of (incorporated into) the delay line. Practical efficiencies greater than 90% are achievable. The length of the delay line per klystron for a 2-stage BPC, is 1.5 times that of SLED-II.

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3. J. W. Wang, et. al. "High-Power Experiments in X-band Accelerator Stuctures" PAC93, May 1993.