

TWO NOVEL STRUCTURES FOR TUNABLE MEMS CAPACITOR WITH RF APPLICATIONS

E. Abbaspour-Sani, N. Nasirzadeh, and G. Dadashzadeh

Urmia University
Urmia, Iran

Abstract—Two novel structures for high- Q MEMS tunable capacitors are presented. The proposed designs include full plate as well as the comb structured capacitors. They can be fabricated employing surface micromachining technology which is CMOS-compatible. The structures do not require the cantilever beams which introduce considerable series resistance to the capacitor and decrease the quality factor. Therefore, our proposed structures achieve better Q in a smaller die area. The simulated results for 1 pF full plate capacitor shows a tuning range of 42% and a Q of 47 at 1 GHz. However, with the same initial capacitance, but the comb structure, the tuning range is increased to 43% but the Q is decreased to 45 at 1 GHz. The simulated Pull-in voltage with no residual stress is 3.5 V for both capacitors. The S_{11} responses are reported for a frequency range from 1 up to 4 GHz.

1. INTRODUCTION

Micromachining technology has been widely used for designing low cost and reliable structures such as sensors and actuators. In recent years, the CMOS compatible surface micromachining technology has been successfully used for RF applications. In design of devices like planar and non-planar antenna, filters, power dividers, switches and passive elements, MEMS technology is employed for its high quality factor, wide tuning range, low phase noise and small chip size. MEMS makes it possible to realize not only low insertion loss and bias power consumption but also single chip package which is impossible with standard semiconductor process [1–5].

The recent voltage tunable capacitors are using two methods, electrostatic and electro-thermal methods. The electrostatic method is derived from varying the distance between two parallel plates, with one movable and the other fixed plate. In this case, the theoretical

tuning range is limited by $C_{\max}/C_{\min} = 1.5/1$ [2, 3]. The electro-thermal method is derived from differential thermal expansions caused by differentiating the widths of the beams, which are supporting the movable plates. Compared with the electrostatic method, the electro-thermal method has wider tuning ranges, but it is slower and needs more die space [4, 5].

We have chosen parallel-plate gap tuning structure because of its small tuning voltage and low power consumption. Our modified plate structures, compared to the traditional MEMS capacitors, have not only reduced the tuning voltage but have gained other advantages.

2. PRINCIPLES OF OPERATION

Two new structures for MEMS varactors are presented. For both designs the basic concept of operation is the same. The main modification in our design is the freedom of movement for both upper and lower. The displaced sections are in the opposite sides of each other. When DC bias voltage is applied to the electrodes, both the upper and the lower plates are moved towards each other due to the electrostatic force. The maximum value of the capacitance variations is specified by the displacement of the plates just before the pull-in effect.

Figure 1 shows the cross sectional view of a general structure before and after application of a DC voltage. The main difference between two varactors is in their plate structure. For the first design a

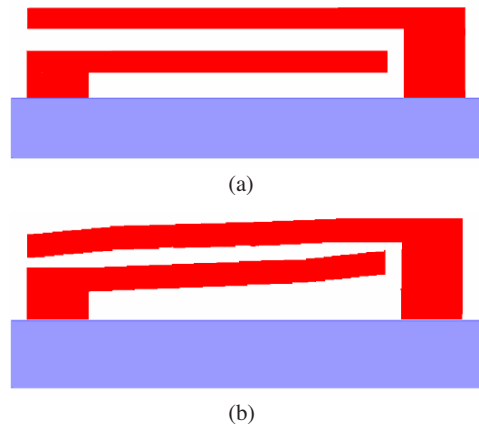


Figure 1. Cross sectional view of the proposed capacitor plates: (a) before and, (b) after, applying DC voltage.

full plate is used while the second varactor has a comb structure. Both capacitors are designed for initial theoretical capacitance of 0.6 pF with no applied DC voltage.

The Q of the conventional MEMS parallel plate capacitors to date is limited by losses arising from the finite resistivity of their suspension beams (cantilever beams) as illustrated in Fig. 2. These beams must be made long to attain stiffness values low enough to insure sufficiently low actuation voltages [2, 7]. Therefore, they introduce considerable series resistance to the structure and decrease the quality factor and also waste chip area. In effect, traditional micromechanical capacitor designs clearly exhibit a Q versus actuation voltage trade-off. This work breaks the above trade-off by eliminating the requirement for lengthy cantilever beams.

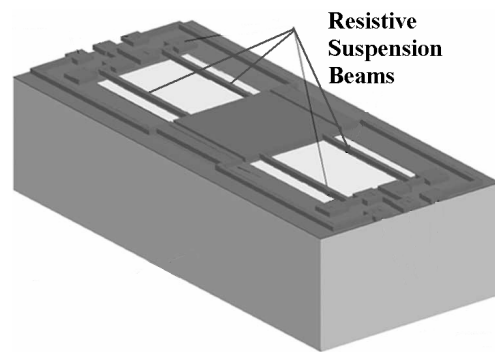


Figure 2. Traditional parallel-plate capacitor with lengthy suspension beams [6].

3. CAPACITORS STRUCTURES

The proposed structures, namely full plate and comb plate varactors are presented separately.

3.1. Full Plate Capacitor

The three dimensional view of the full plate structured varactor is shown in Fig. 3. The assumed dimensions for the capacitor plates are: $340\ \mu\text{m}$ length, $200\ \mu\text{m}$ width and $1.5\ \mu\text{m}$ thickness. Practically, we must provide etch holes on plates to insure a reliable etching of the sacrificial layers. This problem will be resolved when we introduce our comb structured varactor. However, for the simulation purpose we only consider the full plate structure. We assume a $1\ \mu\text{m}$ air gap

between two plates and $1.5\ \mu\text{m}$ air gap between the lower plate and the substrate. The substrate is considered as a silicon wafer of $400\ \mu\text{m}$ thickness. Polysilicon is chosen as the structural material of the plates because of its good mechanical properties.

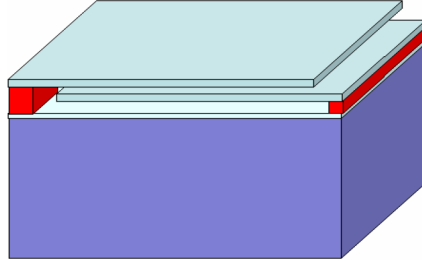


Figure 3. 3D view of the proposed full plate capacitor.

To consider the effect of metalized plates compared to poly plates only, two versions have been simulated. One, with plates of poly only and second, a double layer structure consisting of $1\ \mu\text{m}$ thick poly and $0.5\ \mu\text{m}$ gold on top of it. High frequency simulations are repeated for both versions.

3.2. Comb Structure

Figure 4 shows a conceptual 3D view of the comb structure capacitor. The assumed dimensions for each finger are: $9\ \mu\text{m}$ width, $200\ \mu\text{m}$ length and $1.5\ \mu\text{m}$ thickness. A $1\ \mu\text{m}$ separation between two successive fingers provides a reliable condition for etching the sacrificial layers. This resolves the sacrificial layers etch problem mentioned for the full plate structure. The number of fingers for each plate is considered to be 34.

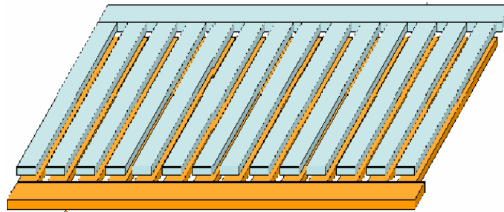


Figure 4. 3D view of the proposed comb structure.

As was the case for the full plate structure, both the double layer (poly/gold) fingers and the single layer (poly only) versions were simulated and the results are reported.

4. SIMULATION RESULTS

ANSYS software was used for Electrostatic and Ansoft HFSS for high frequency simulation of the capacitors.

The simulation results are presented for both full-plate and comb structure capacitors and are discussed separately.

4.1. Full Plate Structure

4.1.1. Electrostatic Simulations

At first, structures have been modeled using ANSYS environment then meshed. After the meshing process, DC voltage is applied between the plates. The plates displacement and therefore, capacitance have been extracted for several load steps. The capacitance variations versus the applied DC voltage is plotted and shown in Fig. 5. Pull-in effect occurs approximately at 3.6 V. This voltage is small enough for CMOS submicron technologies. The calculated tuning range using the C-V curve for both the single and double layer full plate varactor is 42%.

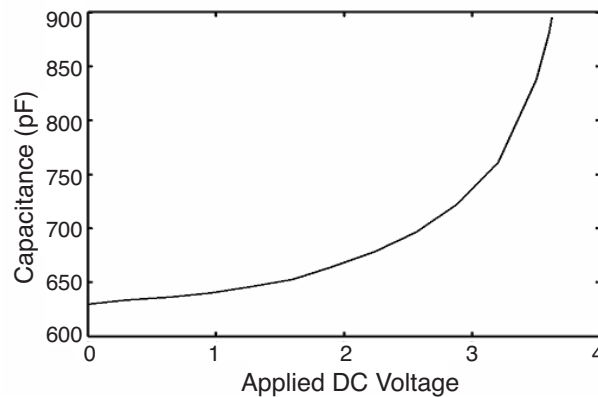


Figure 5. C-V curve for full plate structure.

4.1.2. High-frequency Simulations

We have applied the CPW (coplanar waveguide) which is composed of the ground-signal-ground (GSG) lines. This line is better than the microstrip line in that the ground line is placed under the signal line. It is very difficult to make the ground line contact the signal line through the silicon wafer. So, the CPW is frequently used for the RF signal line because the line is easy to make on the silicon wafer.

The variable capacitor is simulated as one-port network connected to a CPW of $50\ \Omega$. The structure has been simulated over a frequency range from 1 up to 4 GHz. The S_{11} responses are plotted on Smith chart for this range. Using simulation results the capacitance, equivalent series resistance, and the Q can be extracted from S_{11} . We have calculated these values at 1 GHz. The full plate varactor has a Q of 40 at 1 GHz which is equal to a $3.65\ \Omega$ series resistance and 1 pF capacitance.

Modified double layer (poly/Au) version shows a Q of 50 at 1 GHz. As mentioned before, the capacitors are designed for initial capacitance of 0.6 pF but, simulated results give a value of 1 pF for it. The difference between the calculated electrostatic value and the simulated results is due to the top plate to substrate coupling and fringing effects.

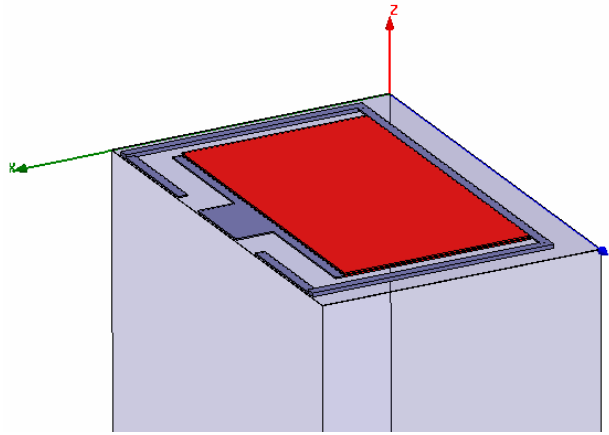


Figure 6. HFSS model of full plate varactor.

Figure 6 shows the HFSS model of the varactors. Also, S_{11} plots for single and double layers are reported in Fig. 7 and Fig. 8 respectively. Real and imaginary parts of Z , capacitance and the Q have been shown in Fig. 9 and Fig. 10 for single and double layers respectively.

4.2. Comb Structure

4.2.1. Electrostatic Simulations

Following the steps mentioned in Section 4.1, capacitance variations versus the applied DC voltage are extracted and plotted in Fig. 11. To plot C-V curve, we have done the simulation for only one finger and multiplied it by the number of the fingers which were 34. The

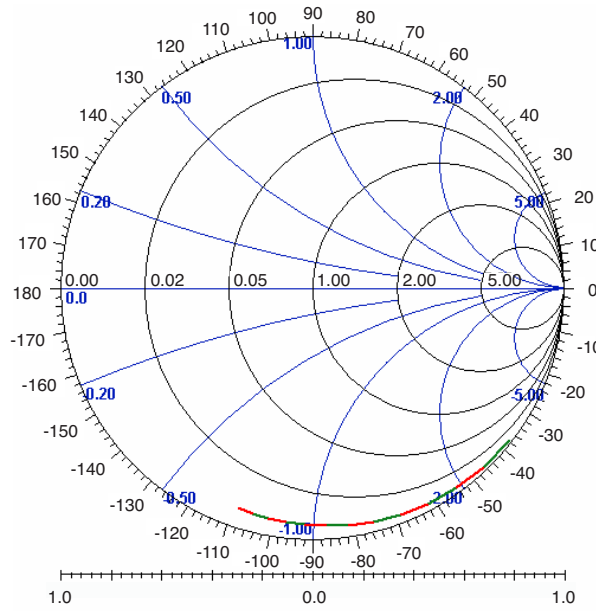


Figure 7. S_{11} response for full plate capacitor poly layer only.

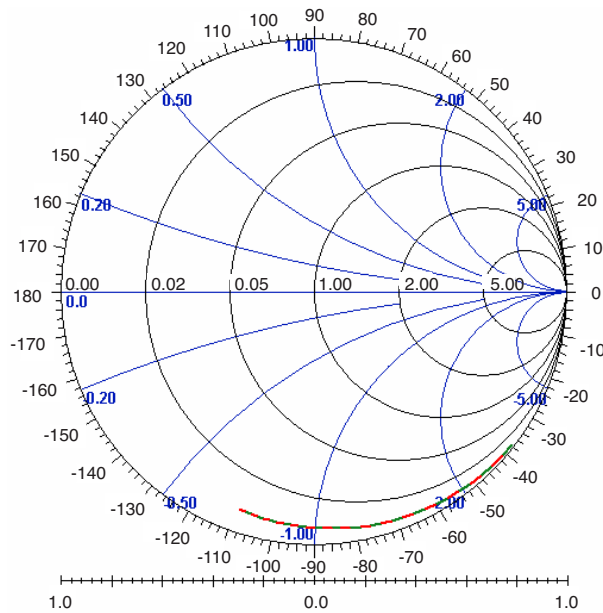


Figure 8. S_{11} response for double layer (poly/Au) comb structure.

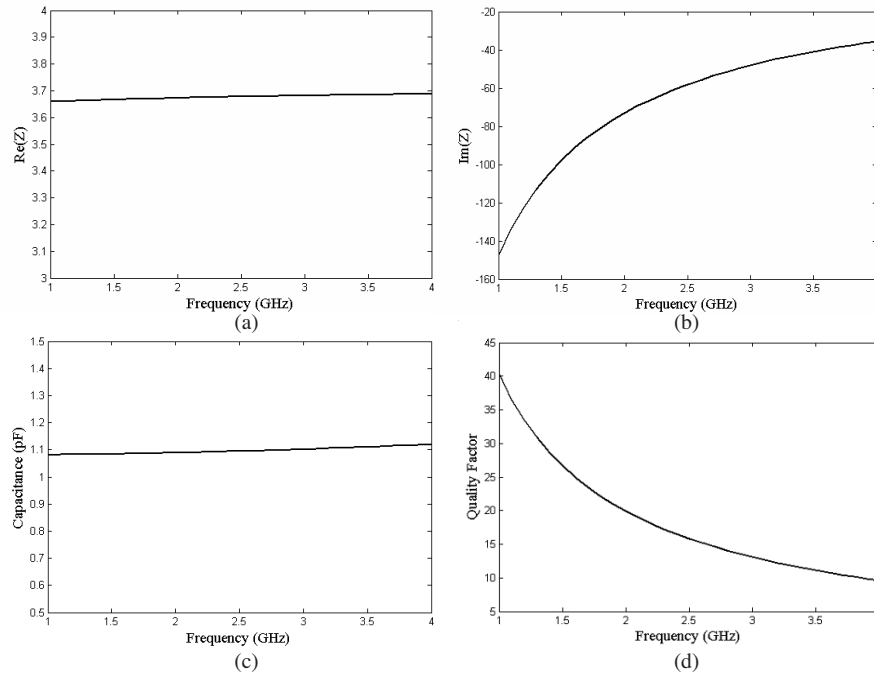


Figure 9. (a) real part and (b) imaginary part of Z , (c) capacitance and (d) the quality factor for single layer (poly only) full plate capacitor.

tuning range of comb structure is 43%. And the Pull-in voltage is approximately 3.6 V.

4.2.2. High-frequency Simulations

The structure has been simulated over a frequency range from 1 up to 4 GHz. The S_{11} responses are plotted on Smith chart for this range. We have calculated the capacitance, equivalent series resistance, and the Q at 1 GHz. The comb structure has a Q of 37 at 1 GHz which is equal to a 3.94Ω series resistance and 1 pF capacitance. Modified double layer (poly/Au) version shows a Q of 47 at 1 GHz.

Figure 12 shows the HFSS model of the varactor. The S_{11} plots for single and double layer structures are shown in Figs. 13 and 14 respectively. The real and imaginary parts of Z , capacitance and the Q are given in Fig. 15 and Fig. 16 for single and double layer capacitors respectively.

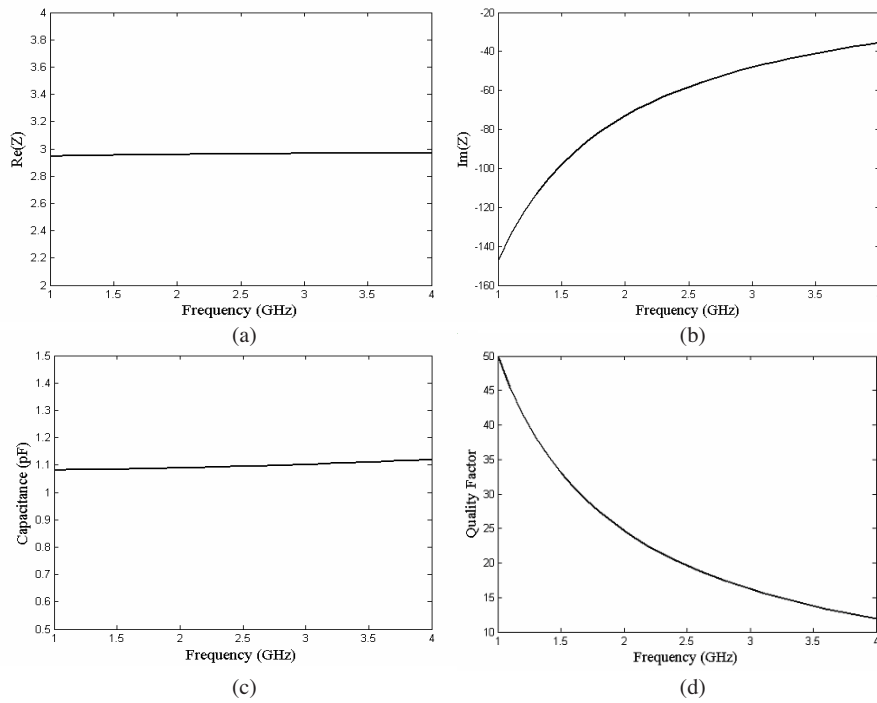


Figure 10. (a) real part and (b) imaginary part of Z , (c) capacitance and (d) the quality factor for double layer (poly/Au) full plate capacitor.

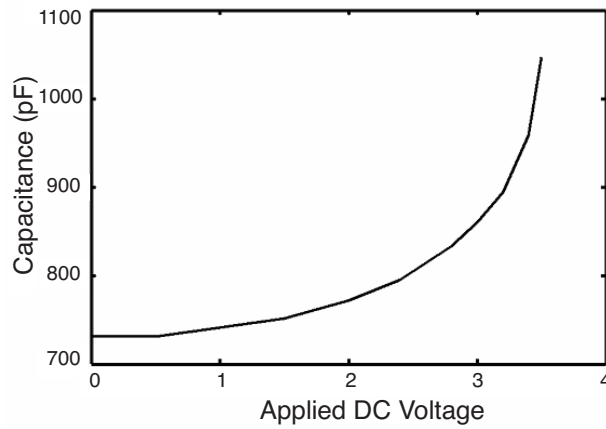


Figure 11. C-V curve of a finger under applied DC voltage.

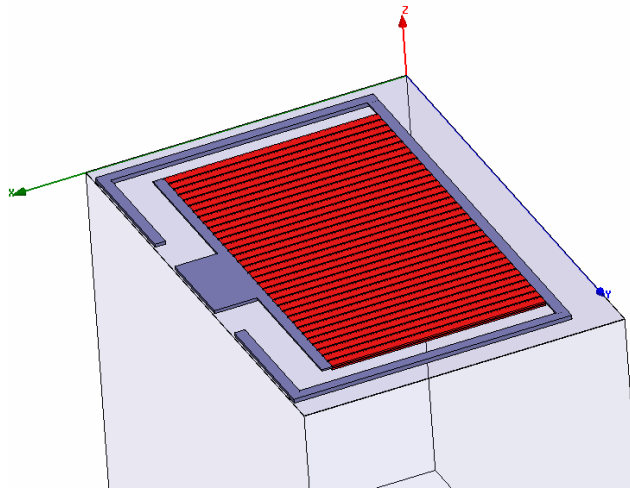


Figure 12. HFSS model of the comb structure.

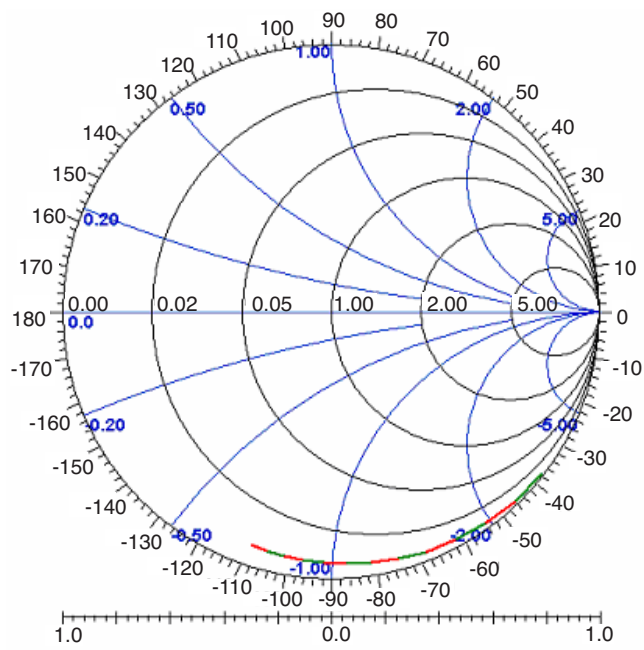


Figure 13. S_{11} response for single layer comb structure.

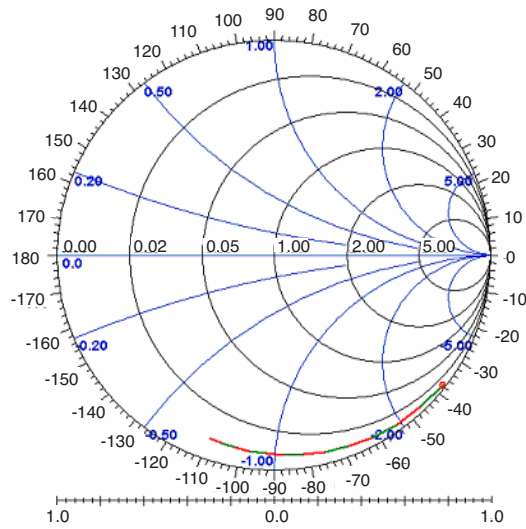


Figure 14. S_{11} response for double layer (poly/Au) comb structure.

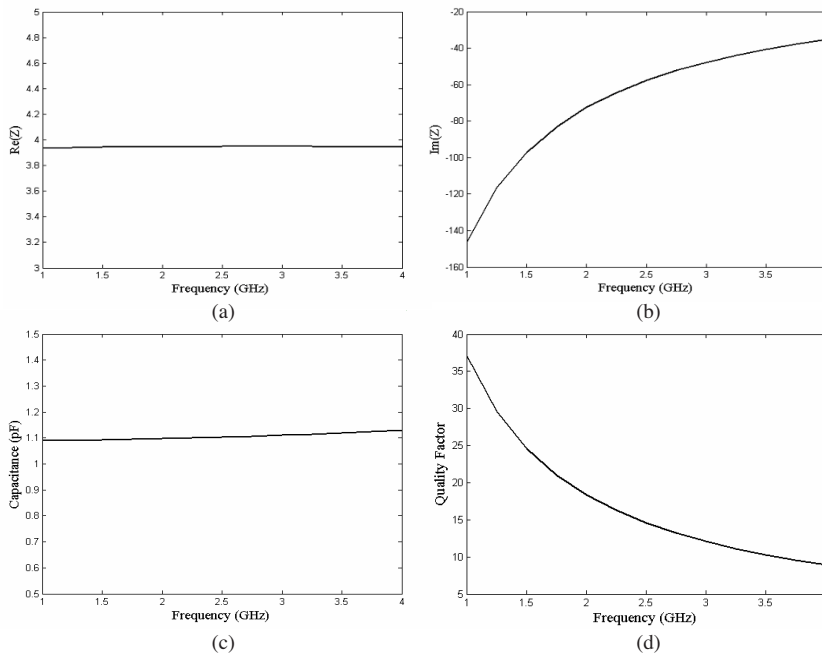


Figure 15. (a) real part and (b) imaginary part of Z , (c) capacitance and (d) the quality factor for single layer comb structure.

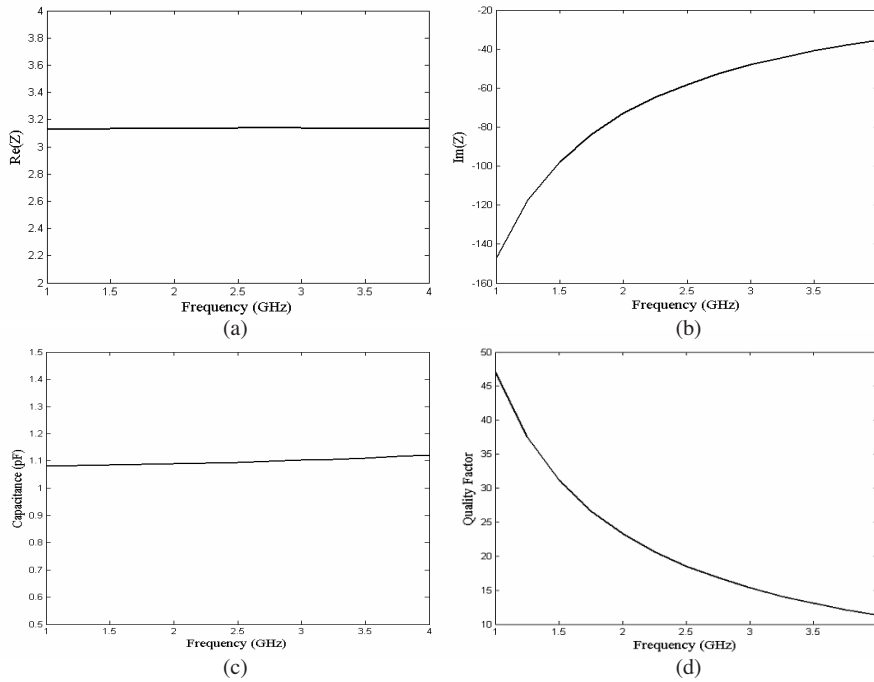


Figure 16. (a) real part and (b) imaginary part of Z , (c) capacitance and (d) the quality factor for double layer (poly/Au) comb structure.

5. CONCLUSION

Two High- Q micromachined electro-mechanically tuneable capacitors for RF applications are presented. In these new structures there is no need for cantilever beams which introduce considerable series resistance to the structure and decrease the quality factor.

Coupled-field analysis capability of ANSYS software has been used to obtain the capacitance variations versus the applied DC voltage. Also Ansoft HFSS software is employed for high frequency modeling of structure to extract capacitance values and the quality factor.

The electrostatic simulated results show Pull-in voltage of approximately 3.6 V for both designs.

High frequency simulations are repeated for single layer and double layer versions of the both full and comb plate structures.

Full plate varactor shows a Q of 40 at 1 GHz and a tuning range of 42%. Added gold layer increases the Q to about 50 at 1 GHz. Comb structure has a Q of 37 at 1 GHz and a tuning range of 43%.

Table 1 summarizes the results for the proposed varactors. Due to the high Q obtained by these structures they can be a good competitor for the conventional parallel-plate MEMS varactors.

Table 1. Summary of the simulation results.

Structure	Tuning range	Q	Z at 1 GHz
Full plate single layer	42%	40	3.65-j147
Full Plate double layer (poly/Au)	42%	50	2.94-j147
Comb structure single layer plate	43%	37	3.94-j146.1
Comb structure double layer plate (poly/Au)	43%	47	2.13-j147.2

Table 2 is a comparison between the proposed varactors and some of the reported MEMS varactors. The reason for higher Q of the case [9] is that it uses only gold as the structural material but nowadays polysilicon is preferred because of its good mechanical properties.

Table 2. Comparison between our structures and previous works.

Varactor	Tuning Range	Q at 1 GHz	Tuning Voltage	Area
[9]	16%	62	0–5.5 V	1
[10]	230%	13	0–7 V	≈ 1
[11]	25%	9.6	0–3 V	1
[12]	50%	20	0–4 V	1
This work: Full plate	42%	40–50	0–3.6 V	$\approx 1/3$
This work: Comb structure	43%	37–47	0–3.6 V	$\approx 1/3$

Although it dose not seem to be fare to compare our simulated results with the measured values of the others, at least we are satisfied that the base of our assumptions and the result of our simulation are correct.

ACKNOWLEDGMENT

This work is supported by ITRC (Iran Telecom Research Center). The authors would like to thank Mr. Fallahi and Mr. Pirhadi for their help with HFSS simulations. Also the authors would like to express their sincere thanks to Dr. M. Bakri-Kassem from the University of Waterloo for his valuable comments.

REFERENCES

1. Clark, T., C. Nguyen, L. P. B. Katehi, and G. M. Rebeiz, "Micromachined devices for wireless communications," *Proceedings of the IEEE*, Vol. 86, No. 8, 1756–1767, 1998.
2. Alexander, D. and K. Suyama, "Miromachined capacitors and their application to RF IC's," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 12, 2587–2596, 1998.
3. Alexander, D. and K. Suyama, "2.4 GHz CMOS LC VCO using micromachined variable capacitors for frequency tuning," *Microwave Symposium Digest, 1999 IEEE MTT-S International*, Vol. 1, 79–82, 1999.
4. Feng, Z., W. Zhang, B. Su, Gupta, Bright, and Lee, "Design and modeling of RF MEMS tunable capacitors using electro-thermal actuators," *Microwave Symposium Digest, 1999 IEEE MTT-S International*, Vol. 4, 1507–1510, 1999.
5. Harsh, K., F. Zhang, Bright, and Lee, "Flip-chip assembly for Si-based RF MEMS," *MEMS'99 Twelfth IEEE International Conference on Micro Electro Mechanical Systems*, 273–278, 1999.
6. Bakri-Kassem, M. and R. R. Mansour, "Two movable-plate nitride-loaded MEMS variable capacitor," *IEEE Transactions on Microwave Theory and Applications*, Vol. 52, No. 3, March 2004.
7. Moaveni, S., *Finite Element Analysis Theory and Applications with ANSYS*, Prentice Hall, 1999.
8. Edwards, T. C. and M. B. Steer, *Foundations of Interconnect and Microstrip Design*, 3rd edition, Chapter 6, John Wiley & Sons Ltd., 2000.
9. Young, D. J. and B. E. Boser, "A micromachined variable capacitor for monolithic low-noise VCOs," *Solid-state Sensor and Actuator Workshop*, 86–89, Hilton Head, SC, June 1996.
10. Kassem, M. B. and R. R. Mansour, "Two movable-plate nitride-loaded MEMS variable capacitor," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 52, No. 3, March 2004.

11. Dec, A. and K. Suyama, "Micromachined varactor with wide tuning range," *Electronics Letters*, Vol. 33, 922–924, May 1997.
12. Dec, A. and K. Suyama, "Miromachined capacitors and their application to RF IC's," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 12, 2587–2596, 1998.