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Two novel ultra high speed carbon nanotube Full-Adder cells

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Abstract: In this paper two ultra high speed carbon nanotube Full-Adder cells are presented. First design uses two transistors, two resistors and seven capacitors and the second one uses four transistors and seven capacitors. The first design is faster and the second one consumes less power. Simulation results illustrate significant improvement in terms of speed and Power-Delay Product (PDP).

Keywords: Full-Adder, nanotechnology, CNFET, CMOS

Classification: Integrated circuits

References

[1] S. Timarchi and K. Navi, "Arithmetic Circuits of Redundant SUT-RNS," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 9, pp. 2959–2968, Sept. 2009, DOI: 10.1109/TIM.2009.2016793.

[2] A. S. Mollahosseini, K. Navi, C. Dadkhah, O. Kavehei, and S. Timarchi, "Efficient Reverse Converter Design for new CRTs," *IEEE Trans. Circuit Syst. I.*

[3] A. Raychowdhury and K. Roy, "Carbon-Nanotube-Based Voltage-Mode Multiple-Valued Logic Design," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 168–179, March 2005.

[4] A. Raychowdhury and K. Roy, "Carbon Nanotube Electronics: Design of High-Performance and Low-Power Digital Circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 11, pp. 2391–2401, Nov. 2007.

[5] K. Navi, M. Moayeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two New Low-Power Full-Adders Based on Majority-Not Gates," *Microelectronics Journal*, vol. 40, no. 1, pp. 126–130, Jan. 2009.

[6] K. Navi, M. Maeen, and O. Hashemipour, "An Energy Efficient Full-Adder Cell for Low Voltages," *IEICE Electron. Express*, vol. 6, no. 9, pp. 553–559, 2009.

[7] C.-H. Chang, J. Gu, and M. Zhang, "A Review of 0.18-μm Full-Adder Performances for Tree Structured Arithmetic Circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, June 2005.

[8] C.-H. Chang, M. Zhang, and J. Gu, "A Novel Low Power Low Voltage Full Addes Cell," *3rd International Symposium on Image and Signal Processing and Analysis (ISPA)*, vol. 1, pp. 454–458, Sept. 2003.

[9] J. Deng and H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Bench-

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marking," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.

1 Introduction

Digital circuit designers have always been encountered in a tradeoff between speed and power consumption to improve their design's performance [1, 2]. One of the solutions proposed to circumvent this tradeoff is to decrease the circuit's size. However scaling of conventional CMOS has many limitations and becomes increasingly harder. Hence carbon nanotube-based transistors (CNFETs) are currently considered as a replacement of silicon transistors (MOSFETs) [3, 4]. CNFETs are transistors which are composed of sheets of graphite rolled into tubes, called carbon nanotubes (CNTs), as their gates. These nano scale transistors have attracted the circuit designers' heed because they consume low power nevertheless their performance are extremely high.

Recently, some circuit applications are presented based on CNFETs, such as ring oscillators, galois fields, invertors, and logic gates. However arithmetic operations are extensively used in many VLSI applications such as signal processing, and digital communication [5, 6]. Therefore the utilization of CNFETs in the design of Full-Adders which are the fundamental core of the arithmetic operations may result in high performance and low power arithmetic circuits.

In this paper we present two new ultra high speed CNFET-based Full-Adders. These Full-Adders are designed based on majority function. Section 2 presents a review of different types of CNFETs. For comparison of the simulation results of these new Full-Adders with previous ones, four Full-Adders are explored in section 3. Two proposed Full-Adders are analyzed in section 4. Section 5 compares the proposed Full-Adders with the others which is illustrated in section 3. And finally, section 5 concludes the paper.

2 CNTFEs

Carbon nanotubes (CNTs) are nano scale tubes which are created by rolled sheets of graphite. Since the discovery of CNT in 1991 by S. Iijima, numerous applications of it have been demonstrated in different fields because of its specific characteristics. It can either be the best metal or semiconductor known relying on rolling direction of the graphite sheets [4]. Another applicable property of CNT is ballistic convey of electrons along the tube, therefore it can be used as the channel of the field effect transistors called CNFETs.

CNFETs operate like traditional silicon transistors. Different types of CNFETs have been presented. One of them is Schottky Barrier CNTEF (SB-CNFET). These transistors use direct contact of the metal with the nanotube in their fabrication process; hence they have Schottky Barrier at the metal nanotube junction. In this type of CNFETs the majority carri-

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ers tunneling through the Schottky Barrier at the end contacts control the conductivity. Due to showing ambipolar transport behavior, SB-CNFETs are suitable for using in CMOS logic families. Another type of CNFETs is MOSFET-like CNFET (MOS-CNFET) which exhibit unipolar behavior unlike SB-CNFET. The conductivity of MOS-CNFETs is modulated by the gate-source bias. Both SB-CNFETs and MOS-CNFETs are used for high speed design because of their high ON current, however the other type of CNFET, band-to-band tunneling CNFET (T-CNFET) is utilized for ultra-low-power design on account of its low ON current and supper cutoff attributes [4]. One of the most useful properties of CNFETs is that the threshold voltage is proportional to the inverse of the diameter of the nanotube as:

$$V_{th} = \frac{0.42}{d(nm)}eV \tag{1}$$

This feature of CNFETs indicates that by changing the CNFETs diameters one can easily acquire different transistors with different turn on voltages. It will ease circuit designing and increase circuit's performance on the other hand [3].

3 Previous works

Various high performance Full-Adders have been implemented in different technologies and logic styles. Most of them use different kinds of CMOS technology. Some Full-Adder designs are shown in fig. 1. These circuits utilize CMOS technology.

The complementary CMOS Full-Adder (fig. 1 (a)) which is called C-CMOS [7], is composed of 28 transistors in two separate networks, PMOS transistors as pull-up network and NMOS transistors as pull-down network. The profit of this design is its strength against transistor sizing and voltage scaling which enables us to provide high performance circuit and credible operation at low voltages and low transistor sizes.

The 26 T Full-Adder (fig. 1 (b)) [8] is constructed by two stages. First stage is composed of six transistors to produce the balanced XOR and XNOR functions and four more transistors to overcome the slow response problem of XOR and XNOR outputs. Second stage is made up of ten transistors to create *Cout* and six transistors to make *sum* function.

The Complementary Pass-Transistor Logic Full-Adder (fig. 1 (c)) [7] is composed of two separate circuits for implementing carry and *sum*. Each circuit has two NMOS logic networks, two pull up PMOS transistors and two inverters. Totally it uses 32 transistors and produces 4 output signals for *sum*, $\overline{sum}$, *Cout* and $\overline{Cout}$. Because of using pass-transistor logic in its structure it has threshold voltage drop problem, thus output inverters are used to guarantee the drivability.

The Transmission Gate Full-Adder (fig. 1 (d)) [7] is based on transmission gates and consists of 20 transistors. A transmission gate is composed of an NMOS transistor and a PMOS transistor that are connected in a parallel manner. These transistors are turned on or off simultaneously and both of

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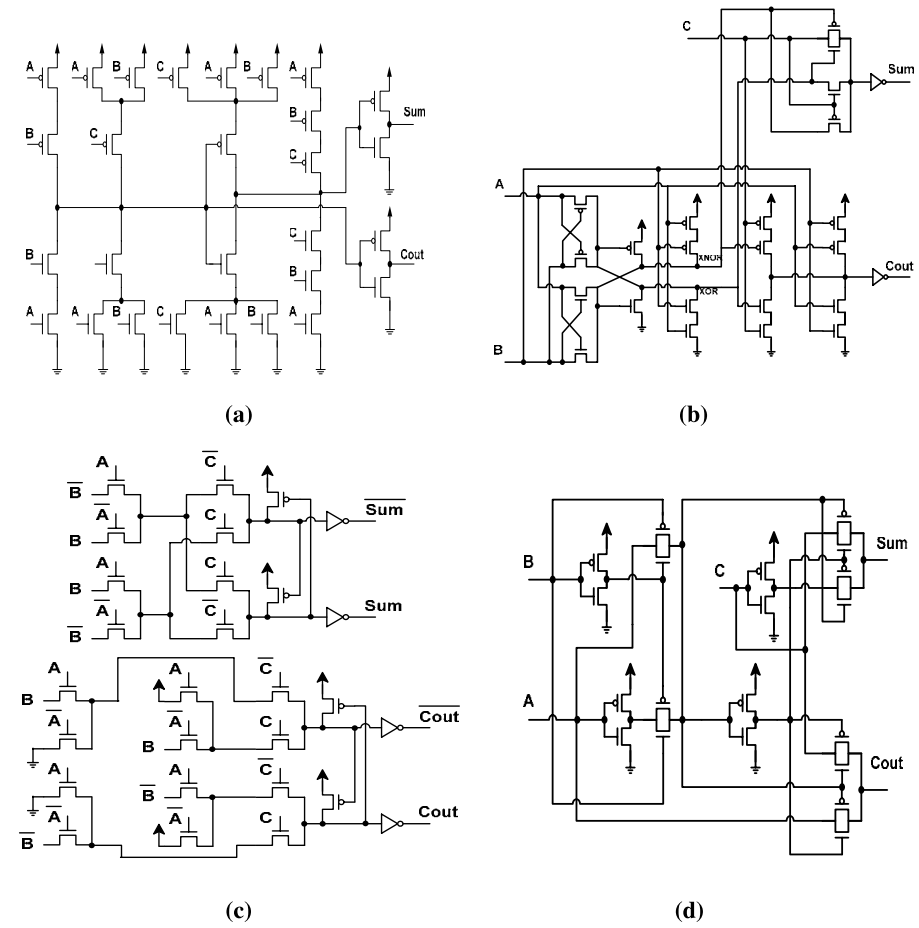

Fig. 1. Full-Adder cells (a) C-CMOS. (b) 26 T. (c) CPL. (d) TGA

them provide the path to the input separately, therefore there is no voltage drop problem in it. However to design the similar function, double number of transistors are needed.

4 Proposed designs

The two proposed Full-Adder designs are implemented by means of majority function, based on carbon nanotube technology. The majority function is discussed in [5] in detail. Looking at the truth table of *Cout* and three-input majority function, it will be considered that *Cout* can easily be implemented with a three-input majority function as shown in equation (2).

$$Cout = AB + AC + BC = Majority(A, B, C) \tag{2}$$

For implementing *sum*, we take advantage of another majority function. The following equations exhibit this idea.

$$\begin{aligned} SUM &= Majority(A, B, C, \overline{Cout}, \overline{Cout}) \\ &= ABC + \overline{Cout}(AB + AC + BC) + \overline{Cout}(A + B + C) \\ &= ABC + \overline{Cout}.Cout + \overline{Cout}(A + B + C) \\ &= ABC + (\overline{AB}.\overline{AC}.\overline{BC}).(A + B + C) \\ &= ABC + \overline{A}.\overline{B}.C + \overline{A}.B.\overline{C} + A.\overline{B}.\overline{C} \end{aligned} \tag{3}$$

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Hence if we exert a majority function on five inputs which two of them are $\overline{Cout}$ and the others are A, B and C, we will have *sum* on the output.

These two equations are foundation of the two novel Full-Adder designs. Since there are no differences between producing *sum* and *Cout* and the invert of them ($\overline{sum}$ and $\overline{Cout}$), we use two majority not function and produce $\overline{sum}$ and $\overline{Cout}$ instead of *sum* and *Cout* to ease the implementation and increase its performance.

4.1 Design 1

The first design is constructed in two stages. The first stage implements $\overline{Cout}$ by means of a majority not function. For this reason it uses three input capacitors to prepare an input voltage for driving the n-CNFET. Through superposition of input capacitors, we have scaled addition of input voltages at point x. for instance in the case of '000' for the inputs, the voltage of point x is 0 V, in the state of '010' we have $\frac{Vdd}{3}$ for this point's voltage, the state of '011' causes to have $\frac{2Vdd}{3}$ and finally in the '111' state the voltage of point x equals to *Vdd*. As mentioned before the threshold voltage of CNFETs can easily be controlled by changing the diameter of nanotubes. The n-CNFET threshold voltage is regulated so that it will be on if more than one of inputs are high and it will be off otherwise. Therefore this stage of the design operates like a majority not function and calculates $\overline{Cout}$. The second stage utilizes a five-input majority not function to implement $\overline{sum}$. Three of its inputs (A, B and C) are similar to the previous stage. Other two inputs are created by using the previous stage output ($\overline{Cout}$). If more than two inputs are high the n-CNFET will be on and the output will reduce to '0'. Otherwise the n-CNFET will be off and the output will increase to *Vdd* through the resistor. Fig. 2 (a) shows the first proposed design.

4.2 Design 2

Even though the first design's speed is extremely high in comparison with other mentioned Full-Adders, it has two disadvantages. Because of using the resistors in its pull up network, it consumes static power when the CNFETs are on. On the other hand when the CNFETs are on, the output should be '0' but it will be more than '0' because of the resistor, so it is not a full swing design.

The second proposed design shown in fig. 2 (b) tries to overcome these problems by substituting the pull up resistors with p-CNFETs. However this design is slower than the previous one because of using p-CNFETs in its pull up network, it consumes less power and its PDP is much better than the first design.

5 Simulation results

The HSPICE circuit simulator has been used for both CMOS and CNFET based circuits of fig. 1 and two proposed Full-Adders. The four circuits C-CMOS, 26 T, CPL and TGA of fig. 1 are simulated using a 0.18 um tech-

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nology. A compact model of CNFETs presented in [9] has been used for CNFET based circuits' simulation. In this model a MOS-CNFET device is implemented in three levels. In first level (CNFET_L1) the intrinsic behavior of MOS-CNFET has been modeled. In level 2 (CNFET_L2) the device non-idealities have been included and in the top level of this hierarchical modeling (CNFET_L3), multiple CNTs for each MOS_CNFET device are allowable. In this paper CNFET_L3 is used for simulating the CNFET based circuits. The supply voltage is 0.9 V for all of the circuits and they are simulated at room temperature. The comparison of DELAY, POWER and POWER-DELAY PRODUCT (PDP) of Full-Adders is discussed below.

Table I shows the value of delay, power and PDP of C-CMOS, 26 T, CPL, TGA and two novel CNFET based Full-Adders. The time from fifty percent of the input voltage swing to fifty percent of the output voltage swing is measured as delay. As is shown in this table the smallest delay belongs to the first proposed design. It is 15.3 times faster than 26 T which has the best delay among CMOS Full-Adders. It is 18.9, 15.7 and 19.4 times faster than C-CMOS, CPL and TGA also. Although the first proposed design has the best speed, its average power dissipation is more than all of the designs and it is because of the using of the resistors in pull up network and therefore static power consumption. To solve this problem second design is proposed. It consumes 46% less power than the first design and is just 0.04% slower than it. As it considered from the table I the second design has the best PDP in comparison with the other Full-Adders. Its improvement is 84.5% in comparison with C-CMOS.

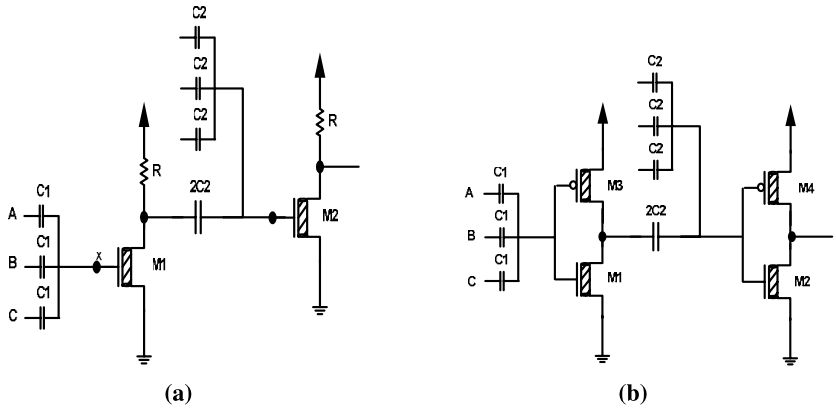

Fig. 2. Full-Adders. (a) Design 1, (b) Design 2

Table I. Simulation results for the Full-Adders in 0.9 V supply voltage

	Delay(*e-12)	Power(*e-6)	PDP(*e-16)
C-CMOS	230.63	1.1643	2.6853
26T	186.435	1.9882	3.7067
CPL	192.38	1.8862	3.6286
TGA	237.231	1.4204	3.3696
Design 1	12.184	6.2357	0.7598
Design 2	12.188	3.4108	0.4157

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6 Conclusion

In this paper, two novel high speed CNFET based Full-Adders has been proposed. These proposed circuits use Majority Not Functions. To evaluate their performance, four CMOS based Full-Adders have been simulated on HSPICE by using a 0.18 μm technology. A CNFET compact model for CNFET based circuits have been used. Simulation results show that the pesented Full-Adders have better speed and PDP in comparision with the CMOS based ones.

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