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Two Optimization Ways of DDR3 Transmission Line Equal-Length Wiring Based on Signal Integrity

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***Abstract*—As we enter the 5G (5th-Generation) era, the amount of information and data has become increasingly tremendous. Therefore, electronic circuits need to have higher chip density, faster operating speed and better signal quality of transmission. As the carrier of electronic components, the design difficulty of high-speed PCB (Printed Circuit Board) is also increasing. Equal-length wiring is an essential part of PCB design. But now, it can no longer meet the needs of designers. Accordingly, in view of the shortcomings of the traditional equal-length wiring, this article proposes two optimization ways: the "spiral wiring" way and the "double spiral wiring" way. Based on the theoretical analysis of the transmission lines, the two optimization ways take the three aspects of optimizing the layout and wiring space, suppressing crosstalk and reducing reflection as the main points to optimize the design. Eventually, this article performs simulation and verification of schematic diagram and PCB of the optimal design by using HyperLynx simulation software. The simulation results show that these two ways not only improve the flexibility of the transmission line layout, but also improve the signal integrity of the transmission lines. Of course, this also proves the feasibility and reliability of the two optimized designs.**

***Keywords*—high-speed PCB, signal integrity, equal-length wiring, HyperLynx**

I. Introduction

With the commercial application of 5G communication technology in 2019, the electronic information industry is showing an upward trend. At the same time, the printed circuit industry is also growing, especially the high-end printed circuit board. The continuous emergence of new PCB markets has promoted continuous innovation in PCB technology [1] [2]. With the advent of the 5G era, the requirements for electronic devices are becoming more compact and thinner. HDI (High Density Interconnection) PCB has become a new topic of current PCB technology development. In particular, the miniaturized drive PCB is more complex and compact, and it is more challenging to assume more functions in a small space. Therefore, SI (Signal Integrity) has become one of the key points of this type of PCB design. The use of SLP (Substrate-Like PCB) in mobile phones is a perfect example of PCB technology innovation and development.

In order to adapt to the new situation in the 5G communication era, literature [3] takes the design and manufacturing of high-speed PCB as an example. It uses analysis methods of signal integrity to combine the design of ground copper bridges, differential transmission lines and vias with the characteristics of high-speed circuits and the actual manufacturing process. Creatively transfer the outer differential microstrip through the blind vias (microporous) to the inner Stripline. This method effectively solves the signal distortion problem of high-speed PCB. To a certain extent, the design of high-speed circuits is optimized and the product development cycle is shortened. Literature [4] solved the measurement requirements of large-scale sensor arrays. It designs a multi-channel high-speed synchronous data acquisition system through signal integrity simulation analysis. The system is based on a daisy chain structure and has a data cache function. Literature [5] solved the SI design problem of digital circuit reflection and crosstalk caused by the increasing wiring density of PCB. It has been designed and verified in the Altium Designer environment and found that it can effectively solve the reflection problem in the signal after ensuring the rationality of the termination. Literature [6] solved the problem of high-speed parallel bus interface signal. It first proposed high-speed parallel bus interconnection design and related concepts of signal integrity. On this basis, it also proposes optimization strategies that cause incomplete signal emission, crosstalk, synchronous switching noise, and inter-symbol interference. In summary, the PCB optimization ways in these documents are designed to solve the following two problems:

- Circuit layout problem of high-density interconnect PCB,
- SI problem of high-density interconnect PCB.

PCB design is highly efficient and fast. PCB layout and signal integrity directly affect the performance of the circuit. In line with the concept of "design is correct", the circuit layout with good signal integrity can not only shorten the development cycle, but also reduce the development cost [7].

This article analyzes and studies the equal-length wiring ways of PCB. The main content can be divided into three parts. Section 2 briefly introduces the traditional equal-length wiring way. Then, in view of its shortcomings, two new equal-length wiring ways are proposed:

- The "spiral wiring" way is used to optimize the line layout of single-ended transmission line,
- The "double spiral wiring" way is used to optimize the line layout of differential transmission lines.

Section 3 and section 4 respectively analyze the optimal design of "spiral wiring" and "double spiral wiring" ways in detail. Then, the two ways were simulated and verified. Based on the transmission line theory, the optimization design of

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the two ways mainly includes three aspects: optimizing layout space, suppressing crosstalk, and reducing reflection.

In addition, this article uses HyperLynx software to conduct schematic diagram simulation and PCB simulation on the optimized design and its signal integrity. The simulation results show that the two ways not only improve the flexibility of the transmission line layout, but also improve the signal integrity of the transmission line.

II. The traditional ways of equal-length wiring

Before the design of the schematic and PCB, the size of the circuit board and the position of some chips have been set by the customer. For example, the size of the ultra-high-speed sampling board and the location of some specific electronic chips. Therefore, how to route among the components on the PCB is a problem that the PCB designer must consider. In the wiring between PCB components, equal-length wiring is an indispensable link, especially some buses with timing requirements, such as DDR. At present, in PCB layout and wiring, equal-length wiring has only two ways, the ”snake-shaped wiring” way and ”zig-shaped wiring” way [8], as shown in Figure 1. But in fact, designers often only use the ”snake-shaped wiring” way.

However, with the increasing demand for informationization and broadbandization in society and the continuous development of semiconductor technology and integrated circuits, the volume of electronic systems has become smaller and chip distribution has become more dense [9]. It is very difficult for designers to layout and wiring between components on a small, compact PCB. At this time, traditional equal-length wiring ways such as ”snake-shaped wiring” way can no longer meet the changes of PCB and the design requirements of designers. First, the traditional equal-length wiring ways is limited to single-layer wiring and lacks flexibility. Second, with the miniaturization of PCB, the traditional equal-length wiring ways not only consumes wiring space, but also easily causes signal integrity problems. In this case, how to ensure good signal quality during transmission and optimize the interconnection layout between components in the PCB is worthy of our in-depth study. Therefore, in view of the shortcomings of the traditional equal-length wiring of PCB, this article proposes two optimization ways: the ”spiral wiring” way and the ”double spiral wiring” way.

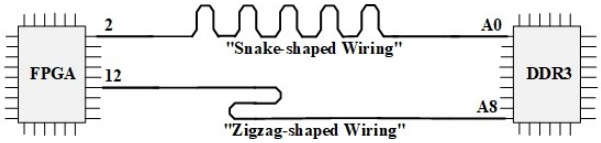

Fig. 1. Two traditional ways of equal-length wiring

III. The”spiral wiring” way and its simulation

”Spiral wiring” way in Figure 2 is an optimization of the traditional equal-length wiring of single-ended transmission line. This section will conduct qualitative analysis and simulation verification from the three aspects of layout space, crosstalk and reflection. But before that, we need to briefly introduce the transmission line theory and its signal integrity. Mainly to facilitate the analysis of the signal integrity of the transmission line.

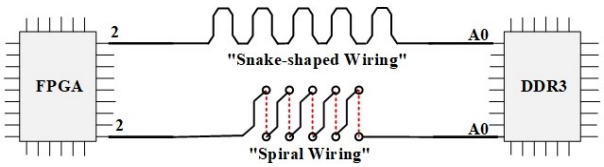

Fig. 2. The ”spiral wiring” way

A. Transmission line theory

In high-speed circuits, when the clock frequency exceeds 100 MHz and the signal rise time is less than 1 ns, interconnect lines longer than 1 inch begin to show transmission line and antenna effects. When the charge flow of the high-speed signal interacts with the transmission line, the characteristic parameters of the transmission line will affect the quality of the transmission signal. Signal integrity refers to the quality of the signal in the circuit transmission. For example, in a DDR (Double Data Rate) memory circuit, when the bus signal can be transmitted to the receiving end with the correct timing, retention time and voltage strength, the circuit system has good signal integrity. Otherwise, the system will have signal integrity problems [10].

1) Transmission line model: There are two common types of transmission line: microstrip and stripline [11]. When the signal is high frequency and the edge rate of signal (rising edge time and falling edge time) is small relative to the signal transmission time, the transmission line effect will have a significant impact on the signal. Figure 3 shows a description of the work of the transmission line.

In the signal transmission process, the two main problems that affect signal quality are signal reflection on the transmission line and crosstalk between lines. Use the RLCG unit (as shown in Figure 4) to build an equivalent circuit model of the transmission line. This is to facilitate the analysis of the influence of characteristic impedance, crosstalk and reflection on the signal integrity of the transmission line. The transmission line is lossy. When constructing the RLCG transmission model with inductance L and capacitance C, the circuit needs to add a series resistance and a parallel resistance. In the figure, the series resistance Rdz indicates that the transmission line is not a pure conductor but lossy; the parallel resistance Gdz indicates that the insulator between the transmission line and the ground is finite; the resistance Ldz represents the magnetic field; Cdz represents the electric field between the transmission line and ground.

2) Characteristic impedance: The main characteristic parameters of the transmission line include characteristic impedance, transmission speed and transmission delay. Among them, the characteristic impedance not only affects crosstalk and reflection. In the following simulation, the line width, line spacing and terminal impedance of the transmission line are all

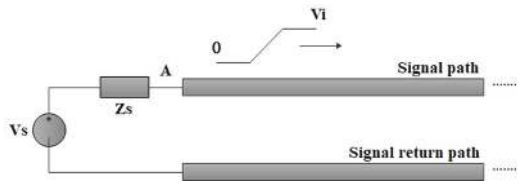

Fig. 3. Signal transmission on the transmission line

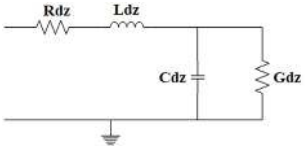

Fig. 4. Differential model of transmission line

related to it. The characteristic impedance Z_0 of the transmission line represents the ratio of voltage to current at different points of the transmission line, that is, $Z_0 = V/I$. Figure 5 represents two equivalent ways of transmission line. Through these two equivalent methods, the characteristic impedance of an infinite transmission line can be extracted or derived.

Assume that the characteristic impedance of the transmission line is equal to the termination impedance Z_0. The input impedance of the equivalent circuit in Figure 5(a) can be obtained and the equation (7) can be obtained. For simplicity, the differential length dz is replaced by a short length $\triangle$Z. Derive as follows:

The series impedance of the length $\triangle$Z is set to,

$$j\omega L\left(\Delta Z\right) + R\left(\Delta Z\right) = Z\Delta Z \tag{1}$$

The parallel impedance of length $\triangle$Z is set to,

$$j\omega C\left(\Delta Z\right) + G\left(\Delta Z\right) = Y\Delta Z \tag{2}$$

Assuming that the load impedance is equal to the characteristic impedance, then,

$$Z_{\text{input}} = Z_0 \frac{\left(Z_0 + Z\Delta Z\right)\frac{1}{Y\Delta Z}}{Z_0 + Z\Delta Z + \frac{1}{Y\Delta Z}} \tag{3}$$

$$Z_0\left(Z_0 + Z\Delta Z + \frac{1}{Y\Delta Z}\right) = \left(Z_0 + Z\Delta Z\right)\frac{1}{Y\Delta Z} \tag{4}$$

$$\Rightarrow Z_0\left(Z_0 + Z\Delta Z\right)Y = Z \tag{5}$$

$$\Rightarrow Lim\left[Z\right] = YZ_0^2 \tag{6}$$

Therefore,

$$Z_0 = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{7}$$

(R is Ω/m; L is H/m; G is S/m; C is F/m; ω is rad/m)

Because R and G are much smaller than the other terms, the characteristic impedance is usually approximately,

$$Z_0 = \sqrt{L/C} \tag{8}$$

Of course, formula (8) is mainly convenient for simple theoretical analysis and simulation calculations later. In the actual design, in order to obtain the maximum accuracy, the PCB line impedance still needs to be calculated by using a two-dimensional electromagnetic field solver.

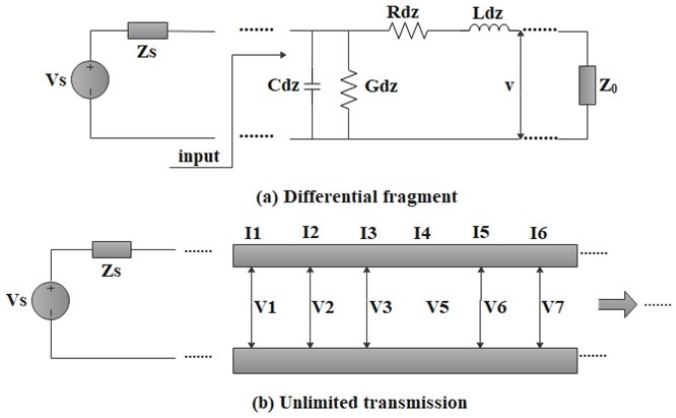

Fig. 5. The methods of extracting characteristic impedance

B. Optimal design of Layout and wiring space

After sorting out the factors that affect the signal integrity of the transmission line, this section first sets out to optimize the design of the layout space. Compared with the traditional "snake-shaped wiring" way, the "spiral wiring" way transfers part of the microstrip into a stripline through a blind hole. According to the amplitude L_p and the gap S, this section will compare the layout and wiring space required by the "spiral wiring" way and the "snake-shaped wiring" way before and after optimization. The schematic diagram of the comparison parameters is shown in Figure 6:

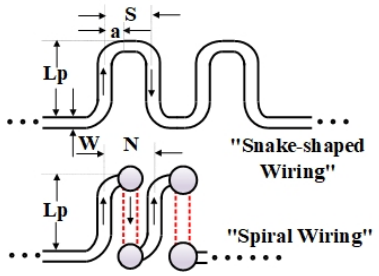

Fig. 6. Schematic diagram of comparison parameters (single-ended transmission line)

In the figure, a represents the distance from the path to the corner; W represents the line width of the transmission line; N represents the gap of the optimized waveform; the gray circle represents the blind vias, and its diameter is equal to a; the black solid line represents the top wiring; the red dotted line indicates the signal layer wiring.

In PCB design, the amplitude and gap of the "snake-shaped wiring" way are generally set to $L_p = 5w$, $S = 3a$. The amplitude of the optimized "spiral wiring" way remains unchanged, and the gap is set to $N = 2a$. Therefore, when the amplitude L_p of the two ways remains unchanged, the wiring

space required for the two waveforms in the "snake-shaped wiring" way in the figure is $5W9a$. However, the wiring space required for the two waveforms in the "spiral wiring" way is only $5W5a$. This shows that the "spiral wiring" way optimizes the layout of the PCB to a certain extent. Secondly, compared with the single-layer wiring of the "snake-shaped wiring" way, the multi-layer wiring of the "spiral wiring" way also improves the flexibility of PCB circuit layout.

In addition, in the PCB design process such as high-speed and ultra-high-speed sampling boards, there are many related components (such as FPGA (Field Programmable Gate Array) modules, DDRX modules, D/A conversion modules, etc.). They are mostly distributed on the top layer. Therefore, the layout and wiring between the top-level components are very difficult and compact. However, compared to the top layer, the signal layer only needs wiring, so its space is much looser. Therefore, for PCB designers, the value of optimizing the layout and wiring space of the top layer is far greater than the impact of introducing blind vias and occupying the space of layout and wiring of the signal layer.

C. Optimal design and simulation of crosstalk

Crosstalk is essentially the voltage noise caused by the mutual inductance and mutual capacitance formed by the mutual coupling between too many transmission line [12]. These crosstalk noises will change the performance of the transmission line in the bus, such as the characteristic impedance and transmission speed of the transmission line. Changes in performance will have a certain impact on the timing and signal integrity of the system. Two important causes of crosstalk on the circuit board are mutual inductance Lm and mutual capacitance Cm. When the signal propagates on the transmission line, the entire signal path and return path are distributed with electric and magnetic fields. At the same time, they extend to the surroundings. If the distance between the two transmission lines is too close, capacitive coupling and inductive coupling will occur, which in turn will cause crosstalk problems [13]. As shown in Figure 7. The current caused by mutual capacitance flows in both directions of the interfered line. The current caused by mutual inductance flows from the far end of the interfered line to the near end cite [14].

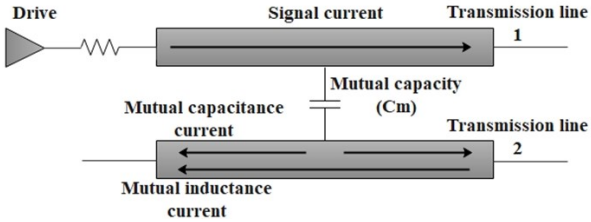

Fig. 7. Schematic diagram of crosstalk

1) Suppressing crosstalk: There are many factors that affect crosstalk in the equal-length wiring process. But there are three main factors, namely the coupling length of the transmission line, the loop area (coupling area) and the line spacing. When the layout and wiring space is tight but the crosstalk between the lines must be considered, the spacing of the transmission line is often set to 3 times the line width. This is the minimum wiring principle for transmission line. Therefore, the optimal design of equal-length wiring of single-ended transmission line mainly analyzes the crosstalk problem from the coupling length and loop area of the transmission line.

As shown in Figure 6 above. Regardless of the "snake-shaped wiring" way or the "spiral wiring" way, the loop area of the transmission line is proportional to the coupling length and the number of coupled transmission line. When the line spacing is constant, the longer the coupling length and the more coupled transmission line, the larger the loop area. At the same time, by the voltage and current noise formula:

$$V_{noise,}L_m = L_m \frac{dI_{driver}}{d_t} \tag{9}$$

$$I_{noise,}C_m = \frac{dV_{driver}}{d_t} \tag{10}$$

It can be seen that the crosstalk between transmission line is also proportional to the loop area. Compared with the "snake-shaped wiring" way, the "spiral wiring" way not only reduces the coupling number and coupling length of the transmission line, but also greatly reduces the loop area between the transmission line. This wiring way suppresses the crosstalk between the transmission line to a certain extent. It also improves the transmission performance of the transmission line

2) Advantages of the "spiral wiring" way: In a crosstalk-free transmission line, the current of transmission line should be in the center of the line, and current density of the center line is the largest. As shown in Figure 8. In the "snake-shaped wiring" way, the currents of adjacent lines have the same magnitude but opposite directions. There will be mutual inductance between these two lines. The effect of mutual inductance is to draw the center current path (A current line) of the two lines closer to each other (B or C current line). Among them, the A and B current lines are approximately the same length, and the C current line is the shortest. But if the actual current line is C, the current path will be greatly shortened. For a line with a line width of 6 mils, about each such "U shape" will cause about 1 ps acceleration. If a line has 10-20 such "U-shaped", there will be an acceleration of 10-20ps, and the delay of the transmission line will increase. This can cause timing problems [15].

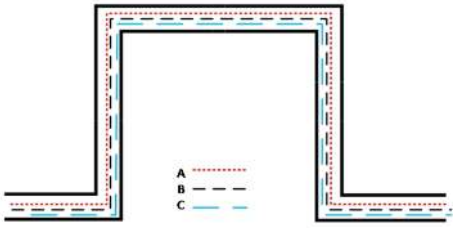

Fig. 8. Current path in the line

However, the "spiral wiring" way converts part of the microstrip into the stripline of the signal layer. This reduces the mutual inductance between the lines to a certain extent, thereby reducing the delay caused by the mutual inductance.

In addition, the "spiral wiring" way can also reduce the impact of characteristic impedance changes and transmission speed changes of transmission line. This change is caused by the coupling between the lines. Through the calculation formula of the characteristic impedance of the transmission line: $Z_0 = \sqrt{L/C}$, and the calculation formula for the transmission speed of the transmission line:

$$V_p = \sqrt{LC} \tag{11}$$

It can be deduced that $V_p = ZC$. That is, when the line is a stripline, the changes of L and C are balanced with each other. The propagation speed of the stripline will not change as a result. And compared with the microstrip, the stripline basically has no forward crosstalk, and the backward crosstalk will not increase when the coupling length reaches the saturation length. So just control the coupling length within the saturation length.

3) Simulation of crosstalk: Before the simulation, the parameters of stackup of the PCB (as shown in Figure 9) have been set. The simulation parameters of the transmission line can be calculated from this. According to the approximate calculation formula of the characteristic impedance of the transmission line:

When the top layer (top layer) $L = 415.0pH$ and $C = 164.0fF$, the characteristic impedance of the transmission line $Z0 = 50.3\Omega$, which is approximately 50Ω. The line width of the simulated transmission line is $W = 6.50mils$. When the SIG layer (signal layer) $L = 754.8pH$ and $C = 303.1fF$, the characteristic impedance of the transmission line $Z_0 = 49.9\Omega$, which is approximately 50Ω. The line width of the simulated transmission line is $W = 7.50mils$.

Basic | Dielectric | Metal | Z0 Planning | Manufacturing | Custom View

	Visible	Color	Pour Draw Style	Layer Name	Type	Usage	Thickness mils	Er
1					Dielectric	Solder Mask	0.5	3
2	☑		Solid	TOP	Metal	Signal	1.8	<Auto>
3					Dielectric	Substrate	4	4
4	☑		Solid	GND01	Metal	Plane	1.2	<Auto>
5					Dielectric	Substrate	5	3.8
6	☑		Solid	PWR	Metal	Plane	0.6	<Auto>
7					Dielectric	Substrate	36	3.7
8	☑		Solid	SIG	Metal	Signal	0.6	<Auto>
9					Dielectric	Substrate	5	3.8
10	☑		Solid	GND02	Metal	Plane	1.2	<Auto>
11					Dielectric	Substrate	4	4
12	☑		Solid	BOTTOM	Metal	Signal	1.8	<Auto>
13					Dielectric	Solder Mask	0.5	3

Fig. 9. Simulation Stackup Structure

Therefore, LineSim (simulation of schematic diagram) is performed according to the set stackup parameters. The simulation model of the "spiral wiring" way is shown in Figure 10. The active device model is usually a SPICE (Simulation Program with Integrated Circuit Emphasis) model or an IBIS (Input/Output Buffer Information Specification) model. Because using the IBIS model for PCB simulation is faster than using the SPICE model, and can also provide some readable ASCII format data [16] [17], this article uses the IBIS model for schematic modeling.

Among them, the input simulation model is the Virtex7 chip of Xilinx FPGA series. The output simulation model is the MT41K256M16HA chip of Micron's DDR3 series. The simulation excitation source is PRBS7 (Pseudo-Random Binary Sequence) of 1.6Gbps/s. Output signal waveforms of LineSim of Crosstalk optimization design is shown in Figure 11:

In the figure, the blue line (circle) represents the output signal waveform before optimization; the red line (triangle) represents the output signal waveform after optimization.

It can be seen from the figure that compared to the waveform before optimization, the transmission delay of the optimized waveform is more in line with the delay requirements of DDR3. At the same time, the optimized waveform also proves that the transmission line has better signal quality. This shows that the "spiral wiring" way has suppressed the crosstalk between the lines and improved the signal integrity of the transmission line. This also proves that the crosstalk optimization design on the coupling length, coupling area and line spacing of the transmission line is feasible and reliable.

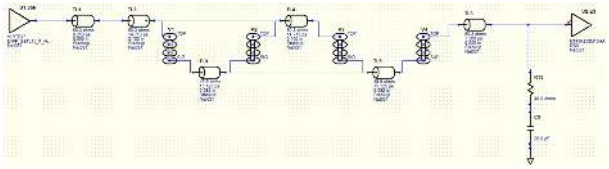

Fig. 10. Simulation model of the "Spiral wiring" way

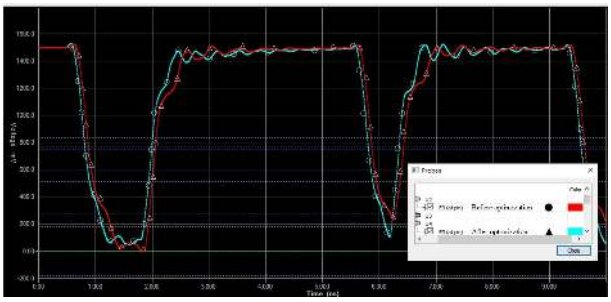

Fig. 11. Output signal waveforms of optimized crosstalk

D. Optimal design and simulation of reflection

Signal reflections on transmission line can have a significant negative impact on signal quality. The main reason for the phenomenon of signal reflection is the discontinuous line impedance. As shown in Figure 12. If the impedance at the end of the transmission line does not match the characteristic impedance of the transmission line. When the incident wave V_i reaches the terminal resistance Z_t, a part of the voltage signal $V_i\rho$ will be reflected to the driving end. At the same time, it will superimpose the incident wave on the transmission line to produce a voltage with a total amplitude of $V_i\rho + V_i$. In addition, the reflected component returning to the drive end may cause retroreflection again. This reflection and retroreflection process will continue until the transmission line reaches a stable state [18]. In this process, signal reflections from the transmission line will cause signal overshoot, undershoot and ringing. This will cause severe signal distortion. Compared

with the "snake-shaped wiring" way, the impedance discontinuity of the "spiral wiring" way is mainly considered from two factors: blind vias and the introduction of stripline.

1) Optimal design of blind vias: The impact of blind vias has two main aspects. One is that the blind vias itself has a certain length. If the length of the blind vias is obvious, it should be included in the line length. Secondly, the impedance of PCB is discontinuous due to the line passing through the blind vias. When a high-speed signal passes, the parasitic capacitance of the blind vias will cause that the signal rise time to be prolonged and the transmission speed slow down. The parasitic inductance will weaken the filtering function of the power supply bypass capacitor. They can cause crosstalk and EMI (Electromagnetic Interference) problems [19].

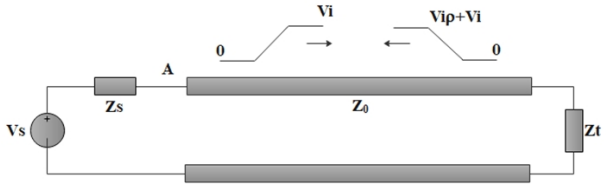

Fig. 12. Schematic diagram of signal reflection of transmission line

The parasitic capacitance estimation formula of the blind vias is:

$$C = (0.0555 D_K T D_1) / (D_2 - D_1) \tag{12}$$

In the formula (12), C is the parasitic capacitance (p_F); T is the PCB thickness (mm); D_k is the dielectric constant; D_1 is the pad diameter (mm); D_2 is the anti-pad diameter (mm).

The parasitic inductance estimation formula of blind vias is:

$$L = 0.2h \left[\ln (4h/d) + 1\right] \tag{13}$$

In the formula (13), L is the parasitic inductance (nH); h is the blind vias length (mm); d is the blind vias diameter (mm).

According to the impedance formula $Z_0 = \sqrt{L/C}$, and substituting formulas (12) and (13) into it. There are:

$$Z_0 = \sqrt{0.2h \left[\ln (4h/d) + 1\right] \times \frac{D_2 - D_1}{0.0555 D_K T D_1}} \tag{14}$$

It can be seen from formula (14) that the blind vias impedance value can be increased by increasing the anti-pad D_2 or reducing the pad D_1 or reducing the diameter of the vias. So as to reduce the signal reflection caused by the impedance discontinuity [20].

2) Optimal design of introducing stripline: In the PCB manufacturing process, compared to microstrip of the outer layer, the stripline of the inner layer has better the uniformity of copper thickness. The uniformity of the etched line width is also better. Therefore, the transmission line can have good transmission performance in the signal transmission process. In order to reduce the signal reflection caused by introducting stripline, the "spiral wiring" way uses butt-joint ways [21] to match the characteristic impedance. For single-ended transmission line, the following butt-joint ways that can reduce reflection are summarized (as shown in Figure 13):

a: The butt-joint way of series connection on source terminal: Its butt-joint way is to directly connect a resistor R in series with the source terminal.

b: David-Nan butt-joint way: the load terminal of the transmission line is connected to a pull-up resistor R_1 and a pull-down resistor R_2.

c: The butt-joint way of parallel connection on source terminal: add a pull-down resistor R to the load terminal of the transmission line, the other terminal of the resistor is grounded. The resistance value is set to the characteristic impedance of the transmission line.

d: RC butt-joint way: the load termination of transmission line is connected with parallel resistance and capacitance.

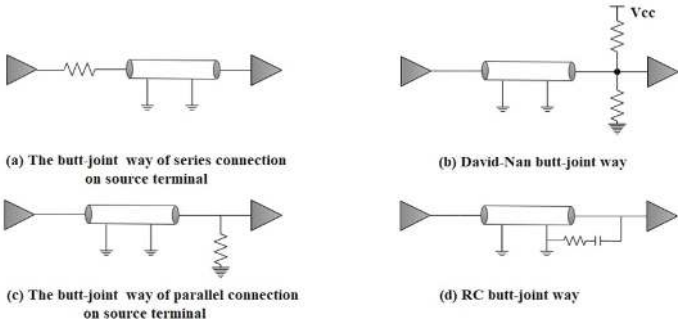

Fig. 13. Four butt-joint ways to eliminate reflection

3) Simulation of reflection's optimization design: For the four butt-joint ways, this article uses LineSim which reference to the stackup parameters set earlier. The simulation waveforms is shown in Figure 14:

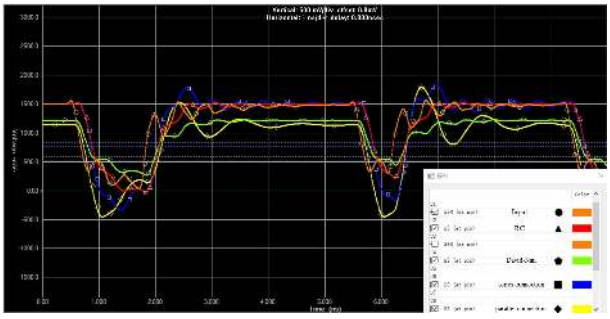

Fig. 14. Waveforms comparison of four butt-joint ways

In the figure, U_1 is the input signal waveform of the transmission line (orange, circular); U_2 is the output waveform (red, triangle) of RC butt-joint way; U_4 is David-Nan butt-joint way output waveform (green, pentagonal); U_6 is the output waveform (blue, rectangle) of the butt-joint way of series connection on source terminal; U_8 is the output waveform (yellow, diamond) of the butt-joint way of parallel connection on source terminal.

As can be seen from the figure, compared to the other termination ways, RC butt-joint way has the best output waveform. When reducing transmission line reflections, its

waveform remains roughly the same as the input waveform. This proves that its transmission line has good transmission performance. Secondly, if RC butt-joint way is used. The DC current on the transmission line will be small, thereby reducing the circuit power consumption. Although the RC butt-joint way could have a delay effect, the size of the delay is related to the value of R and C. Its value can be adjusted appropriately to meet the design requirements. Therefore, in the optimization design of the ”spiral wiring” way, the best impedance matching way to reduce signal reflection is the RC butt-joint way.

E. Simulation and verification of the ”spiral wiring” way's PCB

Through the above three aspects, this section optimizes the design of the ”spiral wiring” way and does a schematic diagram simulation and verification of the optimized design. However, in addition to schematic simulation, PCB simulation is also an indispensable part of simulation and verification. The mutual verification of BoardSim (PCB simulation) and LineSim can ensure the feasibility and reliability of the optimized design part. This article uses a PCB of the DDR3 chip strip to verify the optimized design of the ”spiral wiring” way described above. The PCB design of the DDR3 chip strip complies with JEDEC (Joint Electron Device Engineering Council) standards. The simulation models of the input and output are set according to the LineSim model. The simulation excitation source is PRBS7 at 1.6Gbps/s.

The optimization design of the ”spiral wiring” way takes the A6 address line of the PCB as the optimization object. First of all, through the PADS Layout (PowerPCB) design software, the original ”snake-shaped wiring” way of the A6 address line (as shown in Figure 15) is designed as the ”spiral wiring” way. Then, perform BoardSim on the optimized A6 address line (as shown in Figure 16) through HyperLynx simulation software. The output signal waveform of the A6 address line after the simulation is shown in Figure 17. In the figure, the blue line (circle) represents the input signal waveform; the red line (triangle) represents the output signal waveform.

It can be seen from the figure that the output waveform of the ”spiral wiring” way is approximately the same as the input waveform. The transmission line delay is approximately 0.5ns. This ensures that the transmission line has good signal quality. At the same time, the mutual verification of PCB simulation and schematic simulation ensures the feasibility and reliability of the ”spiral wiring” way, which is designed from the three aspects of layout, crosstalk and reflection.

Fig. 15. A6 address line of the ”snake-shaped wiring” way

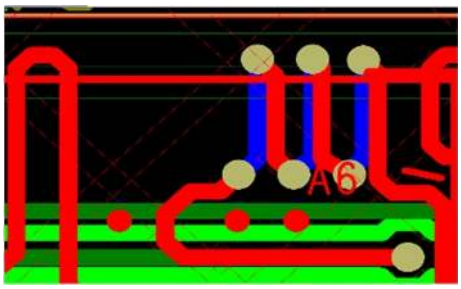

Fig. 16. A6 address line of the ”spiral wiring” way

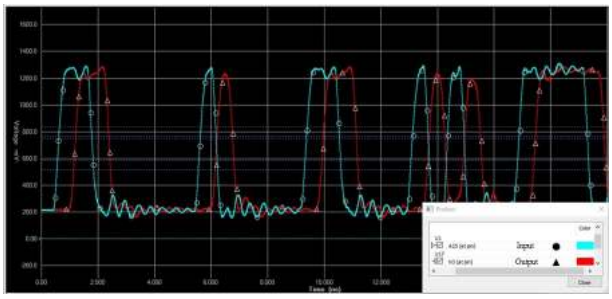

Fig. 17. Simulation waveform of A6 address line's output signal

IV. THE ”DOUBLE SPIRAL WIRING” WAY AND ITS SIMULATION

The ”double spiral wiring” way (as shown in Figure 18) is an optimization of the traditional equal-length wiring ways of differential transmission lines. Compared to single-ended transmission line in point-to-point mode, differential transmission lines in differential mode also have their pros and cons.

The obvious disadvantage of a differential transmission lines is that it requires two signal lines. This leads to a big problem whether it is to layout or route on the PCB. If the signals on the board are all differential signals, we can imagine how desperate the circuit designer will be.

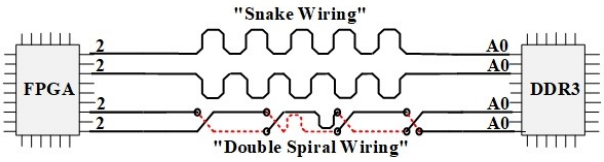

Fig. 18. The ”double spiral wiring” way

But the wide application of differential transmission lines must have its advantages, which can be said from the following four aspects:

(1) Differential signals are very effective in low-level applications.

(2) Since the differential signal is two signals with the same level and opposite phases, there is no need for a reference plane as a signal loop, and no ground plane or power plane continuity and integrity.

(3) Differential signal has natural immunity to signal interference, and its transmission signal quality is better.

(4) Compared with single-point signals, the switching sequence of differential signals will be more accurate.

Whether it is a single-ended transmission line or a differential transmission lines, the equal-length wiring of the transmission line will be a problem that the designer must consider. The wiring rule of the differential transmission lines is to require two signal lines to be of equal length and equal spacing. Therefore, the wiring requirements of the equal-length wiring way need to be met when optimizing. Compared with the single-ended transmission line, the differential transmission lines has a strong anti-interference ability. the crosstalk problem caused by the equal-length wiring part has little effect on it. Therefore, the ”double spiral wiring” way only needs to analyze and design from two aspects: optimizing layout space and reducing reflection.

A. Optimal design of Layout and wiring space

Refer to the ”spiral wiring” way, although the equal-length wiring of the differential transmission line is two signal lines, it can also be analyzed and optimized through the two parameters of L_p and S. The schematic diagram of the comparison parameters between the ”double spiral wiring” way and the ”snake-shaped wiring” way is shown in Figure 19. In the figure, the meaning of each parameter is the same as the parameters of the ”spiral wiring” way.

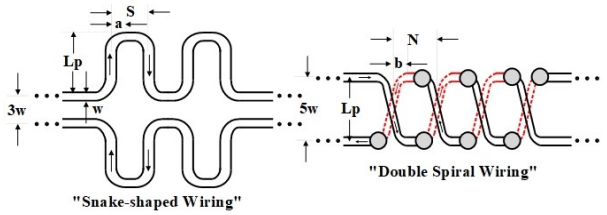

Fig. 19. Schematic diagram of comparison parameters (differential transmission lines)

In the differential transmission lines, the amplitude and gap of the ”snake-shaped wiring” way are still set to $L_p = 5W$ and $S = 3a$. However, the waveform of the optimized ”double spiral wiring” way does not extend outward but inward. Its amplitude and gap are $L_p = 5W$, $N = 3a$. Therefore, when the ”snake-shaped wiring” way expands the space of $2 \times 5W \times 9a$ outside the signal line, the ”double spiral wiring” way only extends the space of $2W \times 9a$ into the signal line. This greatly optimizes the layout and wiring space resources of the TOP layer.

Next, as shown in Figure 18 above. When the layout and wiring space cannot meet the wiring requirements, the ”double spiral wiring” way and the ”snake-shaped wiring” way can be combined for wiring. In this way, the two equal-length wiring ways can be combined to further optimize the space. Compared with the ”spiral wiring” way, the optimization design of the ”double spiral wiring” way has a more significant optimization effect on the space of the top layer. The wiring way is also more flexible. In addition, when there are multiple single-ended lines running side by side on the PCB, you can also use the ”double spiral wiring” way for wiring (as shown in Figure 20). This not only saves layout and wiring space. At the same time, it can also reduce the coupling between signal lines, reduce crosstalk between lines, and improve signal transmission quality.

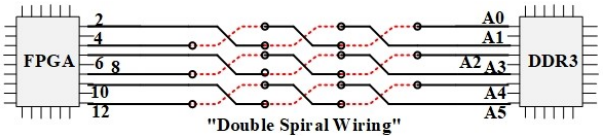

Fig. 20. Layout of multiple single-ended transmission line

B. Optimal design of reflection

Refer to the optimized design for reducing reflection in the ”spiral wiring” way, the ”double spiral wiring” way can also increase the blind vias impedance by increasing the anti-pad or reducing the pad or reducing the blind vias diameter. Thereby reducing the signal reflection caused by the blind vias. Therefore, this section only needs to consider the influence of the introduction of the stripline on the signal reflection. Different from the single-ended transmission line butt-joint way, in order to better suppress the signal reflection of the differential transmission lines, there are two impedance matching butt-joint ways: Pi-type network butt-joint way and T-type network butt-joint way (as shown in Figure 21). The Pi-type network butt-joint way is very effective for differential receiver to receive differential signals. The T-type network butt-joint way has a significant effect on the single-ended receiver receiving differential signals. Because this article mainly simulates the strobed differential signal of DDR3, the impedance matching way of the differential receiver is used.

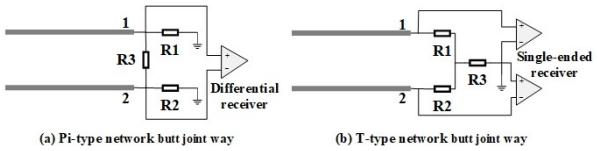

Fig. 21. Two butt-joint ways of differential transmission lines

In the case of differential mode transmission, the input signal is a differential signal with the same value and opposite polarity. When using the Pi-type network butt-joint way, each signal uses R_3 and R_1 (or R_2) in parallel for impedance matching. That is, R_3 can be divided into two series resistors, each of which is $R_{3/2}$. During the differential mode transmission, the two series resistors become a virtual alternating current (AC) ground. At this time, each matching resistance is:

$$R_1 = R_2 = Z_{even} \tag{15}$$

$$R_3 = \frac{2Z_{even}Z_{odd}}{Z_{even} - Z_{odd}} \tag{16}$$

Then, perform LineSim on the differential transmission lines of the Pi-type network butt-joint way according to the stacking parameter settings described above. The simulation model is shown in Figure 22:

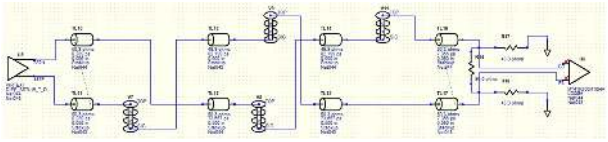

Fig. 22. Simulation schematic diagram of ”double spiral wiring” way

Differential transmission lines have three transmission signals at the receiving end (output signals with the same amplitude and opposite polarity and differential signals). Therefore, it is not suitable to use the waveform analysis method of a single-ended transmission line to judge its quality of transmission signal. The eye diagram is a graph displayed by a series of digital signals accumulated on the oscilloscope, which contains a wealth of information. The measurement of bit error rate can be judged by the degree of eye diagram closure. The greater the degree of eye diagram opening, the lower the bit error rate, and vice versa, the higher the bit error rate. At the same time, the better the signal quality and the lower the bit error rate, the larger the eye diagram will open. The eye diagram can visually see the influence of noise and inter-symbol crosstalk and estimate the pros and cons of the entire system through the characteristics of the overall digital signal [22]. Therefore, this article will analyze the signal quality of differential transmission lines through eye diagrams. The eye diagram of the output signal of the Pi-type network butt-joint way is shown in Figure 23:

According to the analysis of the figure, the eye diagram of the differential output signal has a large degree of opening and low jitter. This shows that the transmission line has good signal quality while also meeting the signal requirements of DDR3. Secondly, the simulation results also show that in the optimization design of the ”double spiral wiring” way, the use of the Pi-type network butt-joint way has a good effect on signal reflection.

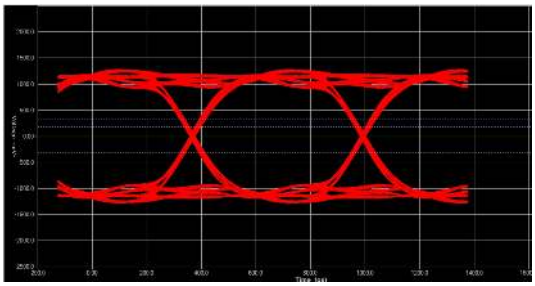

Fig. 23. The eye diagram of the output signal of the Pi network butt-joint way

C. simulation and verification of the ”double spiral wiring” way's PCB

According to the simulation parameter setting of the ”spiral wiring” way, perform BoardSim for the ”double spiral wiring” way. Its optimized design takes the strobe differential signals DQS7 and DQS7b of the DDR3 as optimized objects. First, it designed the ”snake-shaped wiring” way part of the original PCB's DQS7 and DQS7b (as shown in Figure 24) as a ”double spiral wiring” way (as shown in Figure 25). Then, perform PCB simulation for the optimized ”double spiral wiring” way. The eye diagram of the output signal of DQS7 and DQS7b after simulation is shown in Figure 26.

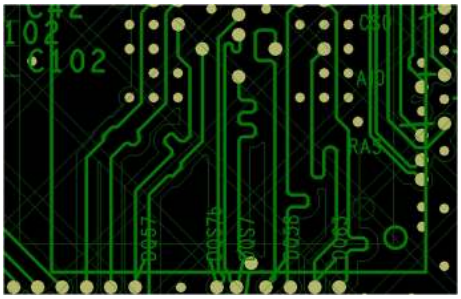

Fig. 24. DQS7 and DQS7b of the ”snake-shaped wiring” way

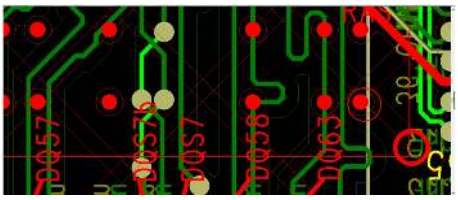

Fig. 25. DQS7 and DQS7b of the ”double spiral wiring” way

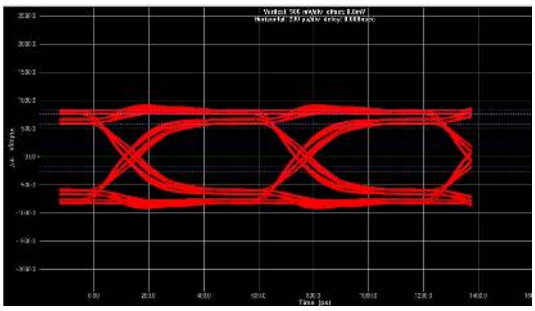

Fig. 26. Simulation eye diagram of DQS7 and DQS7b output signal

From the analysis of the figure, the ”eyes” in the eye diagram have a large degree of opening. Although there is a certain amount of jitter, the transmission performance of the differential transmission lines is generally good. Secondly, the mutual confirmation of the PCB simulation results and the schematic simulation results also proved the feasibility and reliability of the optimal design of the ”double spiral wiring” way.

V. Conclusions

With the advent of the 5G era and the era of artificial intelligence, high-speed PCB as a hot topic in the field of electronic circuit design and manufacturing research will receive more attention. At the same time, with the rapid development of integrated circuit and semiconductor technology, high-speed PCB will also move towards smaller size and better performance. Therefore, how to balance the layout and signal integrity of the components on the PCB will directly

affect the electrical performance, reliability and stability of the high-speed PCB. Based on the relevant theories of signal integrity, this article proposes two optimized design ways for equal-length wiring of transmission line: the ”spiral wiring” way and the ”double spiral wiring” way. After analyzing the design theory, design and simulation are carried out from three aspects: optimizing layout space, suppressing crosstalk and reducing signal reflection. The results show that the two new equal-length wiring ways not only improve the transmission performance of the transmission line, but also prove that its optimized design is feasible and reliable.

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