Two-Path Quadrature Cascaded Band-Pass Sigma-Delta Modulators

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***Abstract*—This paper presents a two-path design of quadrature band-pass ΣΔ modulators and discusses the architectural level implementation issues for power reduction. The methodology uses an architecture which locks IF frequencies to the sampling frequency. The basic delay based solution is converted into integrator based solution for the implementation. Robustness of the structure against the mismatch is analyzed and a two-path quadrature cascaded modulator is proposed to alleviate signal band gain error tone. Simulations at the behavioral level verify the architecture implementation and the effectiveness of the approach.**

***Index Terms*—Analog-to-Digital conversion, band-pass ΣΔ modulation, Image band, complex filters, Two-path, MASH, Cascaded, quadrature,**

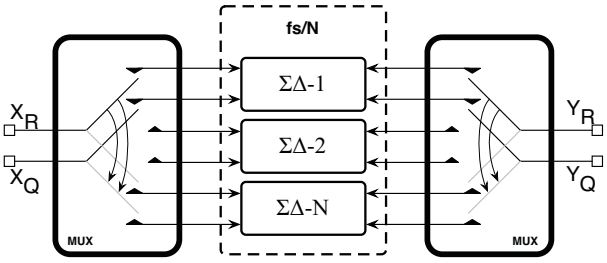

Fig. 1. Generic N-path quadrature band-pass ΣΔ modulator.

I. Introduction

Performance of a ΣΔ modulator can be improved by increasing the over sampling ratio (OSR) and/or increasing the order of filter and/or increasing the quantizer levels. However increasing the OSR results in additional burden on the op-amp bandwidth requirement, eventually dissipating more power. Increasing the quantizer levels beyond 4-5 bits is not good, as the number of comparators needed rises exponentially. Performance of the modulator can also be increased by increasing the order of the filter, however beyond second order, modulator requires extensive stability analysis and the number of op-amps rises. Thus for a given power and SNR requirement [1], combination of the above factors should be carefully optimized. On the other hand power requirement in the system level can be reduced by N-path [2] architectures. Research activities in N-path architectures are still in the development stage. A few of the existing architectures in the literature are in Pipeline ADC [3], low pass [4] and band-pass [5] sigma delta modulators. This paper explores the N-path design techniques in quadrature band-pass ΣΔ modulators. Fig. 1 shows a general N-path quadrature [6] band-pass ΣΔ modulator, where each path operates N-times slower than the sampling frequency (f_s) of the complete system. The solution is attractive for reducing the system power requirement as the power consumption of an op-amp is proportional to square of the ($\alpha * f_s$) and for an N-path system the op-amp power requirement is proportional to square of ($\alpha * f_s/N$) at the cost of duplicating the hardware N-times. Here α lies between 3 and 5, since for a discrete time implementation, op-amp bandwidth requirement varies in that range. Additional duplication of the hardware can be saved by careful interleaving operation without compromising the settling requirement.

This paper presents an architectural solution for signal band gain mismatch tones in quadrature ΣΔ modulators. The provision of placing a zero in the image band helps reducing the injection of quantization noise from image band to signal band. The paper is organized as follows. Section II reviews the basic scheme for a delay based second order quadrature modulator and conversion of the delay based scheme into an integrator based solution. Section III describes the two-path scheme with mismatch analysis. Section IV introduces cascaded architectural solution to the gain mismatch problems. Finally, Section V draws some conclusions.

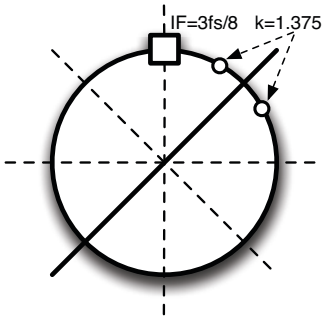

Fig. 2. z-plane, zero placement of a second order quadrature modulator.

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II. Synthesis of noise transfer function

One of the possible quadrature noise transfer function (NTF) [7] with two zeros on the unit circle is given by

$$NTF = 1 - z^{-1}k(1 + j) + jz^{-2} \quad (1)$$

For k=1.375 with IF at $f_N/4$, the positions of the zeros are as shown in Fig. 2. Synthesized architecture for the above NTF is as shown in Fig. 3. More details about the architecture can be found in [7]. The next step is to convert the delay based solution to integrator based architecture for the implementation. In-order to convert the delay to integrator based architecture consider the quadrature delay based filter of the modulator shown in Fig. 3. For simplicity, Fig. 4(a) shows the delay based filtering part of the modulator without injection of quantization error. Since the implementation is done in discrete time, choppers and integrators are used to map the output using iterative use of the following equation.

$$\begin{aligned} Z_{R1}(n+1) &= X_{R1}(n) - Y_{Q1}(n) \\ Z_{Q1}(n+1) &= X_{Q1}(n) + Y_{R1}(n) \\ Y_{R1}(n+1) &= Z_{R1}(n) \\ Y_{Q1}(n+1) &= Z_{Q1}(n) \end{aligned} \quad (2)$$

Fig. 4(b) shows the integrator based scheme. The outputs of the two filters are the same, hence these two topologies are equivalent. The derived topology is extended to incorporate injection of the quantization error between the delays in order to complete the mapping from delay based system to integrator based one. The complete integrator system is as shown in Fig. 5. Ideal spectrum output of Fig. 5 exactly matches with that of Fig. 3.

III. Two-path second order quadrature modulator.

In case of a ΣΔ modulator, the main power consuming blocks are op-amps used to implement integrators, which increases with the order of the filter. For N=2, number of path will be two and each paths will operate at a frequency of $fs/2$, hence the power consumption of each op-amp is reduced to $(f_s)^2/4$. Second order NTF requires z^{-2} term, which are implemented by cascading of two integrators, which operates at a frequency $(\alpha * f_s)$. It is advantageous to implement the z^{-2} term by two first order integrators operating in two-paths at a frequency $(\alpha * f_s/2)$, which also reduces the

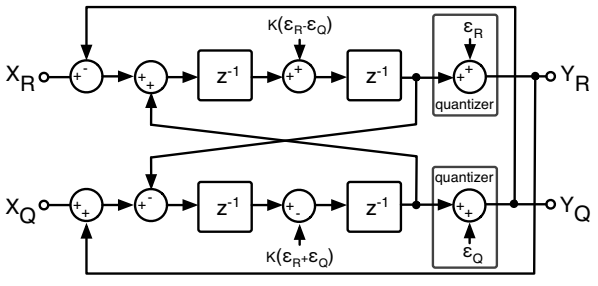

Fig. 3. Second order quadrature band-pass ΣΔ architecture for NTF = $1 - z^{-1}k(1 + j) + jz^{-2}$ with IF = $f_N/4$.

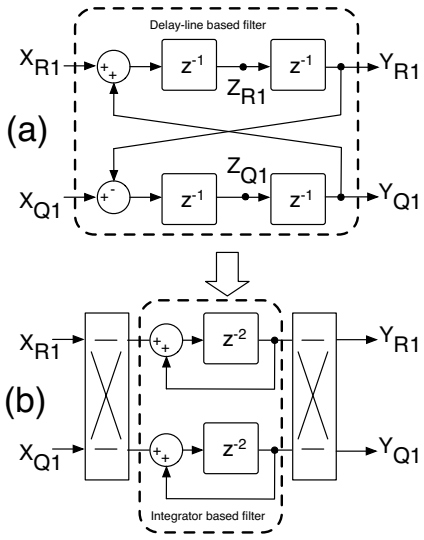

Fig. 4. Conversion from Delay based to Integrator based scheme

settling requirement of the op-amp. Hardware requirement can be reduced by careful time-interleaving operation without compromising settling requirement. This is possible due to unit delay between even and odd paths. Thus one op-amp is sufficient to implement a second order z^{-2} term. Fig. 6 shows the two-path implementation quadrature architecture of Fig. 5. The architecture is referred to system clock frequency f_s, hence each integrator is shown with a z^{-2} term, in reality four op-amps (two for R path, two for Q path) are required for two-path operation with each path operating at a frequency of $f_s/2$.

The output spectrum of the modulator considering the gain mismatch is shown in Fig. 7. Image tone due to nominal mismatch in the feedback path is problematic like any conventional higher order quadrature modulator as quantization error will be leaked from image band to signal band. For a second order quadrature modulator with IF at $f_N/4$ and reasonable bandwidth (OSR=9), image band quantization error is still shaped by the quadrature filter, hence leakage is negligible. Leakage would be critical if the IF is at $f_N/2$ as quantization error reaches maximum power in the image. However for a two-path integrator based architecture, gain mismatch tones fall in the signal band, which is undesirable in a sensitive receiver architecture. Thus the power reduction advantage of a two-path quadrature architecture is limited by tones in the signal band.

The leakage of image band quantization error into the signal band can be reduced by placing a zero in the image band [6] [8] or selecting a signal band near to the image band [9]. The same solution is applicable in the reduction of gain mismatch error. This can be verified by the following quadrature band-pass design. Consider the following NTF with one zero in the signal band and one zero in the image band given by

$$NTF = 1 - z^{-1}k - z^{-2} \quad (3)$$

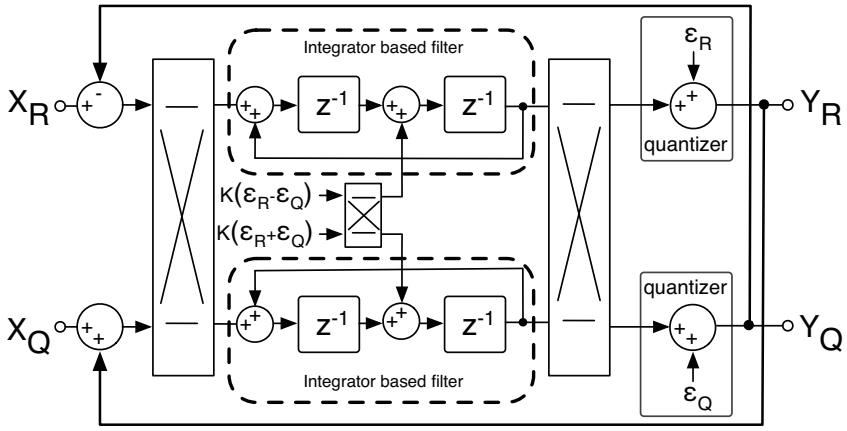

Fig. 5. Integrator based architecture.

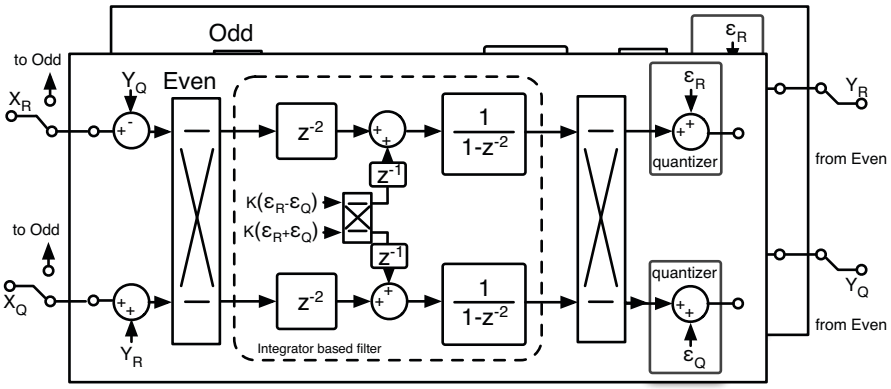

Fig. 6. Two-path implementation scheme.

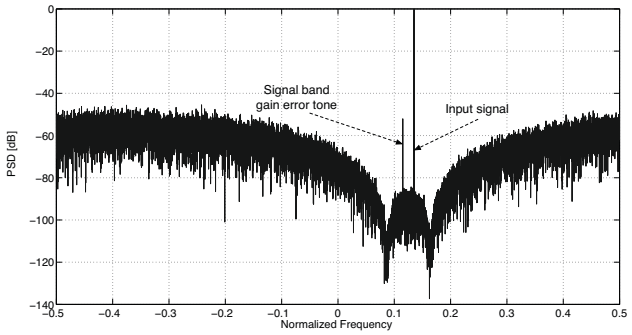

Fig. 7. PSD of the $f_N/4$-IF second order quadrature band-pass modulator with 1% mismatch.

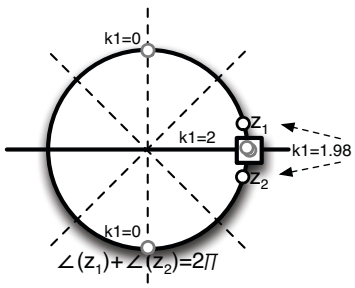

Fig. 8. Zero analysis of the $2f_N$ architecture.

For $k = 1.98$ with IF at $2f_N$, the positions of the zeros are as shown in Fig. 8. Synthesized architecture for the above NTF is as shown in Fig. 9. The architecture is converted from delay based to integrator based scheme and implemented in two-path scheme as shown in Fig. 10 based on the previously derived design steps. Output spectrum considering gain mismatch and feedback path mismatches are shown in Fig. 11. It is worth noting that there is no gain mismatch tones in the signal band.

However the present design has only two zeros, hence placing one zero in the image band will reduce the effectiveness of signal band shaping. One possible solution is to

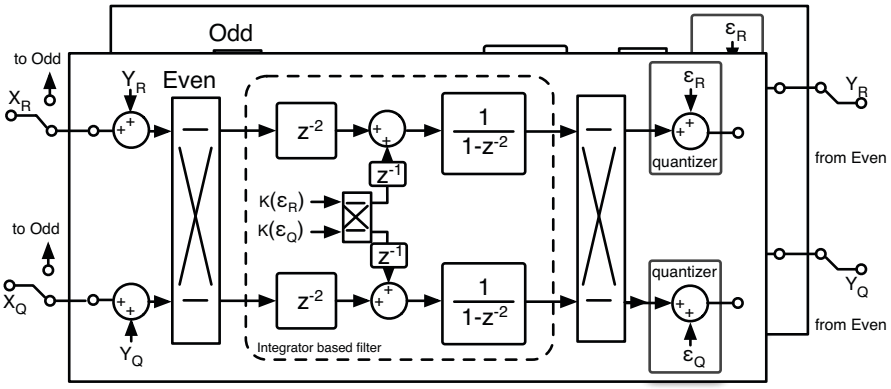

Fig. 10. Two-path implementation of the $2f_N$ architecture.

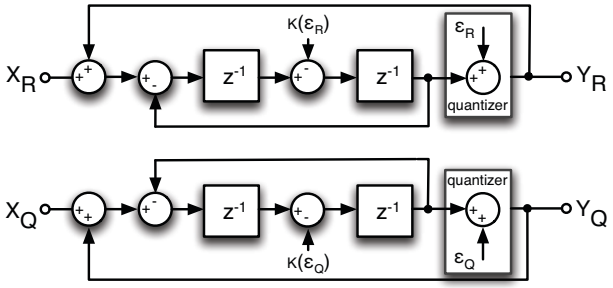

Fig. 9. Second order quadrature band-pass ΣΔ architecture for NTF = $1 - z^{-1}k - z^{-2}$ with IF = $2f_N$.

extend the architecture to a third order such that two zeros are used for signal band shaping and one zero for image band suppression. This requires a z^{-1} to z^{-3} conversion, which is possible only if, N=3 with the advantage of each path operating at a frequency of $f_s/3$. However path mismatch analysis would be complicated and single coefficient control over three zeros would not be possible. In-order to retain the advantage of the signal coefficient control over the two zeros,

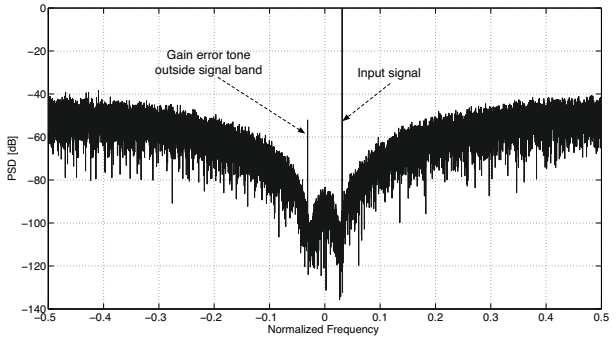

Fig. 11. PSD of the two-path $2f_N$/-IF second order quadrature band-pass modulator with 1% mismatch.

a two-path 2-2 cascaded architecture is proposed.

IV. Two-path 2-2 quadrature cascaded ΣΔ Modulators

Cascading [9] is a well known technique to improve the stability compared to direct synthesis of higher order modulators. The proposed 2-2 quadrature cascaded ΣΔ modulator is shown in Fig. 12, where an individual second order sigma delta modulator is implemented with two-path topology. The proposed modulator has an advantage of placing the zeros using two independent zero controlling coefficients, whereas a fourth order single stage modulator requires three coefficients without locking of IF to sampling frequency. Stability requirement is not a problem with 2-2 cascaded scheme as the architecture inherently uses a second order modulator, which is not a case for the conventional fourth order modulator. The conventional processing used for cascaded scheme cancels the quantization noise of the R and Q paths of the first modulator and obtains a quadrature output $Y = Y_R + j \cdot Y_Q$ for a quadrature input $X = X_R + j \cdot X_Q$. Noise transfer functions NTF_1 and NTF_2 of Fig. 12 is given by

$$NTF_1 = 1 - z^{-1}k_1 - z^{-2} \quad (4)$$

$$NTF_2 = 1 - z^{-1}k_2(1 + j) + jz^{-2} \quad (5)$$

$$Y = Xz^{-4} + \varepsilon_2(NTF_1)(NTF_2) \quad (6)$$

where $\varepsilon_2 = \varepsilon_{2,R} + j \cdot \varepsilon_{2,Q}$.

The first modulator uses the architecture proposed in Fig. 10 with zero placements as shown in Fig. 12 for $k_1 = 1.98$ and the second modulator uses the architecture shown in Fig. 6 with zero position as shown in Fig. 12 for $k_2 = 1.375$. The effective IF of the architecture is given by $f_N/8$.

Output spectrum of the modulator considering the mismatch is as shown in Fig. 13. Inset of Fig. 13 confirms the effectiveness of the cascaded architecture with input signal applied at $2f_N+\delta$ and gain error tone at $2f_N-\delta$. There is no gain mismatch tones in the signal band as image band is suppressed by the first stage of the modulator and second stage further increases the bandwidth of the modulator. It is worth mentioning that interchanging stages creates problems as shown in Fig. 14.

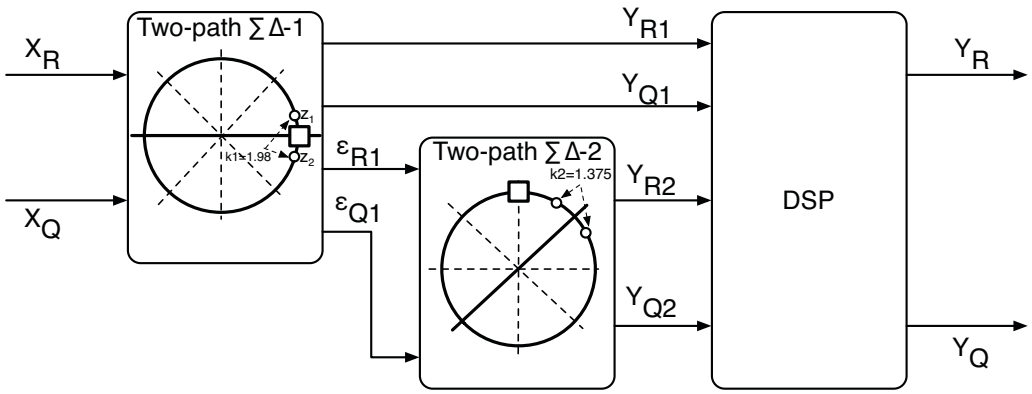

Fig. 12. Proposed cascaded architecture with zero placement to alleviate gain error tone in the signal band.

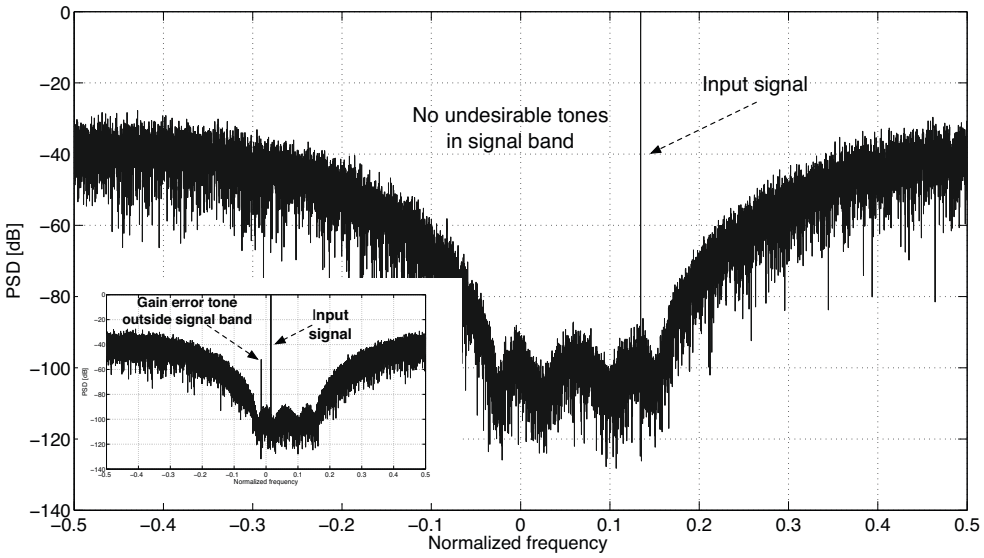

Fig. 13. PSD of the cascaded architecture with IF at $7f_N/8$ using zero position of Fig. 12. Inset shows that for input signal at $2f_N + \delta$ the gain error tone is at $2f_N - \delta$, outside the signal band.

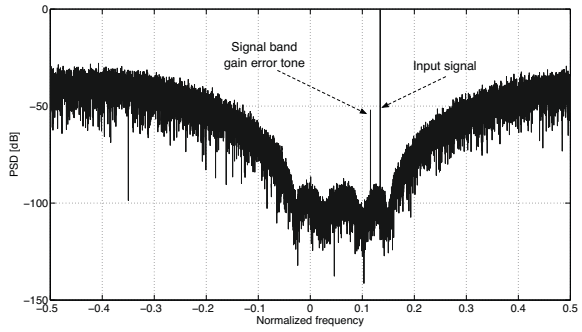

Fig. 14. PSD of the cascaded architecture with IF at $f_N/8$ using interchanged modular stages Fig. 12.

Gain mismatch of the first stage creates tones in the signal band and the second stage image suppression is not useful as tones are already leaked by the first stage. Hence it is important to suppress the gain error tone in the first stage. An additional benefit of this topology is the suppression of image band quantization error. This reduces the leakage of the quantization error from image band to signal band.

V. Conclusion

This work extensively studied power reduction techniques in the system level using N-path quadrature band-pass ΣΔ modulators. Two-path design of integrator based quadrature ΣΔ modulator has been proposed. Gain mismatch problem associated with the architecture is analyzed and solution is provided by using a two-path second order band-pass architecture

with one zero in the image band. Higher performance without compromising stability was demonstrated through a proposed two-path 2-2 cascaded architecture. Cascaded architecture holds the advantage of the locking of IF to sampling frequency f_S. The effectiveness of the proposed scheme was proved by simulations at the behavioral level.

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