# Two-Port Analysis of Switched-Capacitor Networks Using Four-Port Equivalent Circuits in the $z$-Domain

CARL F. KURTH, FELLOW, IEEE, AND GEORGE S. MOSCHYTZ, FELLOW, IEEE

*Abstract*—**In a previous publication by the authors it was shown how switched-capacitor (SC) networks can be analyzed by using nodal charge equations. The result was a description of SC networks as time-variant sampled-data networks which led to a four-port equivalent circuit representation in the $z$-domain. In this paper, the four-port representation is expanded by considering six basic building blocks for the design of any general active or passive SC network. With the four-port equivalent circuit representation, traditional two-port analysis tools, such as the transmission matrix and two-port transfer functions, can be used conveniently. An SC-filter design example is given and the measured response is shown to coincide with the response predicted by the theory.**

## I. Introduction

In a previous publication by the authors [1] switched-capacitor (SC) networks were analyzed using nodal charge equations. As a result, a closed form representation of SC networks as time-variant sampled-data networks was obtained. Physically, the topology of an SC network is changed periodically between two states, assuming that the switches change position at even and odd switching times, periodically. By transforming the time-varying equations into the $z$-domain, it was shown that any SC network can be represented by a four-port, in which even and odd time slots correspond to an input–output port combination, respectively. A general method was presented with which the appropriate four-port equations can be obtained. The equations can be used for analysis in the frequency domain, either by an analytical computation or by means of a numerical analysis with a computer. Simple examples, however, indicated that without a computer the analysis rapidly becomes unmanageable for only slightly more complex SC networks. Even with the use of a computer, the loss of insight may be a deterrent for the use of this general method. This fact and the desire to use traditional network analysis tools, like transmission matrices, transfer functions, $y$- and $z$-matrices, etc., stimulated the development of the four-port equivalent circuits presented in this paper. As will be shown, they readily provide insight into the performance of SC networks in the frequency domain. In addition, they open avenues for the exact synthesis of more complex SC networks, without the need for opamp isolation. Thus, for example, cascades of passive SC networks can now be analyzed in a manner similar to the analysis of passive $LC$ two-ports [2]–[4].

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## II. Building Block Analysis of SC Networks

### A. The Six Basic Passive Building Blocks

Any passive SC network can be constructed with the six basic building blocks shown in Fig. 1. The nonswitched shunt capacitor and its dual are the only storage elements in SC networks. Periodically switched capacitors act like resistors, since their memory is destroyed during the closing period of the switch. The ideal switches can be considered as zero-valued capacitors with a switch in parallel. By connecting the building blocks in Fig. 1 in tandem, or by combining parallel, serial, and tandem connections of the building blocks, arbitrary higher order passive SC networks can be obtained. In what follows, the equivalent four-port circuits will be derived in the $z$-domain. They are listed in Table I. As we shall see, the interconnection of these equivalent four-port circuits will readily provide insight into the behavior of more complex SC networks in the frequency domain. This building block analysis follows the idea developed in Section V and particularly Fig. 14 of [1].

### B. Four-Port Equivalent Circuits of Passive SC Building Blocks

*1) Shunt Capacitor:* The shunt capacitor shown in Fig. 2 can be described as a two-port in the time domain by applying the nodal charge equations as explained in Section III-A of [1]

$$\begin{aligned} v_1(n) &= v_2(n) \\ Cv_1(n) &= i_1(n) - i_2(n) + Cv_1(n-1) \end{aligned} \tag{1}$$

or in the $z$-domain in matrix form

$$\begin{bmatrix} V_1(z) \\ I_1(z) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ C & (1-z^{-1}) \quad 1 \end{bmatrix} \begin{bmatrix} V_2(z) \\ I_2(z) \end{bmatrix}. \tag{2}$$

The matrix in (2) can be interpreted as an equivalent two-port, as shown in Fig. 2. It consists of two compo-

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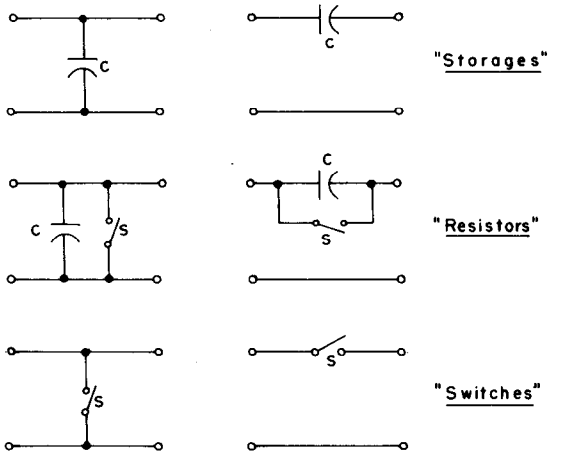
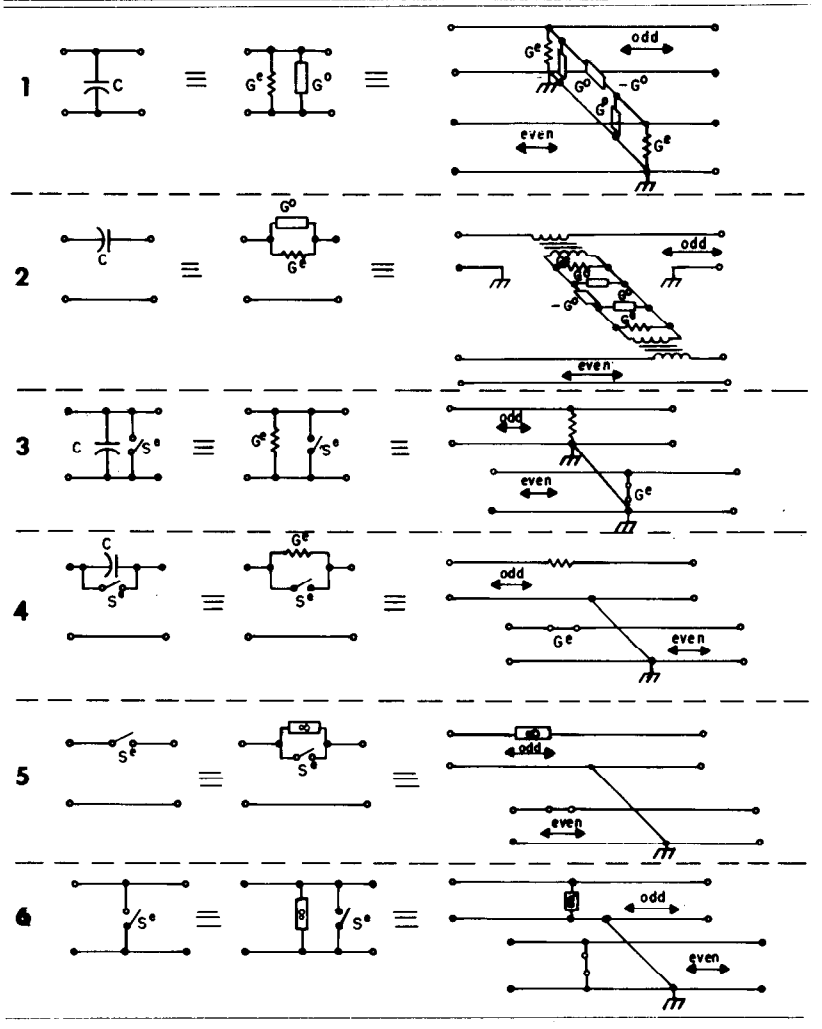



Fig. 1. The six basic components (building blocks) in SC networks.

TABLE I
EQUIVALENT CIRCUITS FOR SIX BASIC ELEMENTS IN SC FILTERS




nents, namely, a conductance

$$G^e = C \tag{3a}$$

and a storage element

$$G^o = -Cz^{-1} \tag{3b}$$

where the superscripts $e$ and $o$ denote even and odd, respectively.

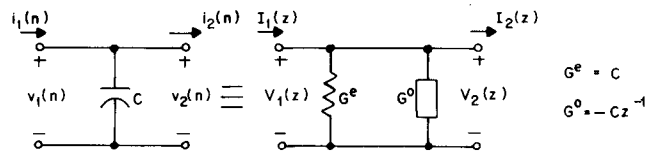



Fig. 2. Shunt capacitor and its two-port equivalent circuit in the $z$-domain.

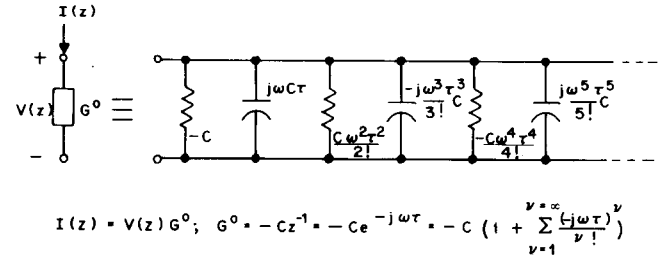



Fig. 3. Equivalent circuit of the storage element $G^o$: the storistor.

This storage element, or "storistor," has the property of delaying the current flowing through it by one delay unit $z^{-1}$ with respect to a voltage sample applied across the element. It was found to be a useful device throughout the following analysis. Its equivalent circuit, shown in Fig. 3, is derived by a series expansion of $z^{-1} = e^{-j\omega\tau}$. Notice that for $\omega\tau \ll 1$ the storistor can be approximated by a negative conductance $(-C)$ in parallel with a physical capacitor $C$, an approximation which becomes convenient later when comparing SC networks with conventional $RC$ networks.

In continuing the analysis of the shunt capacitor, (2) can be rewritten by using $G^e = C$ and $G^o = -Cz^{-1}$ as an even and odd part, respectively, of the $z$-transform in the matrix of (2)

$$\begin{bmatrix} V_1(z) \\ I_1(z) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ G^e + G^o & 1 \end{bmatrix} \cdot \begin{bmatrix} V_2(z) \\ I_2(z) \end{bmatrix}. \tag{4a}$$

This can be expanded into a four-port equation by separating even and odd parts corresponding to the derivations given in Section III-B of [1]. By observing that

$$X^e \cdot Y^o = W^o, \quad X^e \cdot Y^e = W^e, \quad \text{and} \quad X^o \cdot Y^o = W^e$$

and with $I_i(z) = I_i^e(z) + I_i^o(z)$ and $V_i(z) = V_i^e(z) + V_i^o(z)$ the four-port transmission matrix for a shunt capacitor is obtained from (4a), namely

$$\begin{bmatrix} V_1^e \\ V_1^o \\ I_1^e \\ I_1^o \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ G^e & G^o & 1 & 0 \\ G^o & G^e & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_2^e \\ V_2^o \\ I_2^e \\ I_2^o \end{bmatrix}. \tag{4b}$$

The remaining task is to find an equivalent four-port circuit for (4b) [5]. The input and output voltages in the even as well as in the odd path of this four-port must be equal, i.e.,

$$V_1^e = V_2^e, \quad V_1^o = V_2^o.$$

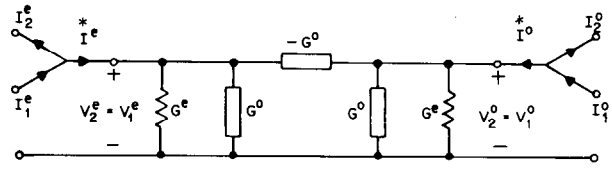



Fig. 4. Two-port equivalent circuit for (6). Link between even and odd path for shunt capacitor.

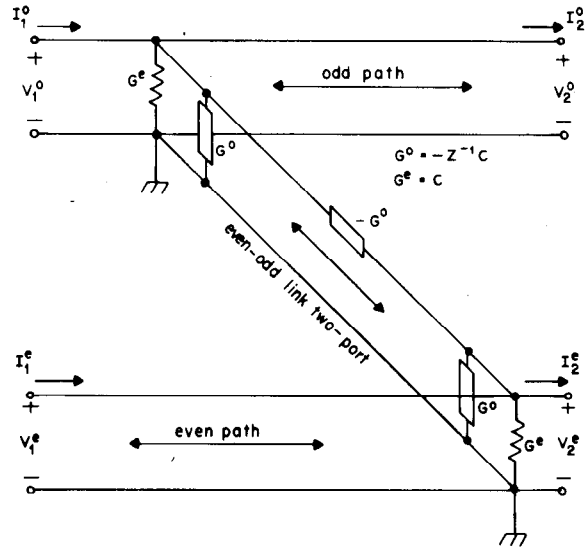



Fig. 5. Four-port equivalent circuit for shunt capacitor.

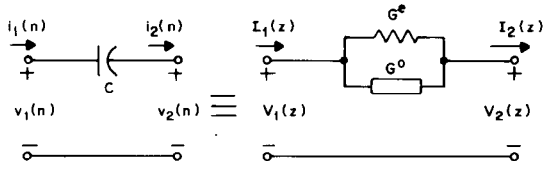



Fig. 6. Series capacitor and its two-port equivalent circuit in $z$-domain.

Furthermore, from (4b), the even and odd parts are related as follows:

$$\begin{bmatrix} I_1^e \\ I_1^o \end{bmatrix} = \begin{bmatrix} G^e & G^o \\ G^o & G^e \end{bmatrix} \cdot \begin{bmatrix} V_2^e \\ V_2^o \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_2^e \\ I_2^o \end{bmatrix} \tag{5}$$

or

$$\begin{bmatrix} I_1^e - I_2^e \\ I_1^o - I_2^o \end{bmatrix} = \begin{bmatrix} \overset{*}{I}{}^e \\ \overset{*}{I}{}^o \end{bmatrix} = \begin{bmatrix} G^e & G^o \\ G^o & G^e \end{bmatrix} \cdot \begin{bmatrix} V_2^e \\ V_2^o \end{bmatrix}. \tag{6}$$

$\overset{*}{I}{}^e$ and $\overset{*}{I}{}^o$ denote the current differences $I_1^e - I_2^e$ and $I_1^o - I_2^o$, respectively. Equation (6) can now be interpreted as the two-port shown in Fig. 4; the $\pi$-configuration was chosen for convenience, since it yields simple expressions for the elements. By redrawing the equivalent circuit shown in Fig. 4 one obtains the final four-port equivalent circuit for the shunt capacitor as shown in Fig. 5, and Table I.

*2) Series Capacitor:* The series capacitor shown in Fig. 6 can be described as a two-port in the time domain with

the following equations:

$$i_1(n)=i_2(n)$$
$$C\{v_1(n)-v_2(n)\}=i_1(n)+C\{v_1(n-1)-v_2(n-1)\}. \quad (7)$$

With the even and odd elements $G^e$ and $G^o$, as defined in (3a) and (3b), the corresponding equation in the $z$-domain can be obtained

$$\begin{bmatrix} V_1(z) \\ I_1(z) \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{G^e+G^o} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_2(z) \\ I_2(z) \end{bmatrix}. \quad (8)$$

This can be interpreted as an equivalent two-port in the $z$-domain, as shown in Fig. 6.

Applying the same technique, separating even and odd parts, and multiplying out the terms in (8), yields the four-port transmission matrix. From (8)

$$(G^e+G^o)(V_1^e+V_1^o)=(G^e+G^o)(V_2^e+V_2^o) + I_2^e+I_2^o$$
$$I_1^e+I_1^o=I_2^e+I_2^o$$

and in matrix form, with even and odd parts already separated

$$\begin{bmatrix} G^e & G^o \\ G^o & G^e \end{bmatrix} \cdot \begin{bmatrix} V_1^e \\ V_1^o \end{bmatrix} = \begin{bmatrix} G^e & G^o \\ G^o & G^e \end{bmatrix} \cdot \begin{bmatrix} V_2^e \\ V_2^o \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_2^e \\ I_2^o \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} I_1^e \\ I_1^o \end{bmatrix} = \begin{bmatrix} I_2^e \\ I_2^o \end{bmatrix}. \quad (10)$$

Writing (9) in terms of voltage differences

$$\begin{bmatrix} I_2^e \\ I_2^o \end{bmatrix} = \begin{bmatrix} G^e & G^o \\ G^o & G^e \end{bmatrix} \cdot \begin{bmatrix} V_1^e-V_2^e \\ V_1^o-V_2^o \end{bmatrix} = \begin{bmatrix} G^e & G^o \\ G^o & G^e \end{bmatrix} \cdot \begin{bmatrix} \overset{*}{V}{}^e \\ \overset{*}{V}{}^o \end{bmatrix}. \quad (11)$$

This equation is similar to the one obtained for the shunt capacitor in (6). The only difference is that current differences occur here instead of voltage differences. Thus the even and odd path of the series-capacitor four-port is linked by the same two-port, as shown in Fig. 4. However, the port vectors are the voltage differences and the input and output currents, $I_1^e=I_2^e$ and $I_1^o=I_2^o$. This is demonstrated in Fig. 7.

The entire four-port equivalent circuit corresponding to (9) and (10) is shown in Fig. 8 and Table I. With the help of ideal transformers it is possible to make $I_1^e=I_2^e$ and $I_1^o=I_2^o$, independent of one another. The voltage differences still appear across the input ports of the link

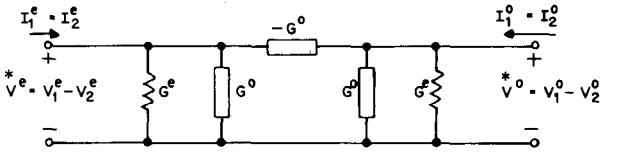



Fig. 7. Two-port equivalent circuit for (11). Link between even and odd path for series capacitor.

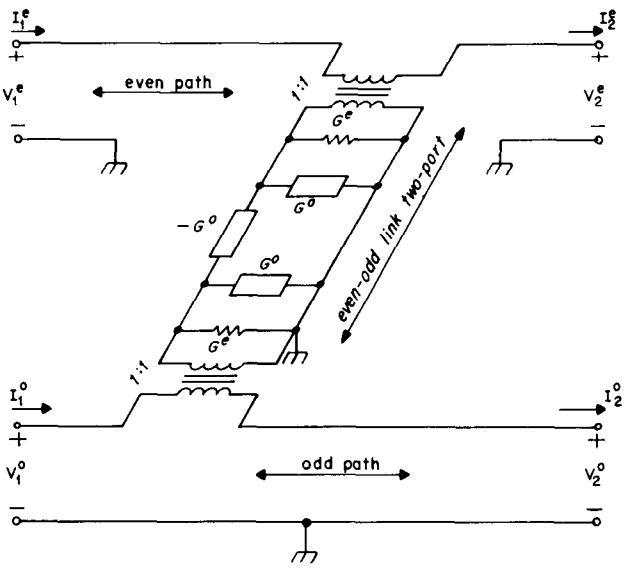



Fig. 8. Four-port equivalent circuit for series capacitor.

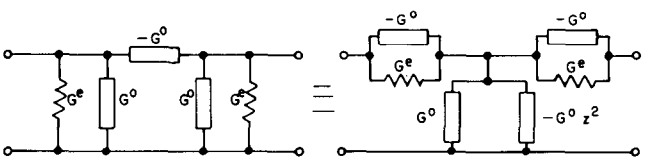



Fig. 9. $\Pi \leftrightarrow T$ equivalents for two-port linking even and odd paths in capacitor equivalent circuits.

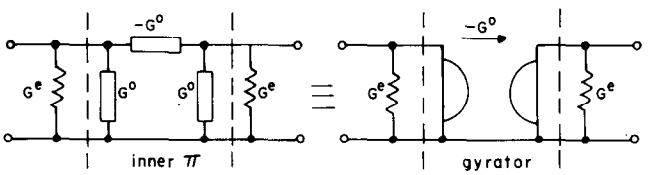



Fig. 10. Gyrator equivalent circuit for the LTP in storage elements.

two-port (LTP), i.e., the two-port which represents the link between the odd and even path.

In Figs. 9 and 10 two other equivalent circuits for the LTP are shown. Whichever is the most convenient can be used in any given analysis.

*3) Switched Shunt Capacitor:* The switched shunt capacitor (line 3, Table I) is described by two sets of equations in the time domain. At even times the switch $S^e$ is closed and the equations are

$n=$ odd

$$v_1(n)=v_2(n)+0\cdot i_2(n)$$
$$i_1(n)=Cv_2(n)+i_2(n)$$

$n$ = even

$$v_1(n) = v_2(n) + 0 \cdot i_2(n)$$
$$0 \cdot i_1(n) = Cv_2(n) + 0 \cdot i_2(n).$$

The two equations can be combined by using the switching function $A^o(n)$, as introduced in Section 3.1 of [1]. For all times $n$

$$v_1(n) = v_2(n)$$
$$A^o(n) i_1(n) = Cv_2(n) + A^o(n) i_2(n). \tag{12}$$

With formula (2) in Table II of [1], (12) can be transformed into the $z$-domain

$$V_1^e + V_1^o = V_2^e + V_2^o$$
$$I_1^o = CV_1^e + CV_1^o + I_2^o. \tag{13}$$

Separating the even and odd parts in (13) yields the following set of equations, which correspond to the four-port equivalent circuit as shown in Table I:

$$V_1^e = V_2^e$$
$$V_1^o = V_2^o$$
$$I_1^o = CV_2^o + I_2^o$$
$$0 = V_2^e. \tag{14}$$

Note when the switch $S^e$ is closed, i.e., $n$ = even, the corresponding path is shorted. This erases all memory on the capacitor, which appears as a shunt resistor in the path corresponding to those time slots in which the switch is open.

In Table I the equivalent circuit corresponds to a switch $S^e$, which is closed at even times. For a switch $S^o$, which is closed at odd times, the short and the shunt resistor are interchanged between the two paths. Notice that due to the elimination of memory on the capacitor, the equivalent circuit in the $z$-domain has no link between the even and odd paths. This is typical for all building blocks comprising a parallel capacitor-switch combination.

*4) Switched Series Capacitor:* The switched series capacitor can be analyzed similarly to the shunt configuration. The resulting equivalent four-port is shown on line 4 in Table I.

*5) Shunt Switch and Series Switch:* The shunt switch and the series switch are obtained from the SC circuits by letting the capacitor value equal zero. Consequently, the resistor values in the open-switch paths of the four-port equivalent circuits will go to infinity (see lines 5 and 6 in Table I). By using these equivalent circuits for the ideal switches, the nontransmitting signal path can easily be identified, therefore permitting the transmitting path to be analyzed directly. This procedure will provide the key for the reduction of the four-port equivalent circuit to the two-port equivalent circuit of an SC network.

### C. Active Elements, Sources, and Loads

*1) Controlled Sources:* The simplest active element in an SC network is a voltage-controlled voltage source. It has no storage capability. Its equivalent circuit in the time domain, and its corresponding four-port equivalent circuit is shown in Fig. 11.

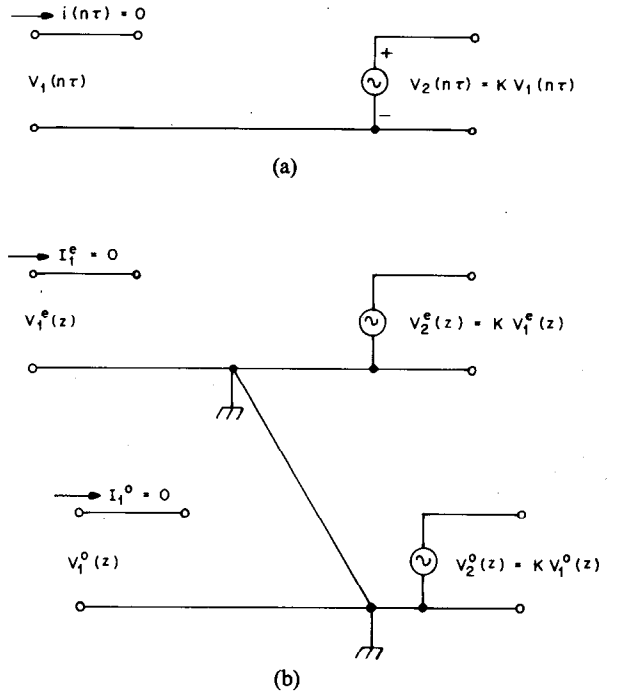



Fig. 11. (a) Voltage-controlled voltage source. (b) Four-port equivalent circuit

A current-controlled voltage source in an SC network is somewhat more complex, since it must have the property of a capacitor, namely that of building up a voltage in response to a current surge $i(n)$. It must therefore follow the equation

$$\frac{1}{C} i(n) = v(n) - v(n-1). \tag{15}$$

If the memory is periodically erased by a switch (similar to an SC), (15) reduces to

$$v(n) = \frac{1}{C} i(n) \tag{16}$$

where $n$ is either only even or only odd.

The equivalent circuit for a current-controlled voltage source with memory according to (15) and its four-port equivalent circuit is shown in Fig. 12. In Fig. 13 the corresponding circuits for a current-controlled voltage source without memory are shown. The timing of the switch determines in which path the resistor or the short occurs. The use of controlled sources will be shown later in an example.

*2) Driving Voltage Sources:* As has been assumed throughout this analysis, an SC network must be driven from a sampled voltage or current source. This is achieved by sampling a continuous source by a periodically operated switch. The impedance of a voltage source must be very small, that of a current source very large in order to guarantee an instantaneous voltage buildup across the capacitor of the SC network.

If the source is to have a finite source resistance this must be simulated by an SC combination as indicated in

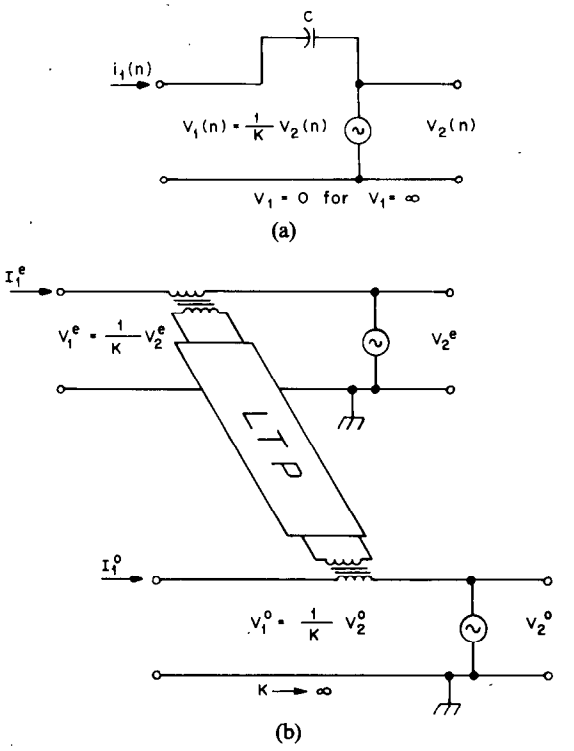



Fig. 12. (a) Current-controlled voltage source with storage. (b) Four-port equivalent circuit.

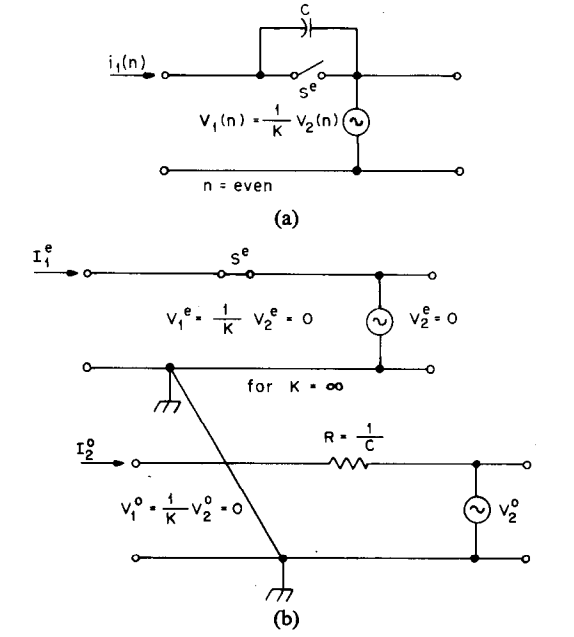



Fig. 13. (a) Current-controlled voltage source without memory. (b) Four-port equivalent circuit.

Fig. 14(a). There, the continuous voltage source $v_o(t)$ (whose output impedance is assumed to be practically zero) is sampled by the switch $S^e$. The capacitor $C_s$ and switch $S^o$ represent the source resistor for the SC network. Using the four-port equivalent circuits of Table I, the equivalent circuit of Figure 14(b) is obtained. Since the sampling switch $S^e$ is closed at even times, the current

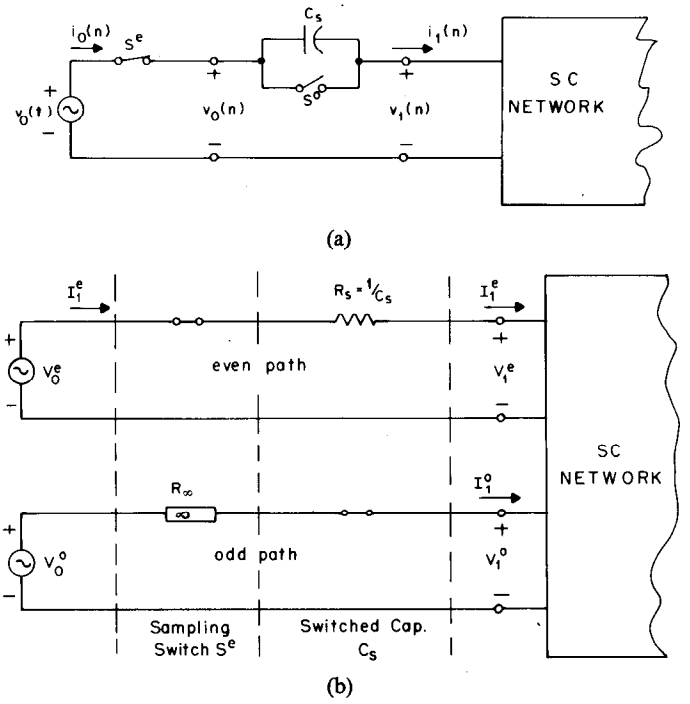



Fig. 14. (a) Sampled voltage source with simulated source resistor $R_s$. (b) Four-port equivalent circuit.

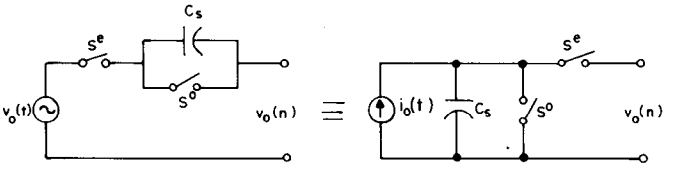



Fig. 15. Thevenin's equivalence for SC network sources.

$I_1^o$ is zero in the odd path and the source is completely disconnected during odd time slots. Thus its zero impedance does not cause any loading effect. The input signal is fed only into the even path, with the source resistance $R_s = C_s^{-1}$. Note that the timing of the sampling switch (even or odd time slot) determines along which path the four-port equivalent circuit of the SC network is driven. The switch across the capacitor $C_s$ has to be closed 180° out of phase with the sampling switch, in order to eliminate the memory of $C_s$.

*3) Driving Current Sources:* It is interesting to note that Thevenin's theorem is applicable. By redrawing the driving circuit in Fig. 14(a) with a current source and a capacitor in parallel, which is periodically charged and discharged by a subsequent sampling switch $S^e$, the same driving conditions for the SC network can be accomplished. This suggests a general "Thevenin's Equivalent" for SC sources as shown in Fig. 15. The current source corresponding to $v_0(t)$ then results as

$$i_0(n) = v_0(n)/R_s = v_0(n) \cdot C_s. \tag{17}$$

*4) Loading Resistors:* Similarly, loading resistors can be simulated by a switched shunt capacitor. By setting the

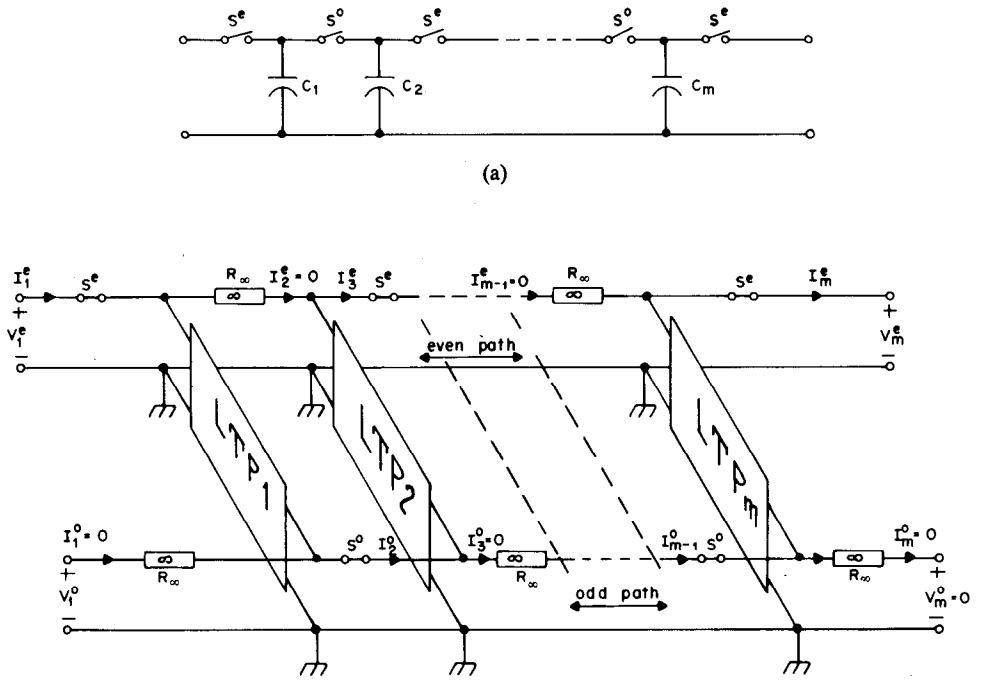



Fig. 16. (a) Cascade of alternating series switches and shunt capacitors. (b) Four-port equivalent circuit.

voltage source in Fig. 14 to zero a typical resistive loading condition is obtained.

### D. Cascading SC Building Blocks

After the four-port equivalent circuits for the basic SC building blocks have been established, they can readily be connected in cascade. Clearly a cascade of shunt or series capacitors, i.e., storage elements, merely leads to a parallel (or series) connection of LTP's without providing any filtering effect. However, alternating the tandem connection of storage elements with switched elements results in SC networks that are suitable for filtering purposes.

In Fig. 16(a) the cascade connection of $m$ alternating shunt capacitors and series switches is shown. Using the equivalent circuits in Table I the four-port equivalent circuit is obtained (Fig. 16(b)). Notice that the timing of the switches alternates along the chain. This leads to the alternating position of the $R_\infty$'s in the even and odd path. Since the currents through the $R_\infty$'s are zero, the signal flows through the network like through a meander, alternating between even and odd paths. The network therefore corresponds to a straight tandem connection of all LTP's, which can be unfolded into a regular two-port network. This important observation will be pursued in Section III.

As can be seen from Fig. 16 the proper timing of the switches in an SC cascade can be determined by the equivalent four-port network. For nonideal switches, i.e., with parasitic capacitors, the $R_\infty$'s will assume finite values. This introduces resistive bypasses and complicates the analysis. A straight cascade analysis of the LTP's is then no longer possible. Interestingly enough, as much as the parasitic capacitors helped to avoid singular matrices for the example in [1], they ultimately complicate a straight two-port analysis of SC networks. However, it still seems preferable to analyze a cascade of two-ports with resistive bypasses, than to proceed rigorously through the matrix analysis of the entire SC network. Parasitic capacitors across the switches can be taken into account, by introducing finite values for the $R_\infty$'s corresponding to the capacitor values.

Similarly the cascade of alternating shunt switches and series capacitors can be modeled.

Other topologies can be obtained by cascading storage capacitors with SC's, as shown in Figs. 17(a) and 18(a). In Fig. 17(a) shunt capacitors are cascaded with switched series capacitors. The corresponding four-port equivalent circuit is shown in Fig. 17(b). Due to the ideal series switches $S^e$($R_\infty$'s in the odd path), the current flowing in the odd path is zero and the ports of all LTP's connected to the odd path are decoupled. This leaves only the even path as the signal path. The input impedances of the open-circuited LTP's are shunted across the even path, alternating with the series resistors related to the switched series capacitors. A similar mechanism applies to the circuit shown in Fig. 18. It can be considered as the dual circuit to the one shown in Fig. 17.

As we shall see in the next section, by unfolding the signal meanders resulting from the four-port representation, most SC circuits of the kind shown in Figs. 16–18 can be reduced to a two-port equivalent circuit that can be further analyzed as such. Naturally other combinations

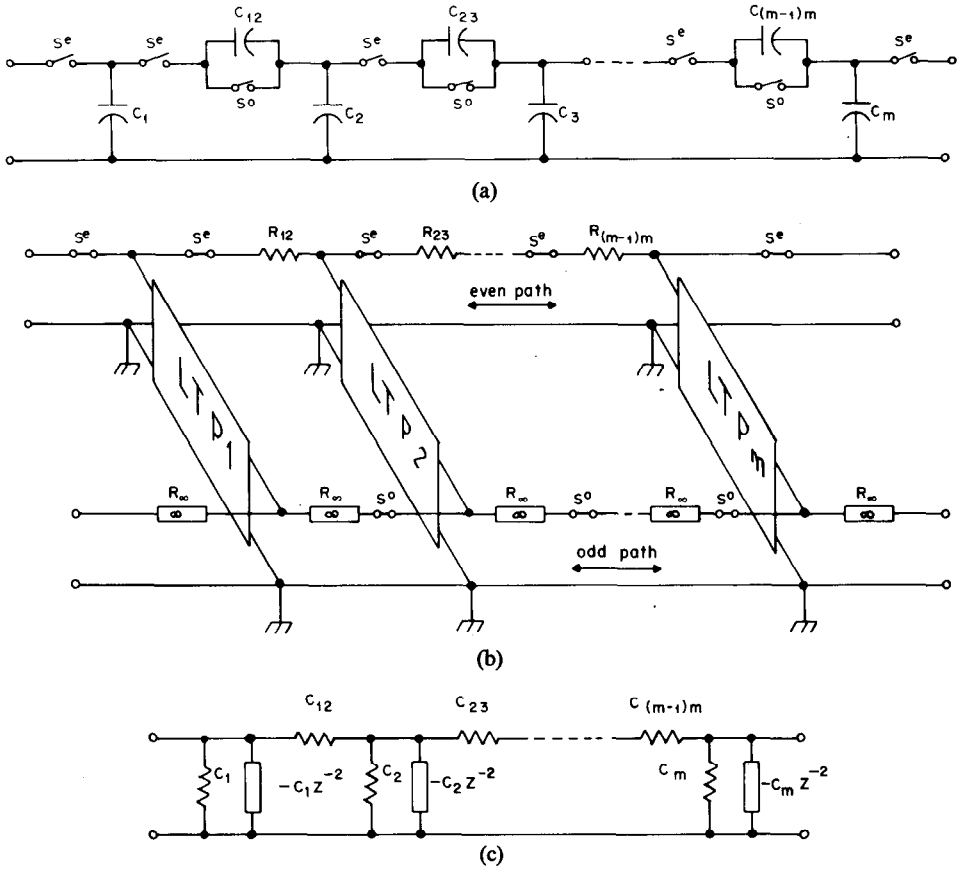



Fig. 17. (a) Cascade of shunt capacitors and switched series capacitors. (b) Four-port equivalent circuit. (c) Final ladder equivalent circuit.

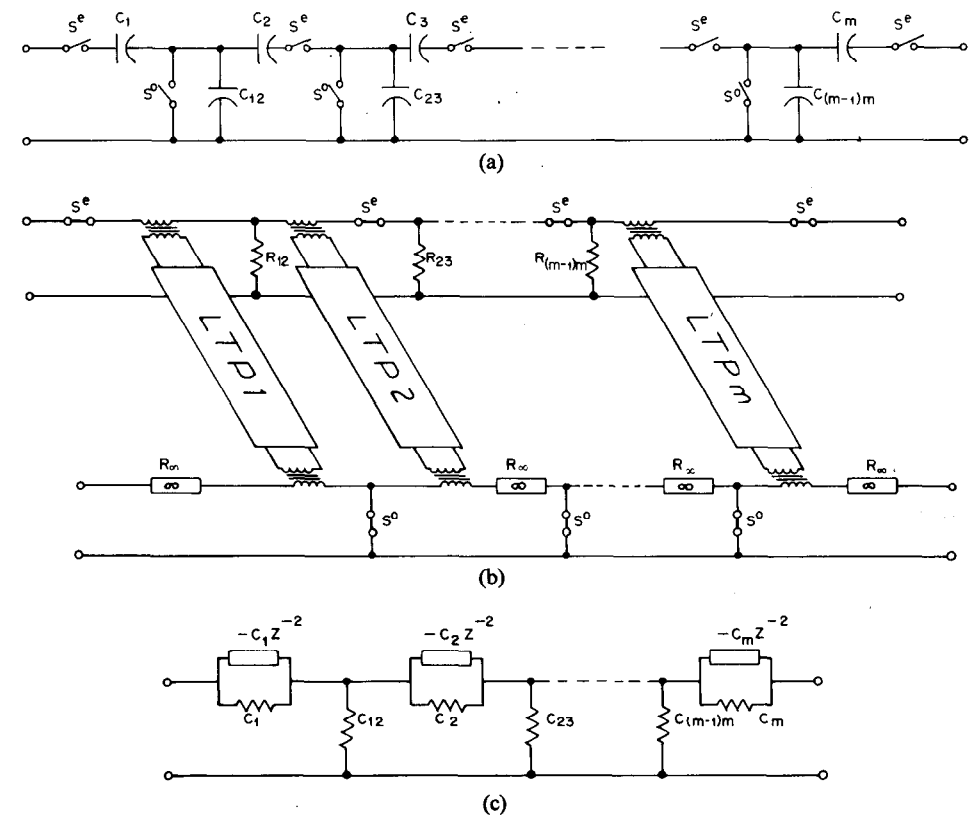



Fig. 18. (a) Cascade of series capacitors and switched shunt capacitors. (b) Four-port equivalent circuit. (c) Final ladder equivalent circuit.

of tandem connections of SC building blocks can be found which will lead to a two-port cascade (e.g., combinations of the circuits in Figs. 16–18). However, the examples given here should suffice to demonstrate the principle of representing SC building blocks by four-port equivalent circuits. In the following, the ensuing step of reducing the four-port to a two-port cascade will be discussed.

## III. Two-Port Analysis of SC Networks

### A. Cascade Analysis of Building Blocks

As we have seen, the SC network shown in Fig. 16(a) can be reduced to an equivalent two-port which resembles the tandem connection of LTP's as shown in Fig. 19(a). The two-port equivalent circuits for the SC networks in Figs. 17(a) and 18(a) can be reduced to the ones shown in Fig. 19(b) and (c), respectively. By, expressing the open circuit input impedance of the LTP's in terms of their elements, the analysis of the two-ports in Fig. 19(b) and (c) reduces to that of a simple ladder structure. Using the gyrator representation for the LTP as in Fig. 10, its open circuit input impedance can be derived (see Fig. 20) [6], [7].

By inspection we obtain

$$Z_{\text{in}} = \frac{V_1}{I_1} = \frac{G^e}{G^{e2} - G^{o2}} = C^{-1} \frac{1}{1 - z^{-2}}. \tag{18}$$

The final two-port equivalent circuits for the SC ladder networks shown in Figs. 17(a) and 18(a) are shown in Figs. 17(c) and 18(c), respectively.

In order to continue the cascade analysis of LTP's as shown in Fig. 19(a) it is necessary to derive the transmission matrix for one LTP. This can be obtained by inverting the $y$-matrix in (6) to an $ABCD$ matrix. We obtain

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} -\frac{G^e}{G^o} & -\frac{1}{G^o} \\ G^o - \frac{G^{e^2}}{G^o} & -\frac{G^e}{G^o} \end{bmatrix} \cdot \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{19}$$

and with (3a) and (3b)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{LTP}} = \begin{bmatrix} z & z/C \\ zC(1-z^{-2}) & z \end{bmatrix}. \tag{20}$$

The transmission matrix of an entire chain of $m$ LTP's is now obtained by multiplying the transmission matrices of the $m$ individual LTP's, thus

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_m = \prod_{\nu=1}^{m} \begin{bmatrix} z & z/C_\nu \\ zC_\nu(1-z^{-2}) & z \end{bmatrix}. \tag{21}$$

For $m=2$ (21) yields

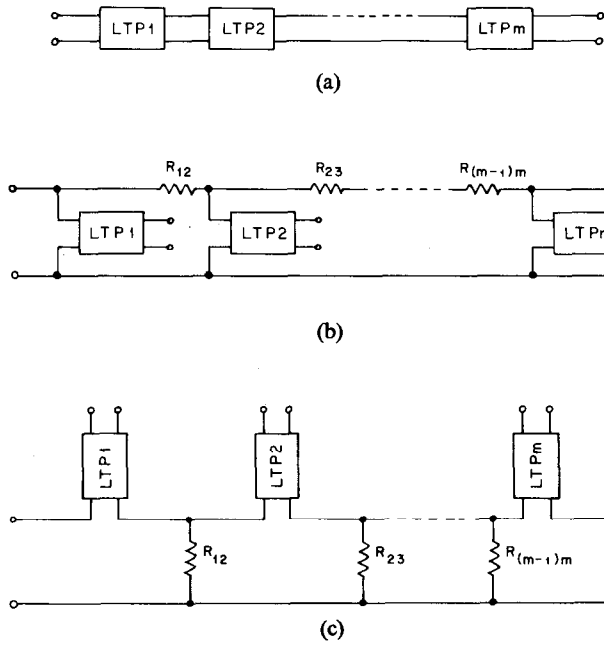



Fig. 19. Two-port equivalent circuits of SC ladder networks (a) corresponding to Figs. 18 and 19, (b) corresponding to Fig. 20, (c) corresponding to Fig. 21.

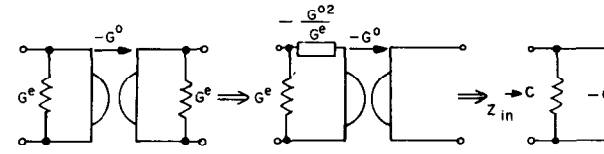



Fig. 20. Open circuit input impedance of LTP derived via gyrator equivalent circuit.

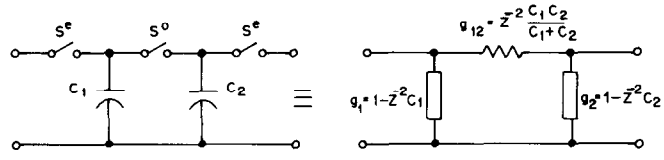



Fig. 21. Π-equivalent circuit cascade of two LTP's.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_2 = \begin{bmatrix} z^2\left[1 + \frac{C_2}{C_1}(1-z^{-2})\right] & z^2\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \\ z^2C_1 + C_2(1-z^{-2}) & z^2\left[1 + \frac{C_1}{C_2}(1-z^{-2})\right] \end{bmatrix}. \tag{22}$$

This matrix represents the $\pi$-configuration shown in Fig. 21. This circuit can be modeled very easily by an $RC$ circuit, as will be shown later in Section IV.

### B. General Two-Port Transfer Functions

The previously described two-port analysis was restricted to cases where building blocks are cascaded by

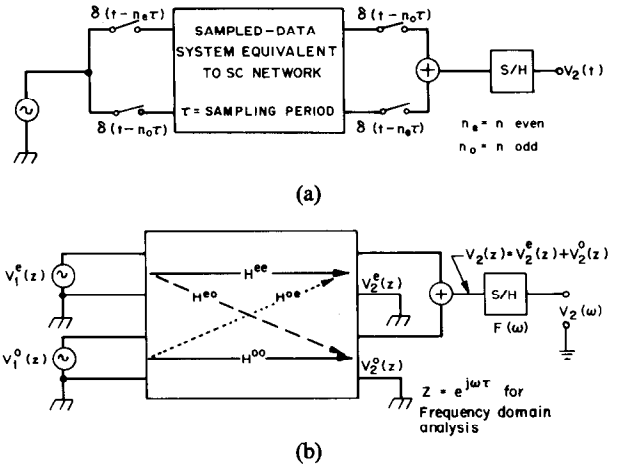



Fig. 22. SC network equivalent system. (a) Time domain. (b) Frequency domain.

tracing the signal flow through the four-port equivalent circuit. This is possible only if the signal is transmitted along either the odd or even path, or if it alternates from one path to the other. When the signal is transmitted through the even *and* odd path and when LTP's are present, a more general approach must be used.

For the general case the entire SC network may be considered as a two-port with an input signal and an output signal in the time domain. A convenient equivalent circuit is shown in Fig. 22(a). In it the entire SC network is represented by a linear, time discrete, or sampled-data system, in cascade with a sample-and-hold circuit. The latter restores the finite pulsewidth for each discrete value coming out of the sampled-data system [8]. The even and odd times are separated in order to provide a direct relationship to the four-port equivalent circuit in the frequency domain as shown in Fig. 22(b). In the general case four transfer functions $H^{ee}$, $H^{oo}$, $H^{eo}$, and $H^{oe}$ must be distinguished. In the simple cases described in the previous section, two or three of these were zero. From Fig. 22(b), the output voltage $V_2(z)$ can be expressed in terms of the even and odd part of the sampled input function $V_1(z)$ as

$$\begin{aligned} V_2(z) &= V_2^e(z) + V_2^o(z) \\ &= V_1^e(z)\left[H^{ee}(z) + H^{eo}(z)\right] \\ &\quad + V_1^o(z)\left[H^{oo}(z) + H^{oe}(z)\right]. \end{aligned} \tag{23}$$

For a uniformly sampled sinusoidal input signal $V_1 e^{j\omega_0 n\tau}$, the $z$-transformed function is given by [8]

$$Z\left\{V_1 e^{j\omega_0 n\tau}\right\} = V_1(z) = \frac{V_1 z}{z - e^{j\omega_0\tau}}. \tag{24}$$

From [1, table 2], the even and odd part can be determined as follows:

$$\begin{aligned} V_1^e(z) &= \frac{1}{2}\left[V_1(z) + V_1(-z)\right] \\ &= \frac{V_1}{2}\left[\frac{z}{z - e^{j\omega_0\tau}} + \frac{-z}{-z - e^{j\omega_0\tau}}\right] \\ &= V_1 \frac{z^2}{z^2 - e^{2j\omega_0\tau}} \end{aligned} \tag{25a}$$

$$\begin{aligned} V_1^o(z) &= \frac{1}{2}\left[V_1(z) - V_1(-z)\right] \\ &= \frac{V_1}{2}\left[\frac{z}{z - e^{j\omega_0\tau}} - \frac{-z}{-z - e^{j\omega_0\tau}}\right] \\ &= V_1 \frac{z e^{j\omega_0\tau}}{z^2 - e^{2j\omega_0\tau}}. \end{aligned} \tag{25b}$$

Substituting $V_1^e$ and $V_1^o$ into (23) yields

$$\begin{aligned} V_2(z) = V_1 &\frac{z^2}{z^2 - e^{j2\omega_0\tau}} \\ &\cdot\left\{H^{ee}(z) + H^{eo}(z) + e^{j\omega_0\tau} z^{-1}\left[H^{oo}(z) + H^{oe}(z)\right]\right\}. \end{aligned} \tag{26}$$

After dividing (26) by (24) we obtain the overall transfer function of the sampled-data system in the $z$-domain

$$\frac{V_2(z)}{V_1(z)} = \frac{H^{ee}(z) + H^{eo}(z) + e^{j\omega_0\tau} z^{-1}\left[H^{oo}(z) + H^{oe}(z)\right]}{1 + e^{j\omega_0\tau} z^{-1}}. \tag{27}$$

This can be evaluated at the frequency $\omega = \omega_0$, $(z = e^{j\omega\tau})$ which is the frequency of the sinusoidal input signal, or at any frequency $\omega = \omega_0 \pm n\pi/\tau$ of the spectrum generated by the sampling process. After further multiplying this frequency response with the response of the sample-and-hold device

$$F(\omega) = \frac{\sin \omega\tau/2}{\omega\tau} e^{+j\omega\pi/2} \tag{28}$$

the overall transfer function can be established.

$$\begin{aligned} H(\omega)_{\text{Tot}} &= \frac{H^{ee}(e^{j\omega\tau}) + H^{eo}(e^{j\omega\tau}) + \left[H^{oo}(e^{j\omega\tau}) + H^{oe}(e^{j\omega\tau})\right] e^{j(\omega_0 - \omega)\tau}}{1 + e^{j(\omega_0 - \omega)\tau}} \\ &\quad \cdot \frac{\sin \omega\tau/2}{\omega\tau} e^{+j\omega\tau/2}. \end{aligned} \tag{29}$$

The individual four transfer functions $H^{ik}$ have to be calculated from the four-port equivalent circuit of the entire SC network. With the general equivalent circuit of an SC network according to Fig. 22(a) and (b), the analysis can be extended to arbitrary duty cycles, i.e., $\tau_1$ and $\tau_2$ being different closing times for the switches. In reference to the 50-percent duty cycle, we have $2\tau = \tau_1 + \tau_2$. Consider now that the input signal $V_1 e^{j\omega_0 t}$ is phase shifted for odd sampling times by the time $(\tau_1 - \tau_2)/2$, as indicated in

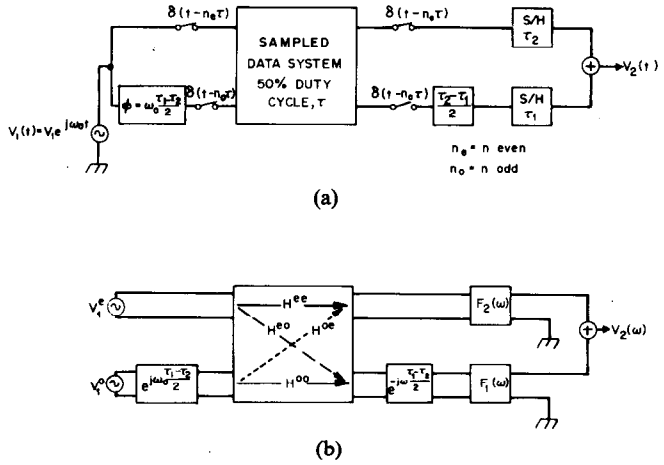



Fig. 23. (a) Equivalent system for SC network with arbitrary duty cycle. (b) Equivalent circuit in the frequency domain.

Fig. 23(a) and (b). In this way, even and odd times again correspond to a system with 50-percent duty cycle. The shift $(\tau_1-\tau_2)/2$ of the input signal guarantees that, at the odd time of the 50-percent duty cycle, the right value of the input signal (which was supposed to be sampled at $\tau_1$) is processed. At the output of the sampled-data system the odd samples must be delayed by $(\tau_1-\tau_2)/2$ in order to bring the even and odd times back to a duty cycle that is no longer 50 percent. Since $\tau_1$ and $\tau_2$ are different, the restoration to a finite pulse length of $\tau_1$ and $\tau_2$ has to be carried out by two different sample and hold systems:

$$F_1(\omega)=\frac{\sin \omega\tau_1/2}{\omega\tau}\,e^{+j\omega\tau_1/2} \tag{30}$$

$$F_2(\omega)=\frac{\sin \omega\tau_2/2}{\omega\tau}\,e^{+j\omega\tau_2/2}. \tag{31}$$

This is indicated in Fig. 23.

By going through a derivation similar to the one in (23)–(29), and taking the phase-shifting and different sample-and-hold devices into account, we obtain the overall transfer function for arbitrary duty cycles as follows:

$$\begin{aligned} H(\omega)_{\text{Tot}} &= \frac{H^{ee}(e^{j\omega\tau})+H^{oe}(e^{j\omega\tau})\cdot e^{j\omega_0\tau_1}\cdot e^{-j\omega(\tau_1+\tau_2)/2}}{1+e^{j\omega_0\tau_1}e^{-j\omega(\tau_1+\tau_2)/2}} \\ &\quad\cdot\frac{\sin \omega\tau_2/2}{\omega\tau}\,e^{+j\omega\tau_2/2} \\ &\quad+\frac{H^{eo}(e^{j\omega\tau})\cdot e^{-j\omega(\tau_1-\tau_2)/2}+H^{oo}(e^{j\omega\tau})\cdot e^{j(\omega_0-\omega)\tau_1}}{1+e^{j\omega_0\tau_1}e^{-j\omega(\tau_1+\tau_2)/2}} \\ &\quad\cdot\frac{\sin \omega\tau_1/2}{\omega\tau}\,e^{j\omega\tau_1/2} \qquad (32) \\ &\quad \omega=\omega_0\pm n\Omega_0, \qquad n=0,1,2,3\cdots \\ &\quad \Omega_0=\pi/\tau. \end{aligned}$$

Both transfer functions (29) and (32) are valid only if the SC network is fed by a staircase function, where at the end of the closing time of the switches information transfer occurs. A more systematic derivation of this general result in equation (32), with an extension to continuous input signals, will be published by one of the authors in the near future.[1]

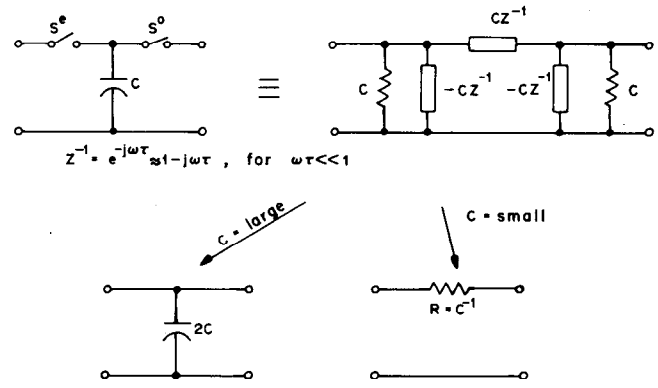



Fig. 24. *RC* analogies for shunt capacitor between toggle switch.

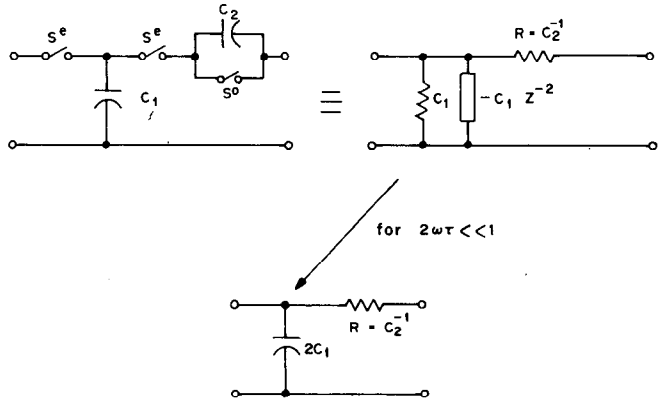



Fig. 25. *RC* low-pass approximation for shunt capacitor and switched series capacitor.

## IV. *RC* Analogies of SC Networks

An SC network frequently used and described in the literature is a shunt capacitor with a toggle switch [9], [10]. It is the basic two-port associated with one LTP, as can be seen from Fig. 16. Its *RC* analogy can be demonstrated by substituting the relations (3a) and (3b) into the elements of the circuit in Fig. 9. As demonstrated in Fig. 24 the circuit can be interpreted as a capacitor for $C$=large and as a resistor for $C$=small. In both cases it is required that $\omega\tau\ll 1$, which allows the approximation $z^{-1}=e^{-j\omega\tau}\approx 1-j\omega\tau$ to be made. However, under the above mentioned conditions the circuit is a rather coarse approximation for a series resistor.

A far more accurate low-pass filter approximation can be obtained by using the SC network structure shown in Fig. 17(a) with its equivalent ladder circuit shown in Fig. 17(c). This is demonstrated in Fig. 25 for one section.

[1]The result expressed in (32), in a different mathematical representation, was independently obtained by Y. L. Kuo and M. L. Liou, by using a different approach for the analysis. Their work, which includes continuous input signals, is scheduled for publication in the April issue of this TRANSACTIONS. Their cooperation in comparing the results and the subsequent discussions are very much appreciated.

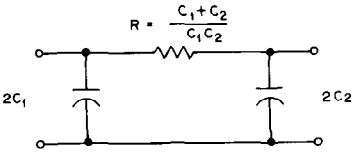



Fig. 26. *RC* analogy for circuit shown in Fig. 21.

Letting

$$z^{-2}=e^{-j\omega\tau 2}\approx 1-j2\omega\tau, \qquad 2\omega\tau\ll 1 \tag{33}$$

the conductive part in the shunt branch can be eliminated and a capacitive component, related to the imaginary part in (33) remains. The only condition for the approximation is $2\omega\tau\ll 1$, regardless of the size of the element values.

Finally, in Fig. 26, an *RC* analogy for the circuit shown in Fig. 21 is presented. It is again based solely on the approximation made in (33), and is independent of the capacitor values. In conclusion, it can be said that passive SC networks with two-phase switches have properties similar to those of passive *RC* circuits. They are not capable of generating complex conjugate pole pairs without including active devices.

## V. Example of Second-Order SC Network with Operational Amplifier

The following example, shown in Fig. 27(a), was chosen to demonstrate how the described analysis method of cascaded SC networks can be used for the analysis of a second-order SC network with one active element. The choice is not based on any performance merits or technological advantages of this particular circuit. A systematic evaluation of various circuits with active elements is presently being undertaken. Thus the purpose of this example is to illustrate how to synthesize filter networks using the four-port equivalent circuits of the building blocks introduced in the previous sections.

The first step in the analysis of the circuit shown in Fig. 27(a) is to convert it into a four-port equivalent circuit. This is shown in Fig. 27(b). The signal flows through the cascade of LTP's in the form of a meander. In terms of currents and the link two-ports the signal flow can be described symbolically as follows:

$$\begin{aligned} V_6^e \rightarrow I_F^e + \; & I_s^e \\ & \uparrow \\ & V_s^e \end{aligned}$$

$$= I_1^e \rightarrow \mathrm{LTP}_1 \rightarrow I_2^o \rightarrow \mathrm{LTP}_2 \rightarrow I_3^e \rightarrow \mathrm{LTP}_3 \rightarrow I_4^o \rightarrow \mathrm{LTP}_4 \rightarrow I_5^e \rightarrow V_6^e.$$

The desired transfer function is

$$T(z)=\frac{V_6^e(z)}{V_s^e(z)}. \tag{34}$$

For a simple derivation of (34) the four-port equivalent circuit can be reduced to a two-port equivalent circuit with feedback as shown in Fig. 27(c). The internal two-port *ABCD* thereby consists of the cascade of the four LTP's in Fig. 27(b). The operational amplifier has been redrawn as a current controlled voltage source, where $g=1/C_g$, thus

$$V_6^e=-I_5^e\frac{1}{C_g}=-I_5^e\frac{1}{g}.$$

The transmission matrix *ABCD* can be obtained from (21) for $m=4$, or from (22) for $m=2$. It is more convenient to calculate the product of two matrices, therefore, with (22) and letting $p=1-z^{-2}$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{m=4} = z^4 \begin{bmatrix} \left(1+\frac{C_2}{C_1}p\right)\left(1+\frac{C_4}{C_3}p\right)+\left(\frac{1}{C_2}+\frac{1}{C_1}\right)(C_3+C_4)p & \left[\left(1-\frac{C_2}{C_1}p\right)\left(\frac{1}{C_3}+\frac{1}{C_4}\right)+\left(1+\frac{C_3}{C_4}p\right)\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right] \\ (C_1+C_2)\left(1+\frac{C_4}{C_3}p\right)+(C_3+C_4)\left(1+\frac{C_1}{C_2}p\right) & \left(1+\frac{C_1}{C_2}p\right)\left(1+\frac{C_3}{C_4}p\right)+\left(\frac{1}{C_3}+\frac{1}{C_4}\right)(C_1+C_2)p \end{bmatrix}. \tag{35}$$

Before considering the feedback loop, the following matrix relation can be derived from the circuit in Fig. 27(c):

$$\begin{bmatrix} V_1^e \\ I_1^e \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{m=4} \cdot \begin{bmatrix} 0 & 0 \\ -C_g & 0 \end{bmatrix} \cdot \begin{bmatrix} V_6^e \\ I_6^e \end{bmatrix} = \begin{bmatrix} -BC_g & 0 \\ -DC_g & 0 \end{bmatrix} \cdot \begin{bmatrix} V_6^e \\ I_6^e \end{bmatrix}. \tag{36}$$

The second matrix factor multiplying the *ABCD* matrix represents the current controlled voltage source. Equation (36) yields the following two simple relations:

$$V_1^e=-BC_gV_6^e \tag{37}$$

$$I_1^e=-DC_gV_6^e. \tag{38}$$

With this, the overall transfer function of the network in Fig. 27(c) results in

$$\frac{V_6^e}{V_s^e}=T(z)=-\frac{C_s}{C_g}\frac{1}{B(C_F+C_s)+D+\frac{C_F}{C_g}} \tag{39}$$

and after substituting the terms for $B$ and $D$ from (35)

$$T(z)=\frac{Kz^{-4}}{p^2+pa_1+a_0+\frac{C_F}{C_g}\alpha z^{-4}} \tag{40}$$

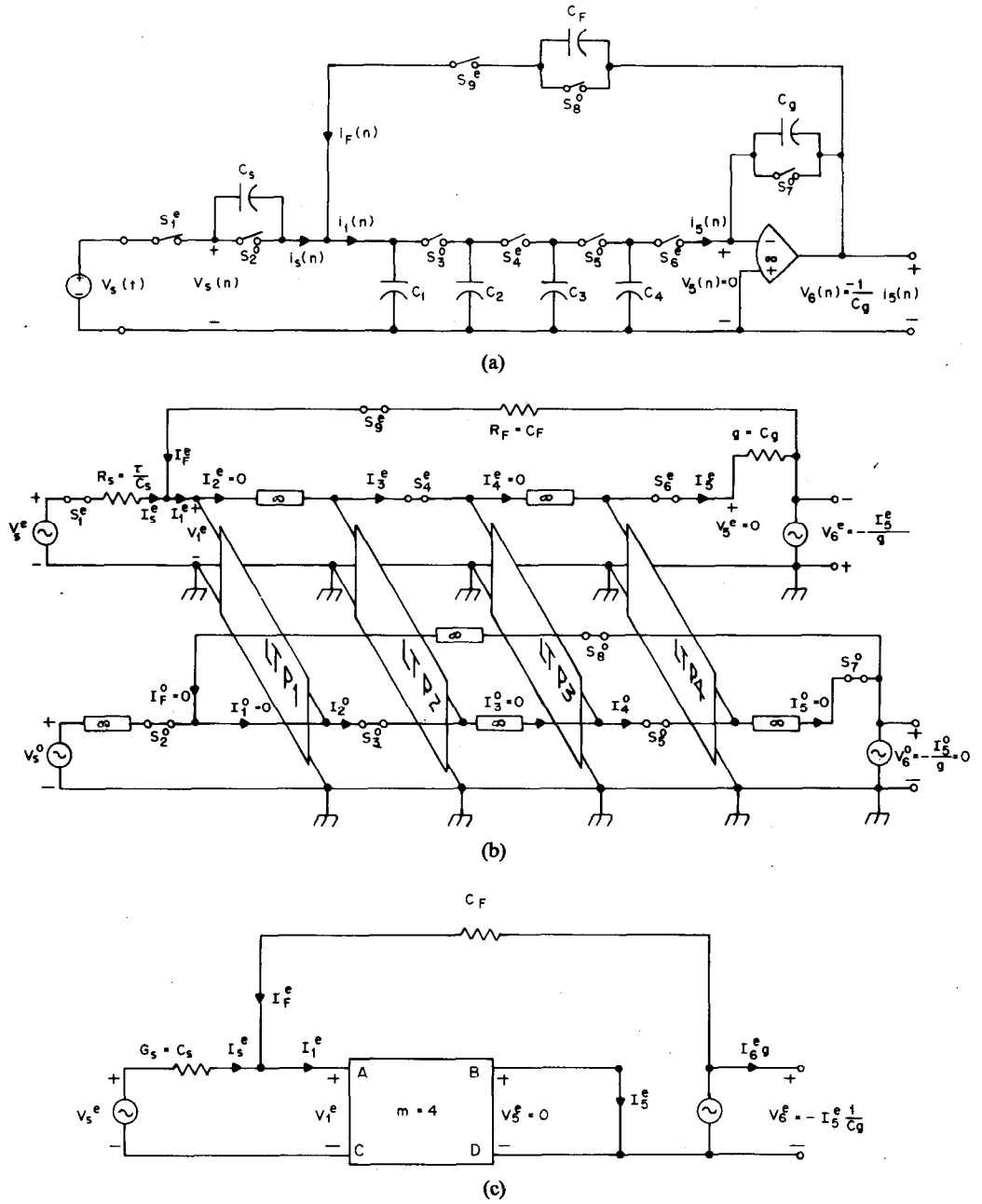



Fig. 27. (a) Second-order SC network with operational amplifier. (b) Four-port equivalent circuit. (c) Two-port equivalent circuit.

where $p = 1 - z^{-2}$ and

$$\alpha = \frac{C_2 C_4}{C_1 C_3} \qquad K = -\alpha \frac{C_s}{C_g} \tag{41}$$

$$a_1 = \alpha\left[(C_F + C_s)\left\{\frac{C_2}{C_1}\left(\frac{1}{C_3}+\frac{1}{C_4}\right)+\frac{C_3}{C_4}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right\} + \frac{C_1}{C_2}+\frac{C_3}{C_4}+\frac{C_1}{C_3}+\frac{C_1}{C_4}+\frac{C_2}{C_3}+\frac{C_2}{C_4}\right] \tag{42}$$

$$a_0 = \alpha\left[(C_F + C_s)\left(\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}+\frac{1}{C_4}\right)+1\right]. \tag{43}$$

As can be observed in (40), the transfer function $T(z)$ is actually a function of $z^{-2}$, since no terms of $z^{-1}$ occur. Hence it can be considered as the transfer function of a sampled-data filter with a sampling period $2\tau$. Consequently the transfer function in (40) can be written with a new variable $z^* = z^2 (z^* = e^{j\omega 2\tau})$ as follows:

$$T(z^*) = \frac{Kz^{*-2}}{z^{*-2}\left(1 - \frac{C_F}{C_g}\alpha\right) - z^{*-1}(2 + a_1) + 1 + a_1 + a_0}. \tag{44}$$

Equation (44) corresponds to the response of the sampled-data low-pass filter shown in Fig. 27(a). This circuit was built in the laboratory using discrete capacitors and discrete FET switches. Although all elements were nonideal (i.e., on-resistors of the switches $R_{on} \approx 500\ \Omega$), a

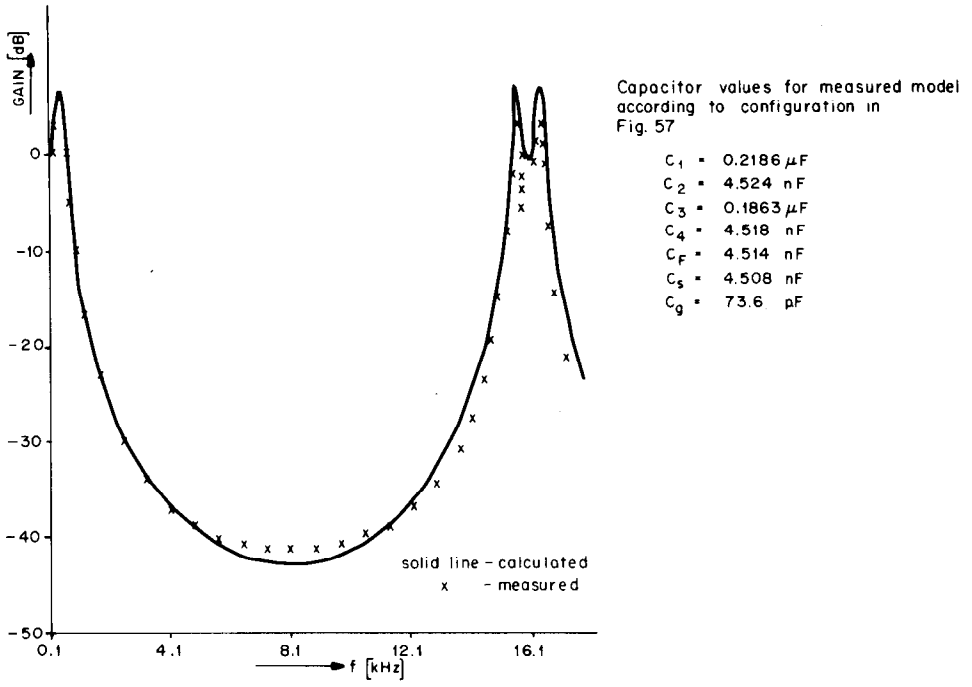



Fig. 28. Measured and calculated response of laboratory model.

relatively good match between the measured and the predicted response was achieved, as shown in Fig. 28. The overall rolloff towards higher frequencies is due to a sin $x/x$ response related to the finite pulsewidth at the output of the network.

## VI. Conclusions

It has been shown in a previous publication by the authors that general SC networks can be analyzed using nodal charge equations, which can be transformed into the $z$-domain. While the nodal charge-equation approach bears some similarity to Kirchhoff's current laws, an SC network can ultimately be considered as a sampled-data system described by a set of difference equations with periodically time-varying coefficients. Carried out routinely, this general analysis rapidly leads to unwieldy analytical expressions, if the SC network has the complexity generally encountered in practice. In order to avoid the resulting loss of insight and analytical complexity, a building block analysis is introduced in this paper, based on six passive two-ports which are most commonly used in SC networks. These basic two-ports are interpreted as four-port equivalent circuits in the $z$-domain. They allow the separation of odd and even time slots (or off and on times of the switches) by introducing separate signal paths for the two time slots. It is shown that the even and odd signal path is linked by an LTP whenever a storage element, such as a shunt or series capacitor, occurs. A two-port equivalent circuit is derived for this LTP by introducing a one-port storage element, the storistor, which delays the current versus the voltage across it by one delay unit $z^{-1}$. The analytical treatment of active devices in conjunction with SC networks is also presented. Finally it is shown how a cascade of SC building blocks can be analyzed using the four-port equivalent circuits. This approach ultimately leads to a two-port analysis with the LTP as the basic element. Some analogies between SC and *RC* networks are shown. SC networks with two-phase switches have *RC* network properties in that they cannot generate complex conjugate pole pairs. An example is presented to show how a complex conjugate pole pair for a second-order system can be generated by incorporating an operational amplifier in SC networks. Some measured results are presented; they agree well with the theoretical prediction.

The analysis method presented here, in particular the building block approach, represents a systematic method of analyzing general SC networks. Using this analysis the performance of various practical circuits can be evaluated, and a design classification may be derived in a manner similar to that carried out for active networks [11]. Such a classification and the analysis of SC networks with parasitics should provide fruitful ground for further work in this area.

## Acknowledgment

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**Carl F. Kurth** (SM'64–F'79), for a photograph and biography please see page 104 of the February issue of this TRANSACTIONS.

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**George S. Moschytz** (M'65–SM'77–F'78), for a photograph and biography please see page 104 of the February issue of this TRANSACTIONS.

# On the Determination of the Smith–Macmillan Form of a Rational Matrix From Its Laurent Expansion

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***Abstract*—A novel method is presented to determine the Smith–Macmillan form of a rational $m \times n$ matrix $R(p)$ from Laurent expansions in its poles and zeros. Based on that method, a numerically stable algorithm is deduced, which uses only a minimal number of terms of the Laurent expansion, hence providing a shortcut with respect to cumbersome and unstable procedures based on elementary transformations with unimodular matrices.**

**The method can be viewed as a generalization of Kublanovkaya's algorithm for the complete solution of the eigenstructure problem for $\lambda I - A$. From a system's point of view it provides a handy and numerically stable way to determine the degree of a zero of a transfer function and unifies a number of results from multivariable realization and invertibility theory. The paper presents a systematic treatment of the relation between the eigen-information of a transfer function and the information contained in partial fraction or Laurent expansions. Although a number of results are known, they are presented in a systematic way which considerably simplifies the total picture and introduces in a natural way a number of novel techniques.**

## I. INTRODUCTION

THE PROBLEM of efficient determination of the Smith–Macmillan form of a rational $m \times n$ matrix $R(p)$ does not seem to have received a great deal of attention in the past, although its importance as a key element in systems analysis and design can hardly be denied. The classical method of using unimodular matrix manipulations is cumbersome and not suited for numerical computations, because it results in an extraordinarily large number of polynomial manipulations. In all methods based hereon, numerical stability is lost because pivoting is not based on the coefficients of $p$ but on its power [1].

On the other hand, a number of papers are devoted to the realization problem for system transfer functions and a host of algorithms have been devised [2]–[7]. Another set of algorithms were proposed for system inversion both in the case of systems over a finite field [8]–[10] and in the case of systems over $\mathbb{C}$ or $\mathbb{R}$ [11], and criteria for system invertibility where derived [12], [13]. Most of these methods require the handling of large size matrices and none devote any attention to the numerical stability problem.

An answer to the invertibility problem is needed, e.g., in coding theory where one is interested in deciding whether the transfer function has a unique zero at infinity (of large degree) and if so, in determining the degree of that zero and the inverse of the matrix. Also, in invertibility theory one wishes to know whether there is actually a zero at infinity in which case the system cannot be inverted. In

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