Two Variations of Five-Level Hybrid-Clamped Converters and Their Voltage Balancing Control Using Three Degrees of Freedom

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***Abstract*—This paper comprehensively utilizes three control freedoms, i.e., switching state selection, zero sequence injection(ZSI) and redundant level modulation(RLM), to maintain capacitor voltage balance in two five-level three-phase converters over the full range of modulation index and power factor. The calculation process of the proposed control method is explained in detail. This method is easy to implement and can be used in other multilevel converters. The first topology is proposed for the first time in this paper. The capacitor voltage controllable region of the second topology has been extended to full operation range without extra circuits. Voltage jumps are found during the deadtime. The performance of the proposed topology and control method is verified by simulation and experiment.**

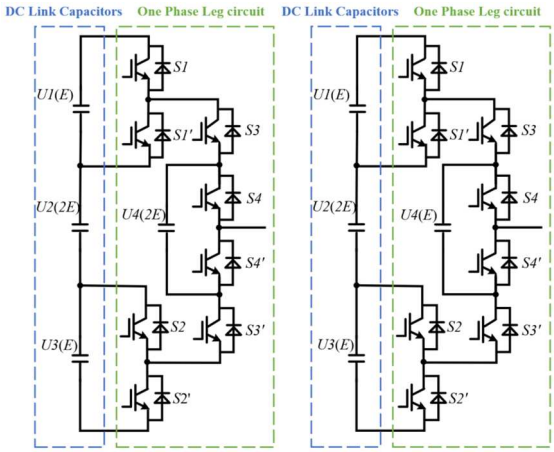
Keywords—multilevel converters, capacitor voltage balance, five-level converters, zero sequence injection, redundant level modulation, switching state selection

I. INTRODUCTION

Multilevel converters have many advantages, such as lower total harmonic distortion (THD), lower output voltage step (dv/dt), lower device blocking voltage stress and lower switching loss over two-level converters. They have been widely used in medium-voltage, high-power applications such as motor drives, renewable generation and HVDC transmission systems and they have also been extended to low-voltage applications [1]. Multilevel converters with more than three levels have better performance than three-level converters in terms of lower output harmonics and the total dc-link voltage that can be achieved, but higher levels need more devices, adding to the cost and control complexity. To obtain new topologies with reduced number of devices, better structures and general control methods with high control ability are two important research aspects of multilevel converters.

Typical types of multilevel converters include the neutral point clamped (NPC) converter, the flying capacitor (FC) converter and the cascaded H-bridge (CHB) converter. Some other topologies have also been investigated, such as the active NPC (ANPC) converter, Vienna-type converters and modular multilevel converters (MMC). To simplify and find the inherent law of multilevel converter topology derivation, generalized topologies are proposed and new topologies can be derived from them. [2] concludes four main generalized voltage source topologies and derivation methods. [3] further proposes an ultimate generalized multilevel converter topology with bidirectional switches for converters with a symmetrical structure. Many recently proposed topologies [4]-[12] can be derived from it.

Advanced control methods can achieve capacitor voltage balance, output harmonic reduction, high DC voltage utilization, heat balance of power devices and so on. This paper focuses on the precise capacitor voltage control. Some converters, especially with reduced devices, cannot realize capacitor voltage balance over the full range of modulation index and power factor, which limits their application areas. To address this issue, researchers utilize additional hardware balancing circuits [13]-[15] or back-to-back topology to balance capacitor voltages [16], [17]. However, additional hardware not only increases the cost, but also hinders the power density. Thus, software methods receive more attention and many novel methods have been proposed. Model predictive control (MPC) [18], [19] can handle multiple-objective optimization problems and respond dynamically. The issues of traditional MPC, such as unfixed switching frequency and heavy computation burden were improved in [18] and [19] respectively. However, it is still time-consuming to obtain effective cost functions and modify weighting factors. Carrier-overlapped PWM (COPWM) [20], [21] is another new approach with the benefits such as natural balancing ability and easy implementation. But the harmonic distortion and difficulty in modifying the carrier waveforms limit its application. Unlike COPWM, redundant level modulation (RLM) [22]-[24] modifies the modulation waveforms to realize voltage balance. RLM utilizes two or more voltage level changes in one switching cycle. It can operate regardless of modulation index and power factor. This method is generally applicable and easy to use. The main disadvantage is the increase of switching loss and some high order harmonics.



(a) (b)

Fig.1 Two five-level three-phase converter structures. (a)Topology A. (b)Topology B.

This paper proposes the combinational use of all three control types based on carrier-based PWM in two three-phase five-level flying capacitor inverters with the aim of achieving capacitor voltage balance over the full operation range. Topology A is proposed in this paper and shown in Fig.1(a)

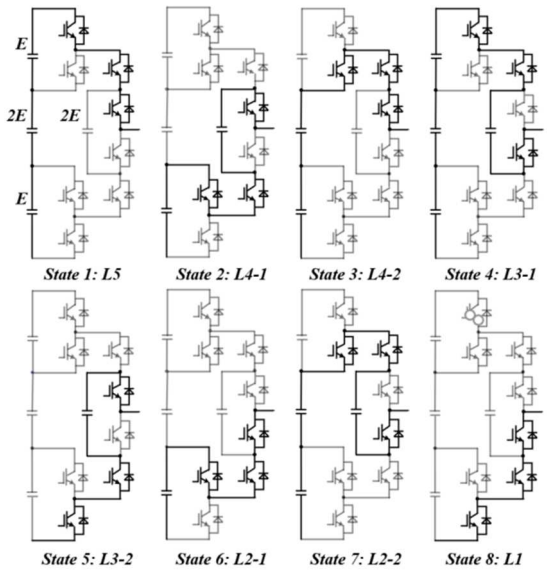


Fig.2. Current paths of all switching states in Topology A.

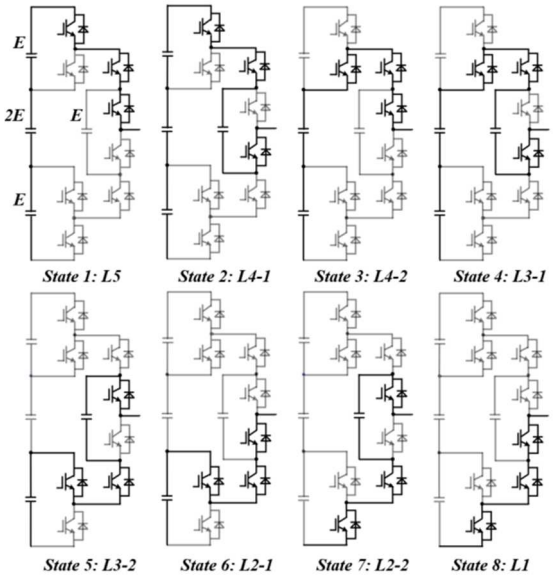


Fig.3. Current paths of all switching states in Topology B.

and topology B is shown in Fig.1(b). Topology B was proposed in [4]. The difference between these two topologies is that the flying capacitor voltages are E and *2E* for topologies A and B, respectively, where *E* is 1/4 of the dc-link voltage (V_{dc}). [4] combines the switching state selection and ZSI and gives the controllable region for topology B. However, the modulation index cannot exceed 0.7 when unit power factor operation is assumed. Therefore, RLM is used additionally in this paper to realize the capacitor voltage balance control in the whole range of modulation index and power factor. [13] uses an auxiliary balancing circuit to control the dc-link capacitor voltages for Topology B, with the expenses of additional hardware cost and volume. [25] further proposes a phase-shifted PWM with ZSI and adjusts the duty ratio of each switching device. This method succeeds in selecting the best switching states among all switching states, however, it does not guarantee that the phase voltage changes only between two adjacent voltage levels because the switching states are selected without considering voltage jump levels. Few *4E*, some *3E* and *2E* voltage jumps exist, which cause high dv/dt at the converter output. Also, three PI controllers employed in [25] increase the tuning time. Furthermore, this method sacrifices the harmonic distortion performance and may be difficult to implement. To solve the above mentioned issues, this paper fully uses the three control freedoms of redundant switching state selection, zero-sequence voltage injection and redundant level modulation, which can control the capacitor voltages. The proposed method has successfully realized the precise voltage control within the range of modulation index between 0-1 and power factor between 0-1. Simulation and experiments have been performed to confirm the effectiveness of the proposed control and topology.

II. CONTROL METHODS OF THE PROPOSED CONVERTERS

A. Current paths of all switching states

The current through capacitors decides the charging or discharging states and needs to be analysed in order to achieve the capacitor voltage balance. Fig.2 and Fig.3 show the current paths of topology A and B respectively following the order of voltage level. The output voltage level 5, 4, 3, 2 and 1 refer to *4E*, *3E*, *2E*, *E* and *0* accordingly. Switching states are divided by voltage level. If one voltage level has two switching states, these two states are noted as '-1' and '-2'. All possible switching states are listed: *L5*, *L4-1*, *L4-2*, *L3-1*, *L3-2*, *L2-1*, *L2-2* and *L1*. Although these two topologies have the same number of switching states, current paths in *L4*, *L3* and *L2* are different because of the flying capacitor voltage. Thus different control methods should be adopted.

Table I and Table II illustrate how capacitor voltages change under different switching states. The upside of capacitors is assigned to be positive. $i>0$ means the output current flows outside, $i<0$ means the output current flows inside, '↑' means the capacitor is charged, '↓' means the capacitor is discharge-ed, '-' means the capacitor voltage remains constant. Voltage of capacitor U_1 and U_3 cannot be balanced instantaneously for one-phase converter. When the current is positive, capacitor U_1 remains the same or charged. U_1 voltage will raise. When the current is negative, capacitor U_1 symmetrically remains the same or discharged. U_1 voltage will fall. So the three-phase system is needed.

B. Control method structure

The control method of topology B is similar to topology A and this paper only analyses the control of topology A. The control objects are U_1-U_4. Switching state selection, ZSI and RLM are three control freedoms and should be used in a proper order.

Firstly, the switching states should be selected and each voltage level can only utilize one switching state in a switching cycle. The switching state of level 3 is decided by U_4 voltage. If U_4 needs to be charged, *L3-1* is chosen when $i>0$ and *L3-2* is chosen when $i<0$. If U_4 needs to be discharged, *L3-2* is chosen when $i>0$ and *L3-1* is chosen when $i<0$. The selection of level 2 and 4 should consider U_2 more than other capacitors because these two levels produce the same influence on U_1 and U_3 and level 3 has been used to control U_4. The selection of them is similar to that of level 3. If U_2 needs to be charged, *L4-1* and *L2-1* are chosen when $i>0$ and *L4-2* and *L2-2* are chosen when $i<0$. If U_2 needs to be discharged, *L4-2* and *L2-2* are chosen when $i>0$ and *L4-1* and *L2-1* are chosen when $i<0$.

TABLE I. CAPACITOR CHARGING/DISCHARGING SITUATION UNDER ALL SWITCHING STATES FOR TOPOLOGY A

Level	U_o	State	S_1	S_2	S_3	S_4	U_1		U_2		U_3		U_4	
							i>0	i<0	i>0	i<0	i>0	i<0	i>0	i<0
5	4E	L5	1	1	1	1	-	-	-	-	-	-	-	-
4	3E	L4-1	1	1	0	1	↑	↓	↑	↓	↓	↑	↓	↑
		L4-2	0	1	1	1	↑	↓	↓	↑	↓	↑	-	-
3	2E	L3-1	1	1	1	0	-	-	-	-	-	-	↑	↓
		L3-2	0	0	0	1	-	-	-	-	-	-	↓	↑
2	E	L2-1	0	1	0	0	↑	↓	↑	↓	↓	↑	-	-
		L2-2	0	0	1	0	↑	↓	↓	↑	↓	↑	↑	↓
1	0	L1	0	0	0	0	-	-	-	-	-	-	-	-

TABLE II. CAPACITOR CHARGING/DISCHARGING SITUATION UNDER ALL SWITCHING STATES FOR TOPOLOGY B

Level	U_o	State	S_1	S_2	S_3	S_4	U_1		U_2		U_3		U_4	
							i>0	i<0	i>0	i<0	i>0	i<0	i>0	i<0
5	4E	L5	1	1	1	1	-	-	-	-	-	-	-	-
4	3E	L4-1	1	1	1	0	-	-	-	-	-	-	↑	↓
		L4-2	0	1	1	1	↑	↓	↓	↑	↓	↑	-	-
3	2E	L3-1	0	1	1	0	↑	↓	↓	↑	↓	↑	↑	↓
		L3-2	0	1	0	1	↑	↓	↑	↓	↓	↑	↓	↑
2	E	L2-1	0	1	0	0	↑	↓	↑	↓	↓	↑	-	-
		L2-2	0	0	0	1	-	-	-	-	-	-	↓	↑
1	0	L1	0	0	0	0	-	-	-	-	-	-	-	-

Secondly, zero sequence voltage signal is injected into three phase voltage and acts as another control freedom. The main aim of ZSI is to regulate U_1 and U_3 voltage because neither switching state selection nor RLM could change the charging or discharging state of U_1 and U_3. Traversal method is used to find the optimised zero-sequence voltage through algorithm in DSP[26].The objective of this method is:

$$S = (U_{1\_trial} - E)^2 + (U_{3\_trial} - E)^2 \tag{1}$$

Here, U_{1_trial} and U_{3_trial} are modified capacitor voltages after ZSI:

$$U_{1\_trial} = U_1 + \frac{I_1}{C_1 * f_{sw}} \tag{2}$$

$$U_{3\_trial} = U_3 + \frac{I_3}{C_3 * f_{sw}} \tag{3}$$

I_1 and I_3 are current through capacitor U_1 and U_3 after ZSI. f_{sw} is the switching frequency. As shown in Fig.4, I_{m1_trial} and I_{m2_trial} are current through the dc capacitor connecting points. The current direction has been noted in Fig.4. I_1 and I_3 can be expressed by I_{m1_trial} and I_{m2_trial} according to capacitor paralleling rule:

$$I_1 = \frac{3}{4} I_{m1\_trial} + \frac{1}{4} I_{m2\_trial} \tag{4}$$

$$I_3 = -\frac{1}{4} I_{m1\_tiral} - \frac{3}{4} I_{m2\_trial} \tag{5}$$

I_{m1_trial} and I_{m2_trial} can be obtained by duty ratio and phase current:

$$I_{m1_{trial}} = I_A * \big((L_{4A} - 1) * D_{4A} + (L_{2A} - 1) * D_{2A}\big) + I_B * ((L_{4B} - 1) * D_{4B} + (L_{2B} - 1) * D_{2B}) + I_C * ((L_{4C} - 1) * D_{4C} + (L_{2C} - 1) * D_{2C}) \tag{6}$$

$$I_{m2_{trial}} = I_A * \big((2 - L_{4A}) * D_{4A} + (2 - L_{2A}) * D_{2A}\big) + I_B * \big((2 - L_{4B}) * D_{4B} + (2 - L_{2B}) * D_{2B}\big) + I_C * ((2 - L_{4C}) * D_{4C} + (2 - L_{2C}) * D_{2C}) \tag{7}$$

Here, I_A, I_B and I_C are phase current of A, B and C. D_{2A}, D_{3A} and D_{4A} are duty ratios of level 2, 3 and 4 for phase A, D_{2B}, D_{3B} and D_{4B} for phase B, D_{2C}, D_{3C} and D_{4C} for phase C. L_{4A}, $L_{2A}, L_{4B}, L_{2B}, L_{4C}, L_{2C}$ are chosen between 1 and 2. For example, L_{4A} is 1 when level 4 chooses *L4-2* and is 2 when level 4 chooses *L4-1* in phase A.

Combining (2)-(7), the best zero sequence voltage can be found to make S the smallest. Note that there is a tradeoff between the steps of interactive calculation and the accuracy of ZSI.

Thirdly, redundant level modulation is used to control U_4 voltage. Fig.5(a) illustrates the essence of RLM. Two voltage levels are used to replace one voltage level. Fig.5(b) shows how RLM is implemented with the carrier based phase disposition modulation. The modulation waveform is split into four parts:-1~-0.5, -0.5~0, 0~0.5, 0.5~1. In this way, modulation waveform parts can be moved higher or lower by ΔU and generate a better switching state combination when they are compared to carrier waves. For topology A, there are two kinds of RLM. One is to replace level 4 with level 3 and 5, the other is to replace level 2 with level 1 and 3. Switching states after RLM provide better current paths for U_4 balance and selection of switching states can be derived from Table I.

Some rules are needed in RLM. The combination of level 3, 4 and 5 is taken as an example. The original phase voltage after ZSI cannot be changed during RLM, thus:

$$D_5' + \frac{1}{2} D_4' = U_{ref} \tag{8}$$

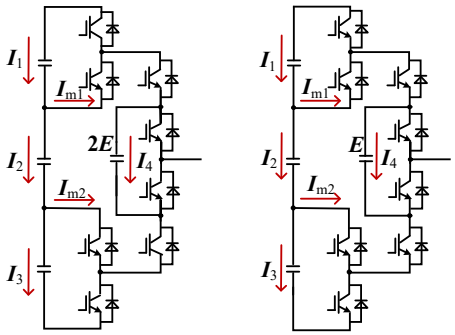


Fig.4. Current through capacitors. (a)Topology A. (b)Topology B.

D_5', D_4' and D_3' are the sum of the revised level 5, 4 and 3 respectively. Note that with the modulation method shown in Fig.5(b), the modifying change value of level 3 and 5 is the same, half of the value of level 4. The sum of duty ratios in one switching cycle is unit, so:

$$D_5' + D_4' + D_3' = 1 \tag{9}$$

According to capacitor voltage-current rule, relationship between duty ratios and the deviation of desired U_4 voltage and measured voltage(ΔU_4) can be obtained:

$$I(-D_{4-1}' + D_{3-1}' - D_{3-2}' + D_{2-2}') = C \cdot \Delta U_4 \cdot f_{sw} \tag{10}$$

$$\Delta U_4 = 2E - U_4 \tag{11}$$

Here, I is the instantaneously measured output phase current. D_{4-1}', D_{3-1}', D_{3-2}' and D_{2-2}' are decided by switching states. For example, if *L3-1* is selected, D_{3-2}' will be zero. If *L3-2* is selected, D_{3-2}' will equal to D_3'. U_4 can be measured by sampling circuits. In each switching cycle, one level only has one state. If *L4-1* and *L3-1* are chosen, revised duty ratio D_{4-1}' can be obtained combining (8)-(10):

$$D_{4-1}' = \frac{2}{3}(1 - U_{ref} - \frac{C \cdot \Delta U_4 \cdot f_{sw}}{I})(0 < D_{4-1}' < 1) \tag{12}$$

Usually, D_{4-1}' cannot be 0 or 1, otherwise, five level voltage wave will be incomplete. Some margin should be left depending on switching frequency and dead time. Also, D_{3-1}' and D_5' should also be within 0 and 1. Then the difference between original duty ratio and revised duty ratio of U_4 is:

$$\Delta D_4 = (D_{4-1} - D_{4-1}') \tag{13}$$

The modulation waveform should be split into four parts:

$$U_{ref1} = \begin{cases} U_{ref}, & U_{ref} < -\frac{1}{2} \\ 0, & U_{ref} \geq -\frac{1}{2} \end{cases} \tag{14}$$

$$U_{ref2} = \begin{cases} U_{ref}, & -\frac{1}{2} \leq U_{ref} < 0 \\ 0, & U_{ref} \geq 0 \ or \ U_{ref} < -\frac{1}{2} \end{cases} \tag{15}$$

$$U_{ref3} = \begin{cases} U_{ref}, & 0 \leq U_{ref} < \frac{1}{2} \\ 0, & U_{ref} \geq \frac{1}{2} \ or \ U_{ref} < 0 \end{cases} \tag{16}$$

$$U_{ref4} = \begin{cases} U_{ref}, & \frac{1}{2} \leq U_{ref} \\ 0, & U_{ref} < \frac{1}{2} \end{cases} \tag{17}$$

As Fig.5(b) shows, modulation wave U_{ref4} is raised by ΔU while U_{ref3} is decreased by ΔU, which generates level 5 and 3 to replace part of level 4. Modulation waves are represented by straight lines because one switching cycle is very short.

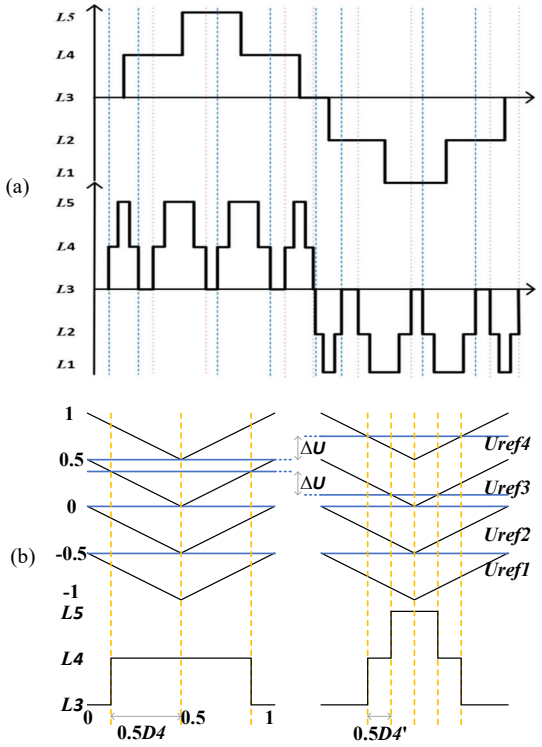


Fig.5. Illustration of RLM implementation. (a)Phase voltage before and after RLM. (b)Carrier waveform and PWM generation before and after RLM.

According to the geometry relationship in Fig.5(b), ΔU should be:

$$\Delta U = \frac{1}{4}\Delta D_4 = \frac{1}{4}(D_{4-1} - D_{4-1}') \tag{18}$$

Then the new modulation signals U_{ref1}'~U_{ref4}' can be expressed as:

$$\begin{bmatrix} U_{ref1}' \\ U_{ref2}' \\ U_{ref3}' \\ U_{ref4}' \end{bmatrix} = \begin{bmatrix} U_{ref1} \\ U_{ref2} \\ U_{ref3} - \Delta U \\ U_{ref4} + \Delta U \end{bmatrix} \tag{19}$$

There are two combinations in topology A: level 3, 4, 5 and level 1, 2, 3. And there are three combinations in topology B: level 1, 2, 3, level 2, 3, 4 and level 3, 4, 5. These RLM methods are all similar to the above process. The switching state of each level is decided in the first step.

This paper divides switching states of topology B into two groups by ΔU_4: *L4-1*, *L3-1*, *L2-1* and *L4-2*, *L3-2*, *L2-2*. The charging/discharging situations are shown in Table I. Then ZSI and RLM can be implemented in a similar way, so the detailed process is not included in this paper.

C. Voltage jump during deadtime

Deadtime is set in order to avoid both switches in one pair conducting simultaneously. It is noted that voltage spikes , up

TABLE III. SIMULATION PARAMETERS

Parameters	Value
DC-link Voltage V_{dc}	4000V
Carrier Frequency f_{sw}	2kHz
Fundamental Frequencyf_0	50Hz
DC-link Capacitors	C1=C3=1.47mF, C2=1mF
Flying Capacitors	C4=1mF
RL-Load	33ohms 3.68mH
Modulation Index	0-1
Power Factor φ	0-1

to 2E, exist in Topology A during the deadtime. It needs more control strategies to solve this problem.

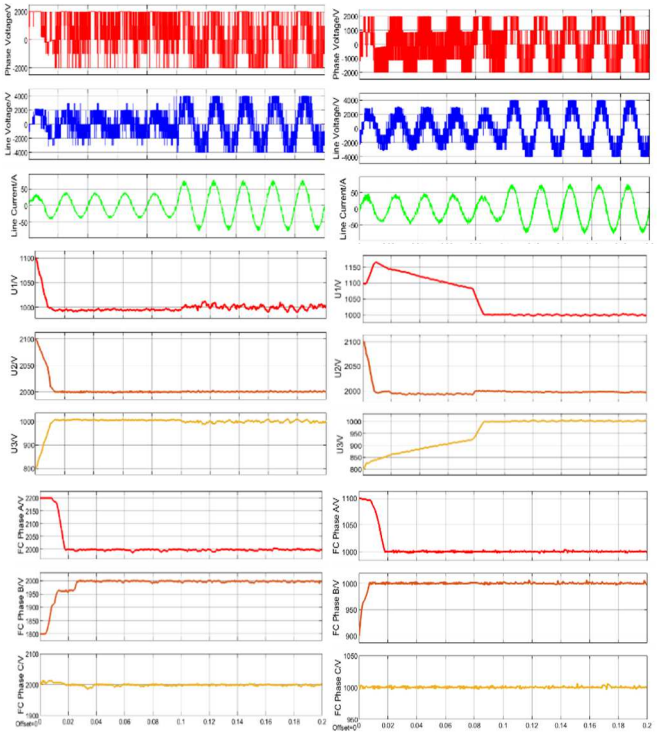
III. SIMULATION AND EXPERIMENT VERIFICATION

A.Simulation

A Matlab Simulink model is built to verify the proposed control method on the three-phase five-level systems with carrier based phase disposition modulation. The simulation parameters are listed in Table III.

The initial voltages are set as 1100V, 2100V, 800V for capacitor U_1, U_2 and U_3. The flying capacitor voltages of three phases are set as 2200V, 1800V and 2000V respectively for topology A and 1100V, 900V and 1000V respectively for topology B.

Fig.6 (a) and (b) illustrate phase voltage, line voltage, line current, voltages of three dc-link capacitors and three flying capacitors for topology A and B respectively at unit power factor. Modulation index increases from 0.6 to 1 at 0.1s. Despite the unbalance initial situation, both two converters reach the balance. Note that topology A responds faster to the voltage unbalance than topology B. Phase voltages and line voltages have the right number of voltage levels. It can be seen that voltage jumps exist in topology A, however, does not exist in topology B. Capacitor voltages are kept balanced well with a less than 1% ripple and ripples become a little larger when MI get larger.

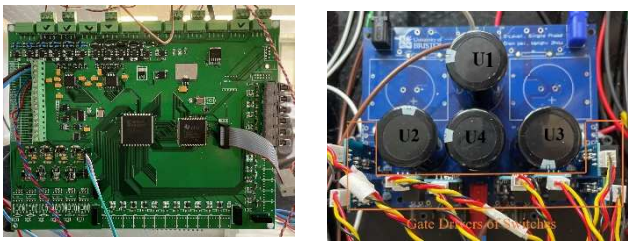


(a) (b)

Fig.6. Phase voltage, line voltage, line current, voltages of dc-link capacitor U_1, U_2, U_3 and flying capacitor per phase. (a) Topology A. (b)Topology B.

B. Experiments

To further verify the proposed control method, a downscaled test rig is built. The experiment parameters are the same as Table III, except that the dc-link voltage is reduced to 200V. The control board uses DSP(TMS320F28335) and FPGA (Xilinx XC3S400) to run the control algorithm. Switches employ IGBTs(K30H603) from Infineon. Fig.7(a) shows the control board and Fig.7(b) shows the circuit of one phase. Switches are connected to the heatsink under the gate drivers.



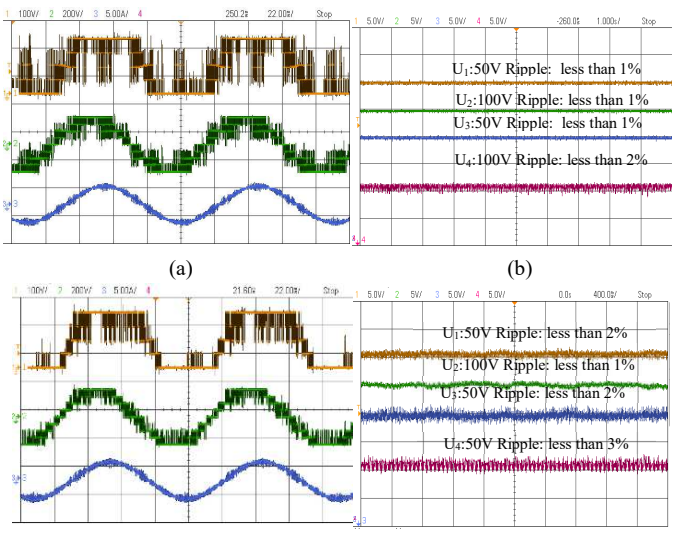
(a) (b)

Fig.7. Experimental prototype. (a)Control board. (b)One phase of converters

Fig.8 shows the converter performance under unit modulation and power factor. Fig.8(a) and (c) show the phase voltage, line voltage and line current of topology A and B respectively. The number of voltage levels all maintain correct: five levels in phase voltage and nine levels in line voltage. Larger voltage jumps can been seen in topology A, which is between *2E* and *3E*. Voltage jumps in topology B are avoided.

Fig.8(b) and (d) show the voltages of three dc-link capacitors(U_1-U_3) and one flying capacitor(U_4). All capacitors maintain a steady voltage. Voltage ripples of topology B are larger than those of topology A, which shows that topology A has a more powerful control ability. Note that phase voltage of topology B is restricted to 0 for a long time. This is caused by ZSI and limit the RLM use, thus reducing the control ability of the control method.

Fig.9 shows the implementation of RLM. Fig.9(a) and (b) show the RLM using com bination of level 1, 2, 3 and level 3, 4, 5 respectively in topology A. The voltage jumps during the deadtime are *2E*. Fig.9(c) shows the RLM combination of level 1, 2, 3 and level 2, 3, 4 in topology B. Fig.9(d) shows the RLM combination of level 2, 3, 4 and level 3, 4, 5.



(a) (b)

(c) (d)

Fig.8. Experiment waveforms at unit MI and power factor. (a)Phase voltage, line voltage and line current of topology A. (b)Capacitor voltages of topology A. (c) Phase voltage, line voltage and line current of topology B. (d) Capacitor voltages of topology B.

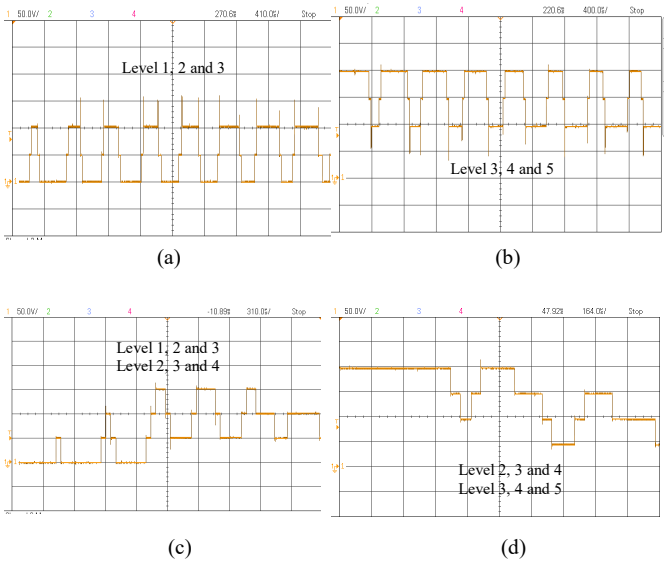


Fig.9. RLM process in experiments. (a)RLM combination of level 1, 2, 3 of topology A. (b)RLM combination of level 3, 4, 5 of topology A. (c)RLM combinations of level 1, 2, 3 and level 2, 3, 4 of topology B. (d)RLM combination of level 2, 3, 4 and level 3, 4, 5 of topology B.

IV. Conclusion

This work proposes a novel control method combining redundant switching state selection, zero sequence injection and redundant level modulation to solve the challenging voltage balancing in two new variations of 5L-HC converters. Both topologies share three dc-link capacitors for three phases and have one flying capacitor, eights switches per phase, while their characteristics differ. For the first time, this work effectively coordinate three modulation-based degrees of freedom to gain the full control of all capacitor voltages in these topologies, which cannot be achieved previously as reported in literature. The proposed method is verified by both simulation and experiments over the full range of modulation index and power factor. Additionally, a comparison between the two topologies has been conducted. Topology A has a higher control ability than topology B, while it suffers from a higher dv/dt during deadtime. The proposed control method can also be extended in other multilevel converters.

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