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Authors

Jiang, Junkai
Parto, Kamyar
Cao, Wei
et al.

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Ultimate Monolithic-3D Integration With 2D Materials: Rationale, Prospects, and Challenges

JUNKAI JIANG (Student Member, IEEE), KAMYAR PARTO (Student Member, IEEE), WEI CAO (Member, IEEE), AND KAUSTAV BANERJEE (Fellow, IEEE)

Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106, USA

CORRESPONDING AUTHOR: K. BANERJEE (e-mail: kaustav@ece.ucsb.edu)

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ABSTRACT As a possible pathway to continue Moore's law indefinitely into the future as well as unprecedented beyond-Moore heterogeneous integration, we examine the prospects of building monolithic 3D integrated circuits (M3D-IC) with atomically-thin or 2D van der Waals materials in terms of overcoming the major drawbacks of current 3D-ICs, including low process thermal budget, inter-tier signal delay, chip-overheating, and inter-tier electrical interference problems. Our holistic evaluation includes consideration of the electrical performance, thermal issues, and electromagnetic interference as well as attention to the synthesis methods necessary for low-temperature transfer-free 2D materials growth in M3D fabrication. Both in-plane and out-of-plane heat-dissipation in 3D-ICs made with 2D materials are evaluated and compared with those of bulk materials. Electrostatic and high-frequency electric-field simulations are conducted to assess the screening effect by graphene and effect of scaling down the inter-layer dielectric (ILD) thickness. Our analysis reveals for the first time that the 2D-based M3D integration can offer >ten-folds higher integration density compared with through-silicon-via (TSV)-based 3D integration, and >150% integration density improvement with respect to conventional M3D integration. Therefore, 2D materials provide a significantly better platform, with respect to bulk materials (such as Si, Ge, GaN), for realizing ultra-high-density M3D-ICs of ultimate thinness for next-generation electronics.

INDEX TERMS 3D integration, 2D layered materials, *h*-BN, MoS_2, WSe_2, beyond-Moore integration, electromagnetic interference, graphene, interconnect, interface thermal conductivity, Moore's law, thermal profile, vertically-stacked devices.

I. INTRODUCTION

As the technology node continues to scale down to sub-10-nm, the cost of advancement in conventional (single active-layer or single tier) CMOS technology tends to overcome the benefits from scaling-down of transistor feature-size, and moreover, interconnect latency, reliability, and bandwidth become the major bottleneck of system performance and energy efficiency improvements [1]–[4]. 3D integration employs multiple vertically-stacked active-layers (containing active devices such as transistors and diodes) for higher integration density, lower power consumption and better signal integrity, and provides a unique platform for heterogeneous integration of different active-layer materials and devices [5]. Through-silicon-via-based (TSV-based) 3D integration that has already been commercialized fabricates all tiers in parallel and then stacks them by a bonding process. Compared with standard back-end-of-line (BEOL) *via*s in planar CMOS technology, TSVs possess large dimensions, thereby creating large parasitic capacitance [6] and thermal/mechanical stress in the substrate. Additionally, defective TSVs create challenges in the testing of TSV-based 3D-ICs [7].

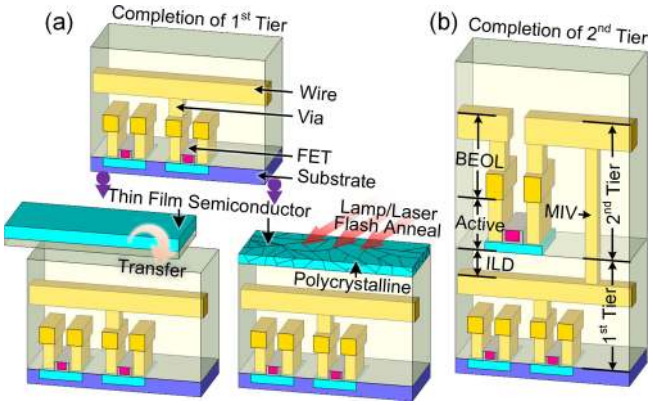

FIGURE 1. **Schematic of conventional monolithic 3D IC fabrication. (a) After the completion of 1st tier (upper figure), a layer of thin film semiconductor is transferred on top (lower left figure) or an amorphous semiconductor film is deposited and annealed to create a polycrystalline film (lower right figure). (b) The 2nd tier must be fabricated within the process thermal budget. The MIVs connect adjacent tiers.**

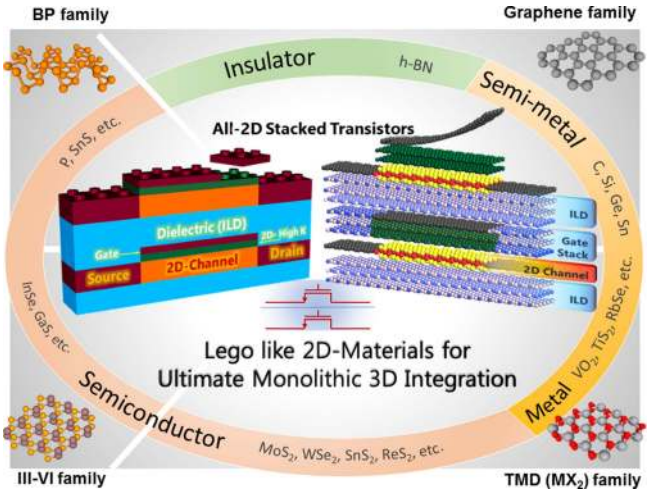

FIGURE 2. **2D materials offer a wide range of electronic properties, including insulator, semiconductor, and metal, in multiple families, as illustrated at the four corners. The inset schematic at the center shows two vertically stacked 2D FETs with *h*-BN as the ILD material.**

Monolithic-3D (M3D) integration is another type of 3D integration scheme, where multiple stacked tiers are fabricated sequentially on the same wafer via deposition/recrystallization of the upper tiers [5], [8] (Fig. 1). Each tier consists of active layer, BEOL layer and inter-layer dielectric (ILD) layer. Monolithic inter-tier-via (MIV) connects adjacent tiers and has similar diameters as *via*s in the BEOL process [9], allowing for higher MIV density w.r.t TSVs, which offers higher routability and design flexibility. In M3D, the process temperature of upper tiers should not exceed a critical temperature (∼500 °C). Violating this process thermal budget causes BEOL degradation, silicide deterioration and dopant diffusion in the lower tiers. However, the fabrication of upper active layers usually requires high-temperature processes such as crystallization and dopant activation. Although several low-temperature processes, including SOI bonding and flash lamp/laser annealing have been reported (Fig. 1), but none of them yield compatible performance and cost-effectiveness w.r.t their single-crystal counterparts. Other research efforts involve exploring high-mobility channel materials, including Ge [10] and InGaAs [11], in the upper tiers to compensate for degraded transistor characteristics from low process thermal budget.

Two dimensional (2D) van der Waals materials (Fig. 2), including graphene, and beyond-graphene 2D crystals (e.g., MoS_2 and WSe_2) [12] have recently shown great potential for next-generation electronics because of their unique 2D nature and ultimately thin bodies [13], [14]. The concept of building M3D-ICs with 2D layered materials was first proposed by Kang *et al.* [15]. Despite some experimental progress on stacking 2D-based devices [16], [17], the advantages of incorporating atomically-thin 2D-materials-based devices and interconnects in M3D integration scheme has only been recently studied by us [18]. In this paper, we present a more extensive version of our recent study and rigorously evaluate the prospects of M3D integration based on 2D materials. We demonstrate via extensive modeling and simulation why 2D materials enabled vertical-scaling is promising for M3D.

This paper is organized as follows. Section II describes the benefits from thinning down the tier thickness, or vertical scaling, in M3D. Section III discusses the feasibility and status of 2D material synthesis and requirements for their M3D integration. Section IV analyzes the thermal management in M3D with stacked 2D materials and its main challenge in combating interfacial thermal resistance. The effect of inter-tier electrical interference in M3D-ICs and strategies for their effective screening are discussed in Section V. Section VI concludes the paper.

II. BENEFITS OF VERTICAL-SCALING IN M3D

Wafer-thinning [19] is a necessary step in TSV-3D fabrication for reducing TSV dimensions and improving integration density. In comparison, M3D inherently offers thinner body thickness or active layer thickness of sub-100 nm, w.r.t ∼20 μm body thickness in TSV-3D ICs [19]. However, the body scaling of common channel materials, such as Si, becomes challenging at ultra-thin body thicknesses due to degradation of their mobility caused by the increase in electron scatterings from surface roughness [13]. On the other hand, 2D semiconductors with their atomically thin bodies and pristine interfaces, exhibit reasonable mobilities and immunity against surface defects, and become the ideal candidate for ultra-thin-body devices [14]. Moreover, these materials are intrinsically more flexible w.r.t conventional electronic materials, which can open up new pathways for flexible 3D-ICs. In this section, we show that further scaling down of the tier thickness in 3D-ICs, which is only possible with the integration of 2D materials, benefits the 3D system

in terms of signal delay, heat dissipation and integration density.

A. INTER-TIER SIGNAL DELAY

M3D offers the flexibility of placing circuits on different tiers to avoid routing congestions and achieve high integration density. However, this is at the cost of increased inter-tier signal delay because the MIVs are usually taller than the standard *via*s. The overhead of increased delay from placing circuits on different tiers can be minimized through design optimizations. In our simulations, a fan-out-of-4 (FO4) driver-interconnect-load circuit, where the load is placed at the same tier or at the adjacent tier to the driver (Fig. 3a,b), is simulated in HSPICE with 7-nm predictive technology models [20] for transistors and a distributed RC model for plugs, *via*s, MIVs [9] and wires (copper based) that are assumed to be of 20-nm in width. Lateral distance between the driver and the load is 100× minimum gate pitch. Compared with intra-tier signals, inter-tier signals suffer from larger delays because of relatively large MIV parasitics [9], and it is even more severe when tier thickness (or MIV height) increases (Fig. 3c). Thus, thinner tiers are preferred for reducing inter-tier signal delay.

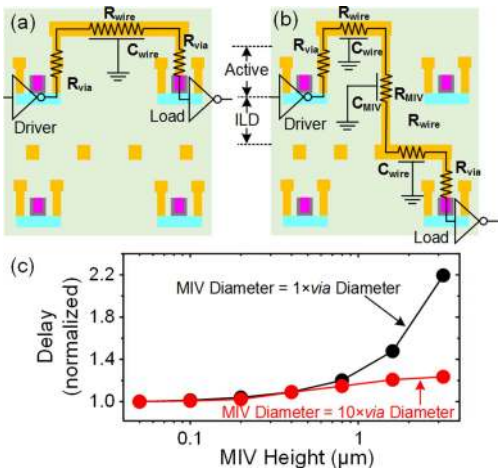

FIGURE 3. Schematic of (a) in-tier and (b) inter-tier fan-out-of-4 (FO4) driver-interconnect-load circuit in a M3D IC. R_{via}, R_{wire}, C_{wire}, R_{MIV} and C_{MIV} are *via* (plug) resistance, wire resistance and capacitance, MIV resistance and capacitance, respectively. (c) FO4 delay vs. MIV height for MIV diameter = 1× and 10× minimum *via* diameters. The delays are measured from the average of high-to-low and low-to-high delays, and normalized by the FO4 delay of in-tier driver-interconnect-load as in (a). In the simulations, barrier layer and size-effect are considered in the Cu wires and *via*s.

B. HEAT DISSIPATION

M3D-ICs not only produce significant heat that can potentially exceed chip package thermal design power (TDP), but also suffer from temperature rise with increasing number of stacked tiers because of tier thermal resistance (Fig. 4a) [21]. Such overheating effect on top tiers degrades the circuits' life time and increases the IC's power consumption. For example, the stacked DRAMs require an increased refresh frequency to compensate for their larger leakage currents at higher temperatures. This problem becomes even more severe when temperature dependence of subthreshold leakage power is considered [22]–[24].

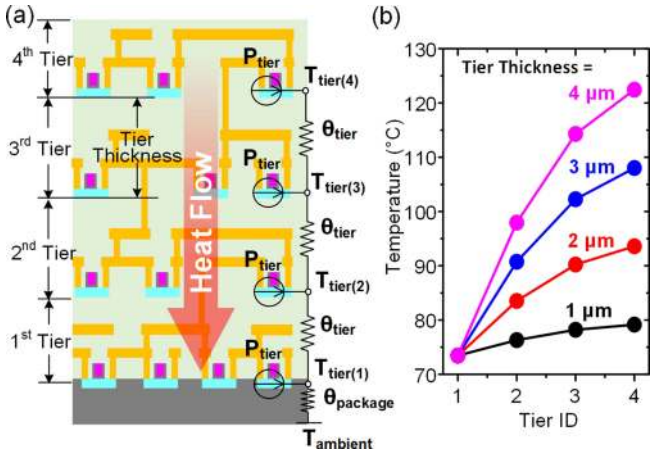

FIGURE 4. (a) Schematic of heat flow in a 4-tier M3D integrated circuit. Uniform power profile is assumed for each tier. (b) Simulated junction temperature of each tier (1-4, as in (a)) with different tier thickness (1-4 μm). Larger tier thickness results in larger tier thermal resistance, thus higher temperature at upper tiers.

In our thermal simulations, a thermal resistor network (Fig. 4a) is applied to model a 4-tier M3D-IC, where a uniform power density (P_{tier}) of 28.86 W/cm^2 reported in [25] is assigned to each tier. The thermal resistance of each tier (θ_{tier}) consists of thermal resistance of BEOL, active layer and ILD layer. The BEOL layer contains 6 metal layers (local and semi-global layers) with wire width to spacing ratio of 1, and its thermal resistance is estimated by considering the effects of metals and low-k dielectrics, via the method described in [26]. The ILD and active layers' thermal resistance values are estimated by assuming a uniform SiO_2 layer (worst case), and the thermal resistance effect of bulk semiconducting channels are neglected for simplicity. Different tier thickness in Fig. 4b is simulated by varying ILD thickness. The package thermal resistance ($\theta_{package}$) is calculated as reported in [21]. Finally, the temperature of each tier ($T_{tier(i)}$) can be calculated by Kirchoff's equations at an ambient temperature ($T_{ambient}$) of 35 °C. The results (Fig. 4b) show that thinner tiers exhibit smaller thermal resistance and alleviate the overheating effect.

III. 2D MATERIAL SYNTHESIS AND INTEGRATION IN M3D

2D semiconductor material family offers a wide range of properties with sizeable/controllable band gaps at atomic-level thickness (Fig. 2), which led to the demonstration of various 2D logic devices [27]–[31] and circuits [32]. Additionally, intercalation-doped multilayer 2D materials in the form of doped-graphene-nanoribbon (DGNR) interconnect have been demonstrated as a promising candidate for next-generation interconnects that offers >50% interconnect thickness reduction leading to significantly

lower parasitics, power consumption, and interconnect delays along with unprecedented reliability [33].

A. GRAPHENE

Graphene is known for its zero bandgap and large momentum relaxation time, thus is suitable for on-chip passive devices including interconnects [34], [35] and inductors [36]. Synthesis methods for graphene have witnessed significant progress in terms of thickness (mono-, bi-, and multilayer), stacking order control, crystallinity (large grain size and low defect density) and scalability (up to wafer scale) [37], [38]. Chemical vapor deposition (CVD) method is the most widely adopted for graphene growth. However, it requires a high-temperature process (∼1000 °C) and a wet transfer process of graphene from metal catalyst surface to the target substrate, which is not suitable for M3D integration. To satisfy the process thermal budget in M3D integration (< 500 °C), recently, CMOS-compatible DGNR interconnects fabricated at 300 °C have been demonstrated [39].

B. HEXAGONAL-BORON NITRIDE

Hexagonal-boron nitride (*h*-BN) exhibits a large bandgap (> 5.0 eV) and is electrically insulating with relatively small dielectric constant (< 4.0). In contrast to the low thermal conductivity of conventional low-k dielectrics (< 1 W/m-K [26]), *h*-BN, like other 2D materials, exhibits a very high in-plane thermal conductivity (> 200 W/m-K [40]) due to strong in-plane covalent bondings and has been used as front-end [41] and back-end [42] dielectric and passivation layer in 2D devices for enhancing the device performance. Growth methods of *h*-BN include CVD [43] and gas phase epitaxy [44]. These methods can control the number of layers and scale up to wafer-scale. However, like the graphene growth, they require high-temperature process that violates M3D thermal budget and a wet transfer process that hinders its application in large-scale manufacturing. Other *h*-BN growth methods exploit mechanical/liquid-phase exfoliation and satisfy the low thermal budget, but they have limited control over the number of layers and the film quality [45]. Overall, wafer-scale growth of high-quality *h*-BN films at low temperature remains challenging.

C. TRANSITION METAL DICHALCOGENIDES

Transition metal dichalcogenides (TMDs) are a family of semiconducting 2D materials and, unlike graphene, is normally synthesized directly on insulating substrates, such as SiO_2. Traditional CVD by vapor phase reaction or physical vapor transport is a common TMD growth method [46]. However, the CVD method requires high-temperature (∼1000 °C) process for high-quality TMD growth. Metalorganic chemical vapor deposition (MOCVD) that uses metal organic or organic precursors is another widely used method for TMD growth. Compared with conventional CVD, MOCVD enables precise control of precursors and has demonstrated wafer-scale TMD growth [47]. However, MOCVD still cannot satisfy the process thermal budget.

Atomic layer deposition (ALD) is a self-limiting chemical reaction process, in which gas precursors react with the substrate and layer-by-layer deposition is achieved. Precise control of layer number and effective thickness of the grown TMDs by varying the number of ALD cycles has been reported [48]. Although ALD allows low-temperature TMD growth (< 300 °C [48]), the dangling-bond-free surfaces of 2D TMDs limit the reactions, and, therefore, the crystallinity of the TMDs by ALD is poor and requires further improvements. Post-annealing process improves the TMD crystal quality, but high-temperature process of ∼800 °C is required [49]. TMD growth by molecular beam epitaxy (MBE) has also been demonstrated, but non-controllable layer thickness and limited TMD surface coverage problems remain challenging [50].

D. INTEGRATING 2D MATERIALS IN M3D

Although, similar to SOI bonding, integrating transferred 2D materials in M3D is possible, low-temperature transfer-free synthesis of 2D materials directly on M3D substrate is highly desired for cost-effectiveness. Graphene and TMDs are promising for M3D integration, as their low-temperature and transfer-free synthesis methods have been reported, while the integration of *h*-BN dielectrics is still challenging. In addition, optimal methods for patterning, terminating, and passivating these materials will be important. By incorporating 2D materials for both active and passive devices [51], we propose and evaluate the first fully integrated M3D-IC with 2D materials (Fig. 5).

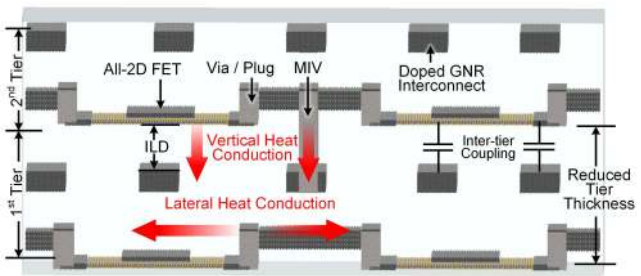

FIGURE 5. Schematic cross-section illustrating the proposed monolithic-3D integration with 2D materials. The 2D FETs exhibit atomic thickness while offering sufficient mobilities. The doped graphene nanoribbon (GNR) interconnects have been demonstrated to offer >50% thickness reduction. Vertical and lateral heat conduction pathways are marked by red arrows. Thin ILD can generate capacitive couplings between adjacent tiers.

IV. HEAT TRANSPORT IN M3D WITH 2D MATERIALS

The overheating problem [5] in 3D-stacking results from heat generation from multiple vertically stacked tiers and is intensified by the increased thermal resistance from each tier to the heatsink (Fig. 4a). Additionally, as threshold voltage (V_t) scales down, while subthreshold swing (SS)

stays almost unchanged (~60 mV/dec at room temperature) in conventional MOSFETs, subthreshold leakage power becomes a major component of total chip power. Moreover, the subthreshold leakage power increases as the temperature increases [24], which aggravates the overheating problem in monolithic 3D-ICs.

At the device level, high electric field at the drain side in a field effect transistor (FET) increases the energy of electrons and generates high energy phonons [52]. Due to the low velocity of optical phonons, this effect contributes to the formation of drain hot spots. These hot spots in FETs lead to degradations in carrier mobility and, eventually, to the breakdown of the 2D channel. When 2D FETs are incorporated in M3D, inherent thinness of 2D materials results in lower thermal resistance of the 2D channel (along out-of-plane direction) w.r.t the thermal resistance of its interfaces to surrounding metal contacts, dielectrics and substrate [53] (Fig. 6a-c). Therefore, the thermal behavior of 2D devices strongly depend on their interfacial thermal conductance (ITC), especially when the ILD thickness becomes less than a critical value (87/59 nm for MoS_2 channel with SiO_2/*h*-BN as interlayer dielectric, Fig. 6d) [54]. For thicknesses less than critical ILD (59 nm for *h*-BN and 87 nm for SiO_2), interlayer thermal conduction will be dominated by their ITC. Thermal conductivities of *h*-BN (out-of-plane) and SiO_2 thin films are reported to be 5.2 and 1.3 W/m-K respectively [55]. Measured ITC of MoS_2/SiO_2 is 15×10^6 W/m-K as reported in [56] and ITC of MoS_2/*h*-BN is simulated via *ab*-initio density function theory (DFT) simulations coupled with atomistic Green's function (AGF) phonon-transport method [54]. Hence, ITC becomes the most critical factor in determining the scaling, reliability and performance limits of M3D-ICs. The critical ILD thickness values determined by ITC set a lower bound on the scaling limit of the tier thickness in M3D-ICs made with 2D materials. Note that 2D transistors and interconnects significantly reduce M3D tier thickness, thus minimizing the total dielectric thermal resistance and self-heating in M3D (Fig. 4).

On the other hand, 2D materials exhibit excellent in-plane thermal conductivity. The thermal conductivities of bulk materials decrease as their thickness scales down, because of phonon (or electron in metals) boundary scatterings caused by surface roughness and interface defects [57]. Silicon thin films, where heat transport is mainly carried out by phonons, suffer from thermal conductivity degradation caused by boundary scatterings [57]. The thermal conductivity degradation also happens in Cu thin films, where heat transport is mainly contributed by the electrons, as shown in Fig. 7, where thermal conductivity in Cu thin films is estimated from fully diffusive surface electron scattering [58] and Wiedemann-Franz law (Lorenz factor $L = 2.31 \times 10^{-8}$ V^2/K^2 [59]). Such thermal conductivity degradation is not severe in 2D materials (Fig. 7). The in-plane thermal conductivity helps lateral heat spreading, which in turn can help removing thermal hotspots in M3D-ICs. For example, higher in-plane thermal conductivity

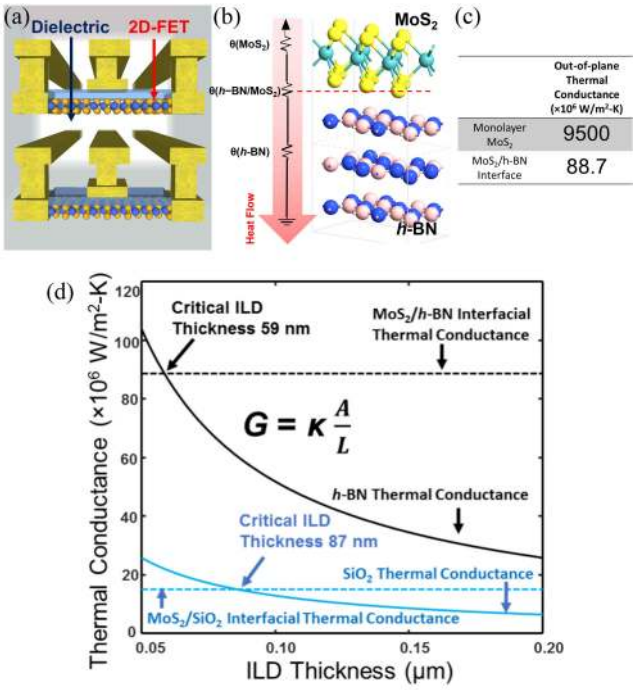

FIGURE 6. (a) Schematic of vertically stacked atomically-thin MoS_2 channel FETs in M3D with *h*-BN dielectric (ILD). (b) Thermal resistance network of vertical heat dissipation in channel region. (c) For monolayer MoS_2 with thickness of about 6.5Å and out-of-plane thermal conductivity of 4.75 W/m-K [55], the corresponding thermal conductance normalized by the area, given by G/A, is 9500 W/m^2-K. This implies that the thermal resistance of the channel is negligible compared to the interface thermal resistance of MoS_2 and *h*-BN and, hence, the interface becomes the main bottleneck for heat-transfer in the out-of-plane direction. (d) Out-of-plane thermal conductance (normalized by the area, G/A) of interlayer region vs. interlayer thickness for MoS_2 FETs with both *h*-BN and SiO_2 as interlayer dielectric. *G* is the absolute thermal conductance, κ is the out-of-plane thermal conductivity, *A* is the cross-sectional area and *L* is the ILD thickness. The interface becomes the dominant factor in out-of-plane heat conduction, as one reduces the ILD thickness.

of multi-layer graphene w.r.t Cu can help alleviate thermal gradients and improve thermal-integrity in long global interconnects [65], [66].

V. ELECTRICAL INTERFERENCE AND THEIR SCREENING BY 2D MATERIALS

Thin ILD in M3D allows capacitive coupling between adjacent tiers (Fig. 5). This vertical electrical interference causes noise coupling between tiers, and unwanted threshold voltage (V_t) variations [8] that can potentially increase leakage current/power and reduce ON-current. In M3D with 2D, ΔV_t increases to 30% of V_t when ILD thickness is scaled down to 10 nm, from TCAD simulations (Fig. 8a). In the TCAD simulations, we used a standard semiconductor, in which material parameters are modified for few-layer MoS_2, ultra-thin-body structure with a body thickness of 3 nm to study the electrostatic bias from the noise source (Fig. 8b-d). Note that similar ΔV_t is predicted for M3D with FinFET [67]. Previous works have highlighted this vertical electrical interference issue between interconnects and devices [9] in different tiers with measured results, and placing conductive

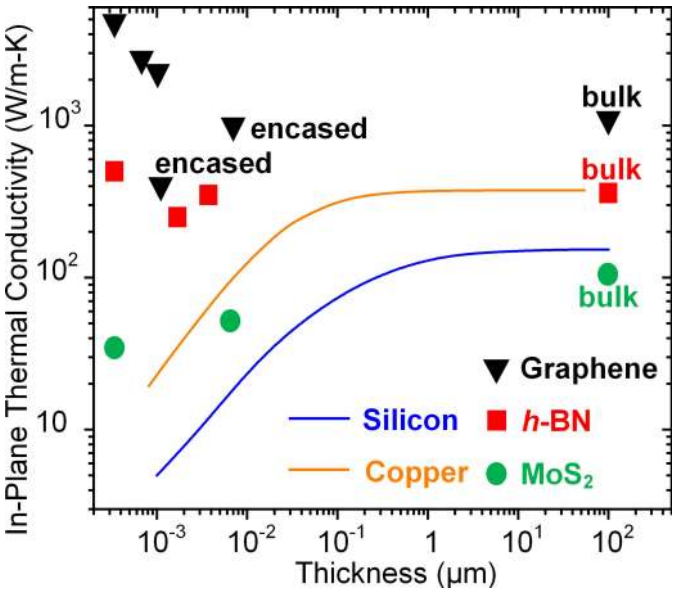

FIGURE 7. **In-plane thermal conductivity *vs.* film thickness for bulk materials (simulated for silicon [57] and copper [58]), graphene, *h*-BN, and MoS_2 (from monolayer to bulk). The thermal conductivities of 2D materials are collected from reported experimental work [40], [60]–[64]. 2D materials are suspended samples by default, unless marked as 'encased' (by SiO_2).**

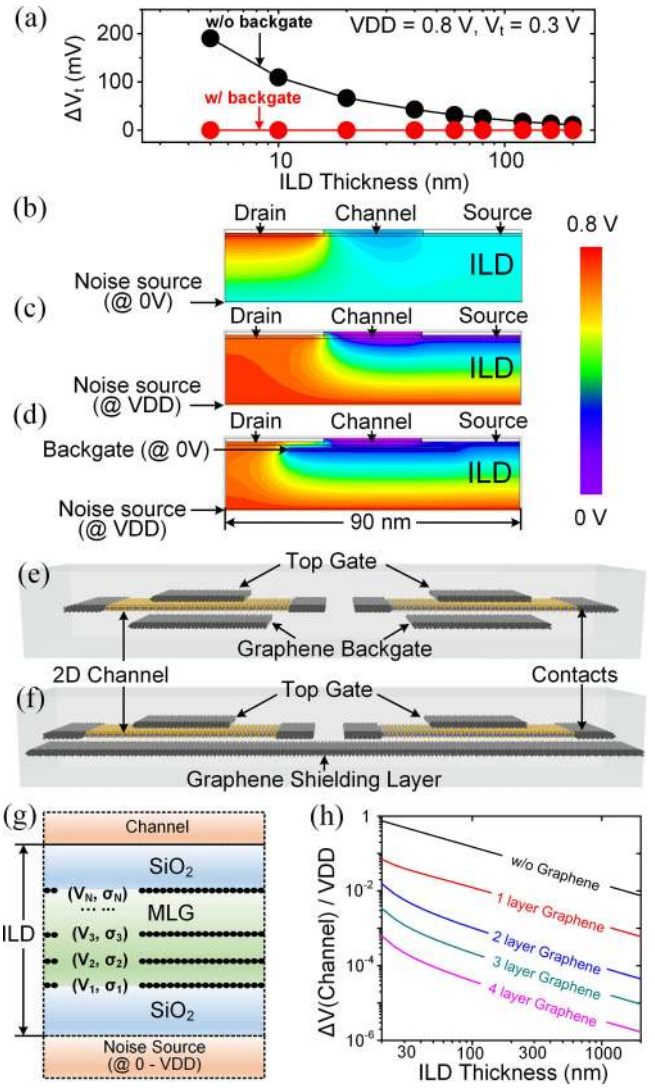

FIGURE 8. **(a) Threshold voltage variation of an upper-tier FET vs. ILD thickness for M3D with 2D materials with and without grounded graphene backgate. Potential distribution in a 20 nm thick ILD layer is plotted for (b) noise source at 0 V without grounded graphene backgate, (c) noise source at VDD without grounded graphene backgate and (d) noise source at VDD with grounded graphene backgate. The noise source is at fixed electrostatic bias in the simulations. (a)-(d) are from Silvaco TCAD simulations. For controlling electrostatics of top-tier FET, grounded graphene (e) backgate or (f) shielding layer is inserted in the ILD layer. (g) Schematic of simplified noise coupling model with existence of multilayer graphene (MLG) shielding in ILD layer. (h) Simulated 2D channel potential variation (when noise source potential changes from 0 to VDD) *vs.* ILD thickness for various graphene backgate/shielding layer thickness of the structure in (g).**

thin films between tiers for interference screening (Fig. 8d) has been proposed [68]. In this work, to minimally impact the 3D-IC thickness, we propose to use a layer of 2D metallic material (e.g., graphene) in ILD (as backgate or shielding layer, Fig. 8e,f) for noise screening. In this section, the screening effect of graphene layer is studied by both electrostatic and electrodynamic (high-frequency electric field screening) analysis.

A. ELECTROSTATIC SCREENING

The 2D material (graphene) in monolayer or few-layer form possesses relatively low density-of-states (DOS), compared with bulk metals, because of the quantum confinement effect. Unlike in a bulk metal, where sufficiently high surface carrier density can be achieved, the net surface carrier density in graphene is a function of its potential, or the Fermi level (E_F) with respect to the Dirac point. Different graphene layer numbers and doping levels result in different electrostatic screening effects.

We developed an in-house simulator to model the vertical interference with a multilayer graphene shielding layer (Fig. 8g). The electrical potential (V_1, V_2, ..., V_N), obtained from Gauss's law, and surface charge density ($\sigma_1, \sigma_2, \ldots, \sigma_N$), obtained from Fermi-Dirac distribution of each graphene layer are solved self-consistently until convergence is reached. The in-plane and out-of-plane dielectric constants of graphene are 1.8 and 3, respectively [69]. The vertical electrical interference becomes stronger as the ILD thickness decreases (Fig. 8h). Although 2D materials exhibit low DOS that tends to lower their capacity of electrostatic screening, 2-layers of graphene (~0.7 nm thick) is found to be sufficient for suppressing the capacitive coupling to $<$ 1%, when ILD thickness is $<$ 100 nm. Note that the DOS of doped graphene at the Fermi level is higher compared to that of undoped graphene, which will further enhance the electrostatic screening effect.

B. HIGH-FREQUENCY ELECTRIC FIELD SCREENING

The electromagnetic interference is a serious concern in mix-signal circuit designs, especially in monolithic 3D, where heterogeneous integration is desirable. The high-frequency

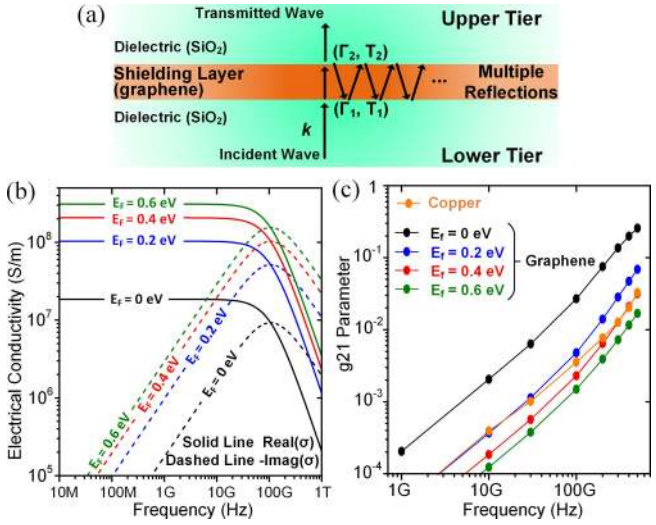

FIGURE 9. (a) Schematic of high-frequency electric field screening by a conductive layer. (Γ_1, T_1) and (Γ_2, T_2) are the reflection and transmission coefficients of the bottom and top surfaces, respectively. (b) Graphene electrical conductivity (σ) *vs.* frequency for different doping levels ($|E_F| = 0, 0.2, 0.4$ and 0.6 eV). (c) Network parameter g_{21} vs. frequency for copper and graphene with different doping levels from ANSOFT's High Frequency Structure Simulator (HFSS) simulations. The screening layer thickness for both graphene and Cu is fixed at 1 nm. The carrier scattering time in graphene is 3 ps, and surface scatterings in Cu are considered. Larger g_{21} indicates stronger capacitive coupling and weaker screening effect.

electric field interference screening by metal conductors and graphene is studied in this section. The screening effect is the result of interface reflection, wave absorption and multiple reflection and transmissions in the screening layer (Fig. 9a). In this study, few-layer graphene (1 nm, approximately 2-3 layers doped graphene) is explored as the screening layer for high-frequency electrical interference screening. Note that the layer separation in the intercalation doped few-layer graphene restores its linear band dispersion property as in monolayer graphene [36].

The scattering parameter S_{21}, which describes the power transferred from one tier to the other, was used to quantify coupling between adjacent tiers and simulations predict that screening effects will be negligible when screening layer thickness is reduced to 1 nm in previous studies [68]. This is because, under quasistatic approximation (the geometries are much smaller than the wavelength in the frequency range under study), although the electric field is effectively screened by the conductive layer, the magnetic field leaks through it, which causes power transmission through inductive coupling. However, in monolithic 3D-ICs, capacitive coupling by electric field dominates the inter-tier coupling, whereas the inductive coupling by magnetic field is negligible because of the small geometries of the interference source (e.g., local and semi-global wires) and victims (e.g., transistors), as well as weak magnetic fields. Hence, we propose to use another existing network parameter g_{21}, which describes the voltage amplification factor of capacitive coupling, to measure the crosstalk between tiers, and screening efficiency of the screening layer.

Furthermore, as we are studying the electric field screening by graphene screening layer in the high-frequency range (> 1 GHz), a dynamic in-plane electrical conductivity model for graphene is necessary. By neglecting the magnetostatic-bias-induced in-plane anisotropic effect (in capacitive coupling within sub-THz regime, as described above) of graphene conductivity, we utilize a *Drude-like* graphene surface conductivity model [70] (1),

$$\sigma_g = -j\frac{e^2 k_B T}{\pi\hbar^2(\omega - j2R)}\left[\frac{E_F}{k_B T} + 2\ln\left(1 + e^{-\frac{E_F}{k_B T}}\right)\right] \quad (1)$$

where k_B is the Boltzmann's constant, T is temperature, $\hbar$ is the reduced Planck's constant, ω is the circular frequency, R is the scattering rate in graphene, and E_F is the Fermi level in graphene (modulated by doping graphene). The *Drude-like* model arises from the fact that graphene's electrical conductivity cannot be described solely by the classical Drude model, due to its linear band dispersion and a zero effective mass. Hence, to correctly model and study the transport of Dirac fermions, quantum mechanical models in the framework of Boltzmann Transport Equation (BTE) have been developed specifically for graphene to work-around this problem. It is found that, at high frequencies, graphene still exhibits a similar frequency dependency in electrical conductivity compared to conventional materials [71].

Graphene's electrical conductivity and screening efficiency can be enhanced by doping (e.g., intercalation doping, chemical doping, etc., Fig. 9b). Graphene's out-of-plane electrical conductivity is assumed to be 10^3 times lower than the in-plane conductivity [72]. The calculated anisotropic graphene conductivities are used in defining the graphene properties in HFSS simulations. It is worthwhile to note that we assume a constant electrical conductivity of Cu, with consideration of surface scatterings in the frequency range of simulations, because the scattering time τ of carriers in thin Cu film (thickness of 1 nm) is on the order of 1 fs [73] that corresponds to a much higher frequency than the studied frequency range. Thus, the high-frequency electrical conductivity degradation of Cu films can be neglected based on the Drude model. Moreover, for both the extremely scaled (~1 nm) Cu and graphene shielding layers, the corresponding high frequency skin- and anomalous-skin effects [35], [74] do not play a significant role because the respective skin depths are larger than the film thickness, and hence, can be safely neglected.

In the studied frequency range (1 GHz – 500 GHz), g_{21} increases with frequency, indicating capacitive coupling becomes stronger as frequency increases (Fig. 9c). Moreover, doping of graphene can effectively enhance the screening efficiency of graphene screening layer, and graphene with doping level of E_F larger than 0.4 eV shows better screening efficiency than Cu for frequency smaller than 300 GHz. Note that the required doping level ($|E_F| > 0.4$ eV) was demonstrated in our experiments [33]. More importantly, metal thin film of thickness of 1 nm in this simulation is far from being achieved in fabrication. In summary, although the vertical

electrical interference becomes more severe with the scaling down of tier thickness in M3D, the conductive 2D (graphene) screening layer can be a promising solution to this problem.

The thinned bulk Si in TSV-3D is around 20 μm [19] for robust handling process, whereas the M3D eliminates the need for bulk Si substrates in stacked tiers. As discussed in Section V-A, to suppress the capacitive coupling to $< 1\%$, the ILD layer thickness is required to be > 2 μm (Fig. 8h). Therefore, the electrical interference between adjacent tiers in M3D prohibits further thinning of the stacked tiers. In the proposed M3D with 2D, the vertical electrostatic and electromagnetic interference can be screened by doped few-layer graphene in the ILD layer, enabling a pathway for scaling the ILD layer thickness to below 100 nm without inter-tier couplings. This thickness reduction in ILD enabled by incorporating 2D materials also leads to a decrease of the tier thermal resistance that minimizes the temperature increase in the top tiers (Fig. 4b), and allows more stacked tiers, compared with that in TSV-3D or conventional M3D. Note that the use of low-k (dielectric constant < 3.9) materials in the ILD stack promises even smaller ILD thickness, but their integration in M3D requires further investigation. Additionally, a wire thickness reduction of 50% by using doped GNR interconnect leads to approximated 25% reduction in BEOL thickness, which consists of 6 local and intermediate interconnect layers, as reported in [25]. The corresponding tier thickness for TSV-3D, M3D and M3D with 2D materials are plotted in Fig. 10a. The consequent integration densities (assuming 100 nm ILD for 2D-M3D) are estimated from the number of tiers per unit thickness and shown in Fig. 10b, provided all thermo-mechanical constraints are satisfied.

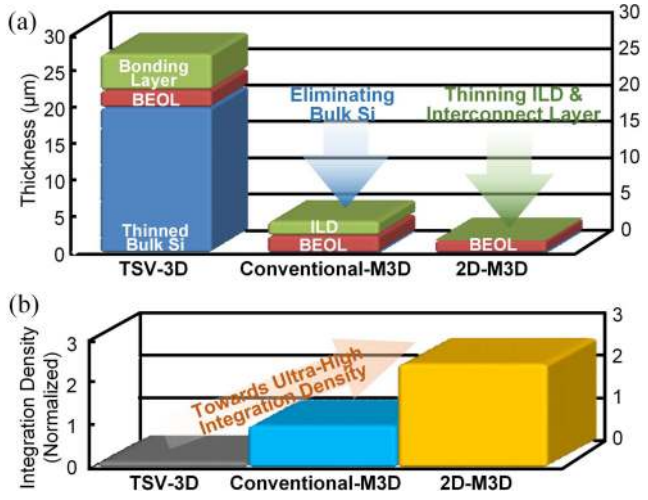

FIGURE 10. (a) Estimated tier thickness for TSV-based 3D integration (TSV-3D), conventional monolithic-3D (Conventional-M3D) and proposed monolithic-3D integration with 2D materials (2D-M3D). (b) Predicted integration density of TSV-3D, conventional M3D and proposed 2D-M3D, assuming a fixed total 3D integration thickness (or vertical height). The integration densities are normalized w.r.t the integration density of conventional-M3D.

VI. CONCLUSION

In this paper, we provided the rationale and underlined the prospects for monolithically integrating various 2D materials in future heterogeneous 3D-ICs. While identifying the 2D materials growth and integration challenges, we showed how their excellent electrical and thermal properties can be uniquely harnessed to overcome several major problems that plague conventional monolithic-3D integration. For example, owing to the atomically-thin vertical dimensions of 2D semiconducting channel materials, significantly ($> 50\%$) lower graphene interconnect thickness, and carefully-designed inter-tier electrostatics with graphene shielding layer that also benefits from enhanced heat dissipation, aggressive scaling of tier thickness down to sub-μm can be achieved. Such a scaling allows $>$10-folds higher integration density w.r.t TSV-based 3D integration, and $>150\%$ integration density improvement w.r.t conventional M3D integration (Fig. 10b), with possibility for further improvements via incorporation of appropriate low-k ILD materials. Thus, our analysis reveals that Moore's law can be extended well beyond the foreseeable roadmap of transistor scaling and unprecedented beyond-Moore heterogeneous integration can be realized by monolithic integration of 2D materials in 3D-ICs.

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JUNKAI JIANG (S'12) received the B.Sc. degree in microelectronics from Peking University, Beijing, China, in 2012. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of California, Santa Barbara, CA, USA.

His current research interests include the modeling, design and fabrication of emerging interconnect structures and materials, and 3-D integration.

KAMYAR PARTO (S'18) received the B.Sc. degree in engineering science and electronics from the University of Tehran, Iran, in 2017. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of California, Santa Barbara. His research lies in exploration and engineering of quantum materials for novel energy convertors and beyond CMOS electronic devices.

WEI CAO (S'12–M'17) received the Ph.D. degree in electrical and computer engineering with the University of California, Santa Barbara, CA, USA.

He is currently a Post-Doctoral Researcher with the Nanoelectronics Research Laboratory, University of California, Santa Barbara, where he is involved in design, fabrication, and the circuit exploration of 2-D material-based electron devices.

KAUSTAV BANERJEE (S'92–M'99–SM'03–F'12) received the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1999.

He is currently a Professor of electrical and computer engineering and the Director of the Nanoelectronics Research Laboratory, University of California, Santa Barbara, CA, USA.