ULTRA BROADBAND LOW POWER MMIC AMPLIFIER

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Abstract – **A low power two-stage InP HEMT MMIC amplifier has been developed. The amplifier utilizes 0.12 µm T-gate InP HEMTs with 2×25 µm gate periphery. This compact microstrip MMIC is only 1.5 mm^2 in size. It exhibits gain of 12.5±1 dB at 15 mW of dissipated power over an operating range from 1 to 50 GHz. The gain·bandwidth/dissipation figure of merit is 40 dB·GHz/mW. The average noise figure is 3 to 3.8 dB over the Ka band.**

I. INTRODUCTION

Ultra broadband amplifiers are an attractive component as general building blocks in systems such as instrumentation and measurement equipment as well as broadband communications. They can also be cost effective since they can be used in many applications. Additionally, next generation fiber-optical receivers with 40 Gbit/s or higher will require ultra wideband amplifiers.

Typical circuit configurations for designing multi-octave amplifiers are feedback and distributed or traveling wave amplifiers [1]. A traveling wave amplifier with 7 dB gain from 1 to 112 GHz using InP HEMT technology has been reported [2]. One disadvantage of the distributed amplifier is that they require large chip area, which increases cost. Additionally, they may consume significant power, making them less attractive for low power applications. Feedback Darlington amplifiers using HBT devices have been reported [3,4]. In [3] a SiGe HBT was presented with 9.5 dB of gain from DC to 18 GHz, 50 mW of power consumption and noise figure of 5.3 dB. In [4], a 50 GHz InP/InGaAs HBT amplifier was reported with 9.8 dB of gain and 110 mW of DC power.

In this work, we present a 1-50 GHz AlInAs/GaInAs/InP HEMT amplifier with 12.5±1 dB of gain with only 15mW of dissipated power. The circuit configuration is extremely simple with resistive gate and drain loading and microstrip line peaking in the drain bias lines. InP HEMT technology is the best choice for this application due to its exceptional performance in terms of maximum oscillation frequency (f_{max}), gain and noise figure.

II. DEVICE AND PROCESS TECHNOLOGY

The amplifier is designed using a 0.12 µm T-gate AlInAs/GaInAs/InP HEMT devices with 2×25 µm gate periphery. Small gate width is chosen in order to reduce DC power consumption. The material structure used for fabrication of the HEMTs is shown in Fig. 1. The devices exhibit a dc transconductance of 1090 mS/mm and breakdown voltage of 4 V.

The device S-parameters were measured on wafer using a TRL calibration from 10 to 50 GHz. A HEMT small signal model was then developed and used in simulation. Fig. 2 shows the agreement between the measured and modeled S_{21} and maximum stable gain (MSG) or maximum available gain (MAG). f_{max} can be determined by extrapolating the model above 50 GHz.. The estimated f_{max} is about 530 GHz. The extrinsic cutoff frequency (f_τ) is estimated to be about 160 GHz by extrapolating H_{21}, as seen in Fig. 3.

The device noise behavior is modeled using an effective temperature of the output (drain-source) resistor, as described in [5]. The noise model also has a current noise source between gate and drain to model the gate leakage current.

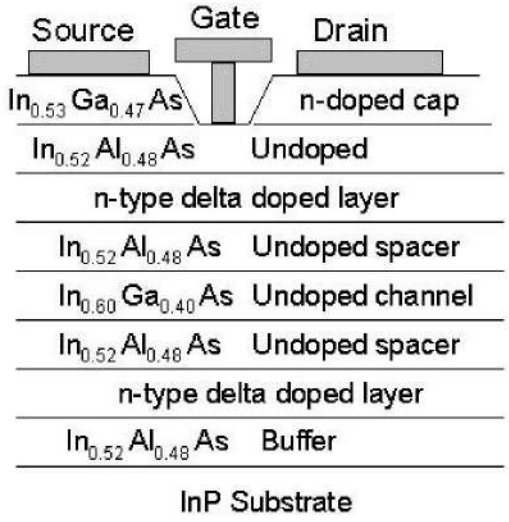

Figure 1: InP HEMT layer structure.

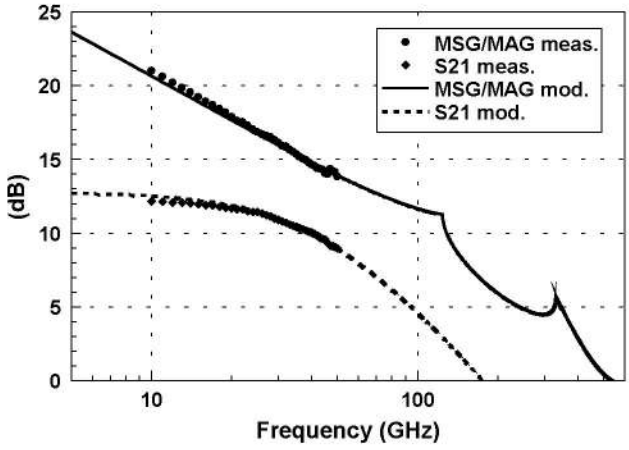

Figure 2: Measured and modeled S_{21} and MSG/MAG for a 2×25 µm HEMT.

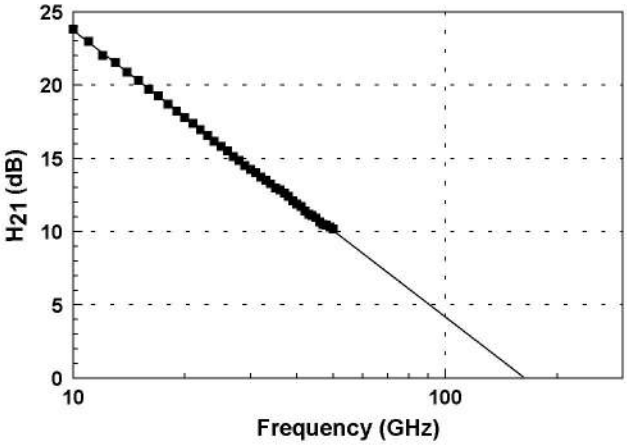

Figure 3: Measured H_{21} for a 2×25 µm HEMT.

III. AMPLIFIER DESIGN AND MEASUREMENTS

A two-stage microstrip amplifier is designed using HP-EEsof SeriesIV software. The amplifier configuration is quite simple. The gate and drain bias is provided though 10 KΩ and 40 Ω resistors, respectively. The drain resistor is used for matching and flattening the gain. The microstrip lines are kept short to improve the bandwidth, with the exception of the microstrip line in the drain bias, which is used as a peaking inductance.

The microstrip MMIC was fabricated on 625 µm thick semi-insulating InP substrate. The wafer was then thinned to 50 µm. This process also includes a wet etched backside via holes, which are necessary for the microstrip design. Fig. 4 shows a photograph of the fabricated amplifier. The chip size is only 1.5×1 mm^2 and is dominated by the coplanar probe launchers and capacitors. Moving some of these capacitors off-chip can further reduce the chip size.

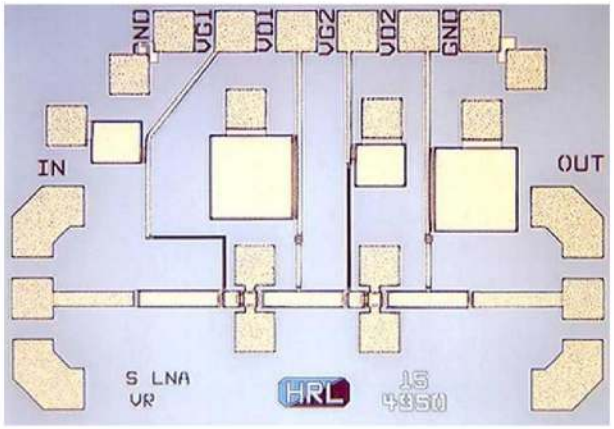

Figure 4: Photograph of the 1-50 GHz MMIC. The die size is 1.5×1 mm^2.

The amplifier S-parameters were measured using a HP8510C network analyzer from 0.5 to 50 GHz. The system is calibrated to the probe tips using SOLT standards on an impedance standard substrate. The measured and simulated S-parameters are shown in Fig. 5. The measurements were taken with the amplifier biased at drain voltage of 1 V and total drain current of 15 mA. The amplifier demonstrated a gain of 12.5±1 dB at only 15mW of dissipated power from 1 to 50 GHz. The upper design frequency limit extends beyond 50 GHz, but has not yet been measured due to test equipment limitations. The lower frequency limit can be extended below 1 GHz and is limited by the size of the DC-blocking capacitors. The gain·bandwidth/dissipation figure of merit for this amplifier is exceptional, measured to be 40 dB·GHz/mW.

The amplifier noise figure was measured from 1 to 26 GHz and from 26.5 to 39 GHz using HP8970B noise figure meter and external mixers. In both cases the system was calibrated using an on-wafer thru line. Figs. 6 and 7 show the measured noise figure in two bands. The ripples in the noise figure are due to the source and amplifier reflections that have not been calibrated out. A longer cable is used between the source and DUT in the second band (26.5-39 GHz) and therefore the ripples are more pronounced. In the first band (1-26 GHz), the amplifier noise figure is between 3.5 and 4 dB. In the second band, the amplifier noise figure is between 3 and 3.8 dB if the ripples are averaged out. The noise improves at higher frequencies due the fact that the optimum noise match for 50 µm device is closer to 50 Ω at higher frequencies.

The noise figure can be improved if device size is chosen so that the optimum impedance for noise is close to 50 Ω. However, this would involve using a larger device and would increase the DC power.

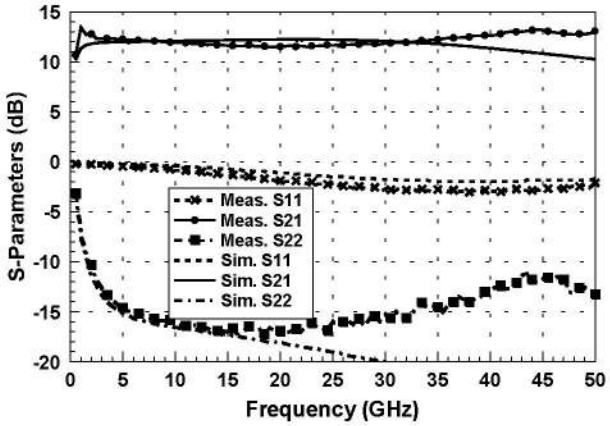

Figure 5: Measured amplifier S-parameters.

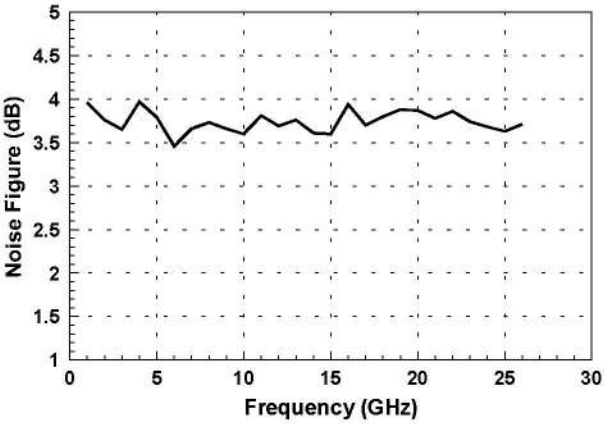

Figure 6: Measured amplifier noise figure from 1 to 26 GHz.

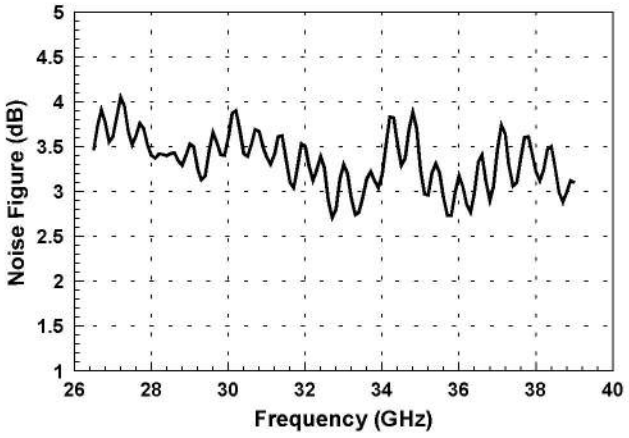

Figure 7: Measured amplifier noise figure from 26.5 to 39 GHz

IV. CONCLUSION

A monolithic, resistively loaded two-stage amplifier is designed and fabricated. The amplifier uses 50 µm InP HEMT devices. This compact MMIC chip is 1.5 mm^2 in size. A flat gain of 12.5 dB is demonstrated from 1 to more than 50 GHz. This amplifier consumes only 15 mW of DC power. The average noise figure is between 3 and 3.8 dB in Ka band.

This low power broadband amplifier is suitable for use in high bit rate fiber-optics receivers, broadband communications or instrumentation.

V. REFERENCES

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