

Ultra Compact Three-phase PWM Rectifier

P. Karutz, S.D. Round, M.L. Heldwein and J.W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
Zurich, 8092 SWITZERLAND
karutz@lem.ee.ethz.ch

Abstract – An increasing number of telecom, data server and aircraft power supply applications require high power, highly efficient, compact, sinusoidal input current rectifiers. The design and experimental performance of an 8.5 kW/liter (139 W/in³), 3-phase PWM rectifier with a power output of 10 kW is presented. The high power density is achieved by increasing the switching frequency up to 400 kHz, which results in smaller EMI filters and boost inductors, while still maintaining a high efficiency over 95%. To minimize the switching losses, a combination of a CoolMOS and SiC diode are used in a custom power module. The module together with an optimized forced air cooled heat sink, optimized EMI filter, and a fully digital controller are used to obtain the high power density of the rectifier.

I. INTRODUCTION

The historical trend in power electronics, especially for power supplies, has been the increase in power density [1]. Based on this trend it is predicted in [1] that the power density will approach 30 kW/liter (500 W/in³) after 2015. Increasing the power density results in a smaller, more compact system that should also have lower production costs. However with higher power densities it is important to have a high efficiency as power losses are difficult to remove from small volumes. The European Center for Power Electronics (ECPE) has identified a roadmap where they are targeting a power density of 50 kW/liter (820 W/in³) for power supplies [2]. We at ETH Zurich are an ECPE Competence Center that is developing both ac-dc and dc-dc converters along the roadmap path.

New applications for high power density converters are in more-electric aircraft power supplies [3]. In this aircraft application, the weight and size of the converter are important as well as meeting the required specifications for sinusoidal input current quality and EMC performance. One of the challenges is that the aircraft power system is moving towards a variable frequency ac voltage in the frequency range of 360 to 800 Hz. To be able to control the current to be sinusoidal requires a current controller bandwidth in the order of 20 kHz, therefore this in turn requires the switching frequency of an active rectifier to be in the hundreds of kHz [4]. Increasing the switching frequency has the added benefit that the size and weight of the passive components can be decreased.

A further application area is in telecom and data server power supplies, where an increasing number of systems require high power, highly efficient, compact, sinusoidal input current rectifiers [5]. The input stage of these power supply systems can be realized with either a modular topology using a star-connection [6] or delta-connection [7] of single-phase boost rectifier modules with individual DC output voltages, or a

direct three-phase rectifier topology, such as the Vienna Rectifier in [8], where the DC output voltage is common to all phases. The three-level structure of the Vienna Rectifier results in a low blocking voltage stress on the power semiconductors and a small input inductor volume. Therefore, the Vienna Rectifier is the ideal choice for the implementation of a high power, unity power factor rectifier that also has a high power-density.

The Vienna Rectifier topology can be implemented with either three switches [6] or six switches. In this design, a six switch Vienna Rectifier (see Fig. 1) is selected as it has lower conduction losses since the phase current flows through only one diode in each phase during the switch conduction and it is guaranteed that the switch voltage is clamped to half the output voltage. The rectifier presented in this paper is designed to operate over a wide line-to-line input voltage range of 160 to 480 V_{RMS}, with a nominal input voltage of 400 V_{RMS} and nominal power output of 10 kW at switching frequencies up to 400 kHz. For an output voltage of 800 V and a power of 10 kW, the input phase current is approximately 15 A_{RMS}. For the aircraft power systems that operate off 115 V the output power is reduced to 5 kW with an output voltage of 400 V.

This paper presents the design and experimental results of a new 8.5 kW/liter (139 W/in³), forced air cooled, 3-phase, six-switch PWM Vienna Rectifier that is designed to deliver 10 kW of output power. In Section II, details on the switching devices and losses are presented, including a description of a custom power module to implement the complete six-switch Vienna Rectifier. A high bandwidth current sensor and auxiliary power supply are described in Sections III and IV. Details on the passive components, such as the boost inductors and the EMI filter, are given in Section V. The thermal design

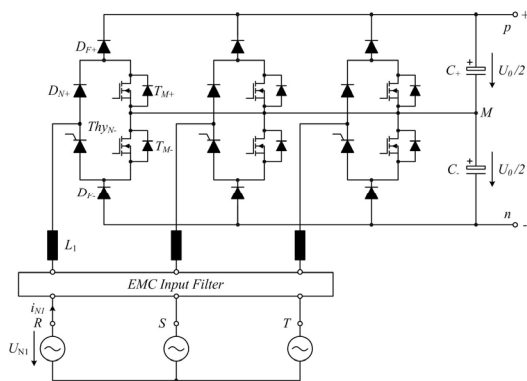


Figure 1. The 3-phase, 6-switch, 3-level Vienna Rectifier topology used to implement the 8.5 kW/liter (139 W/in³) ac-dc converter.

of the rectifier and the digital control implementation are described in Sections VI and VII. The hardware construction to achieve a power density of 8.5 kW/liter is presented in Section VIII and the experimental performance in Section IX. An initial design concept for a 2.5 MHz active rectifier is briefly presented in Section X.

II. POWER DEVICE SELECTION

For the implementation of the six-switch Vienna Rectifier switching at frequencies up to 400 kHz the selection of the optimal switch/diode combination is fundamental. Since the minimum blocking voltage of the switches is half of the output voltage (400 V for the maximum dc output voltage of 800 V), it is possible to select 600 V MOSFETs as the main switch. MOSFETs have lower losses at very high switching frequencies compared to IGBTs that are commonly used for 400V_{RMS} applications. However, the use of SiC diodes (D_{F+} and D_{F-}) operating at a 400 kHz would cause unacceptable switching losses and a major reduction in system efficiency. Therefore new SiC diodes are used since these devices have virtually no reverse recovery although they have a larger forward voltage drop.

A. Switching Loss Comparison

An air-cooled heat sink traditionally occupies a large percentage of the rectifier's total volume. To minimize the heat sink it is important to minimize the semiconductor power losses. When operating at high frequencies the switching losses can dominate. Switching loss measurements of a variety of combinations of switch and diode types have been undertaken to determine the combination that has the lowest losses and best switching performance.

Switching losses measurements of CoolMOS 600 V, 47 A C3 and CS devices, together with a 600 V, 10 A Cree SiC diodes, are undertaken in a boost circuit using the same inductor construction as in the rectifier. The output voltage is pre-charged to 400 V_{dc} and a double pulse with adjustable width is applied to the isolated gate driver in order to operate the switch at different current levels. The turn-on and off switching losses are measured using a LeCroy Waverunner LT584L (1GHz, 4GS/s) oscilloscope, through the measurement of the drain-source voltage and a time compensated, custom current sensor placed directly over the leg of the switch. This

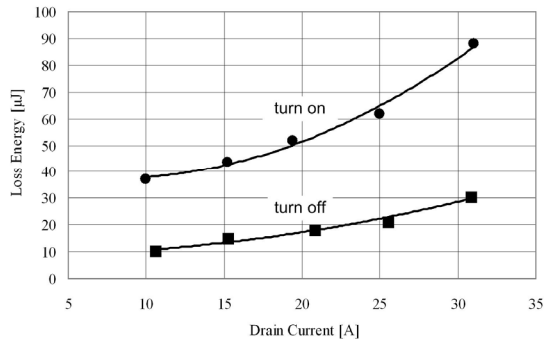


Figure 2. Loss Energy for Turn-on and Turn-off as a Function of Drain Current in Boost Circuit using Infineon CoolMOS and Cree SiC Diode.

ensures that the parasitic inductance of the switching circuit remains at a level similar to that in the final rectifier design.

Fig. 2 summarizes the turn-on and off loss measurements of an Infineon CoolMOS C3 for drain currents from 10 to 30A. Due to the measurement of the switch current in the drain leg, the current charging the junction capacitance is included in the measurements during turn off. Subtracting its influence from turn-off losses and adding it to the turn-on value results in zero turn off losses at zero drain current. By minimizing the external gate resistance and using the internal resistance of the gate driver and MOSFET gate, the switching losses can be reduced and the over-voltage limited to an acceptable level. From Fig. 2, it can be seen that the turn-on losses have the biggest contribution to the total switching losses. At a switching frequency of 400 kHz the total semiconductor power losses, including conduction and switching losses for all 3-phases, are 195 W. The switching losses make up 32% of the total overall losses.

B. Power Module Design

To minimize the volume occupied by the semiconductor, a single custom module has been produced. The module contains the semiconductors for all three phases. A photograph of the module is given in Fig. 3. The module layout has specifically been designed to have low inductance, where the input current is connected to the center connectors of the module and the output DC bus connections are on the outer sides of the module. A separate Kelvin source terminal on the MOSFETs has been added to allow faster switching by reducing the impact the source current has on the gate voltage signal.

C. Gate Driver Design

Special gate driver requirements are necessary for a high switching frequency PWM rectifier system. The requirements are a short signal propagation delay-time (in the range of a few nanoseconds), good edge symmetry (low pulse width distortion), and outstanding common-mode transient immunity. The general schematic of the gate driver is shown in Fig. 4 and consists of a signal isolator, gate driver IC and an isolated power supply.

Due to the high dv/dt-rate of up to 50 kV/µs in conjunction with unavoidable parasitic capacitive coupling (a few pF) leads to large common mode noise currents, which can distort the signal electronics of the gate driver. Therefore, a signal coupler

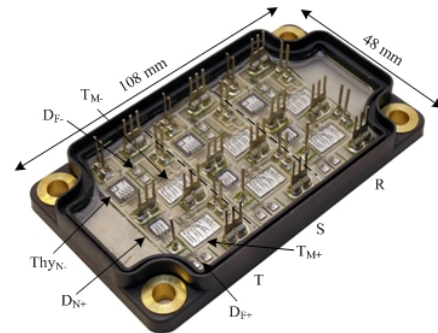


Figure 3. Custom Rectifier Power Module containing all Three Phase Legs.

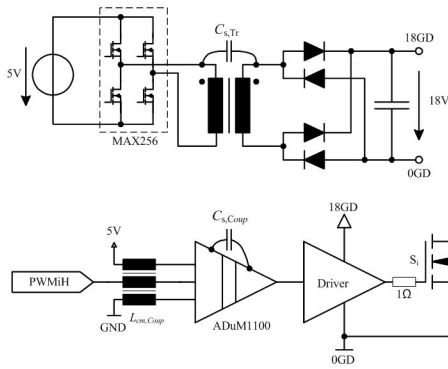


Figure 4. Gate Drive Isolated Power Supply and Gate Drive Circuit with Coupling Capacitance indicated.

needs to have a very low parasitic capacitive coupling and a high common mode transient immunity. The maximum voltage between the control electronics and MOSFET switch is half of the rectifier output voltage (400 V). If over-voltages are considered, then the coupler should have a transient rating of at least 500 V. The integrated magnetic coupler, ADuM1100 [9], comes in a small package and offers a short propagation delay-time of typically 10 ns. This device offers a specified common mode transient immunity of 35 kV/ μ s at an admissible transient magnitude of greater than 500 V. The parasitic capacitance of the magnetic coupler is given as 1 pF. In order to limit the amplitude of common-mode noise currents when switching, an additional common-mode inductor is used on the control electronics side.

The requirements for the gate driver are a small output-impedance, a large current capability and a low signal propagation delay-time. The driver has to be able to drive the relatively large CoolMOS gate-charge of 286 nC at a high switching frequency. The high-speed, high current gate drive IXDN414YI from IXYS [10] is selected for driving the gate of the MOSFET. A series gate resistance of 1 ohm is used. A unipolar supply voltage for the gate driver was selected, in order to keep the complexity, the required PCB board space and the costs low.

The isolated power supply for the gate drive is constructed using a classic dc-dc converter with a HF transformer. To minimize the size a Maxim MAX256 H-bridge driver IC together with a small toroidal transformer based on a EPCOS R6.3 core with a 10:38 turns ratio is used. The bridge chip is supplied with 5V and is switched at 600 kHz and 18 V is generated for the switching of the CoolMOS gate.

III. CURRENT SENSING

In order to control the rectifier, low volume, high bandwidth, noise-immune current sensors are required. Anisotropic magneto-resistive current sensors, which have been commercially available for several years, are highly attractive for integration into power electronics systems and modules. However, the bandwidth is typically limited to 100 kHz, although a frequency limit of about 1 MHz is stated for the magneto-resistive sensing element. A commercial Sensitac

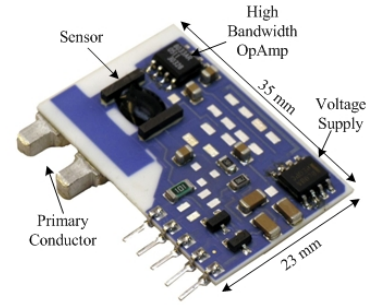


Figure 5. Magneto-resistive Current Sensor with 1MHz Bandwidth.

current sensor, depicted in Fig. 5, has been modified and a frequency bandwidth of approximately 1 MHz, which was verified experimentally in [11], has been obtained. It also has been shown experimentally that the sensor has a low susceptibility if subjected to high dv/dt rates of the primary conductor.

IV. AUXILIARY POWER SUPPLY

The auxiliary power supply is an important part of the rectifier design as it must supply all the gate drive and control electronics power. To achieve a high power density for the rectifier the auxiliary power supply must not be overlooked. A compact 45 W auxiliary power supply based on a two switch forward converter design switching at 200 kHz and this is followed by two separate 400 kHz switching voltage. It can operate from a wide three-phase voltage input (180 to 530V rms) and produces 5 V at 4 A, 12 V at 2 A and -12 V at 0.2 A with efficiency of 80%. The physical dimensions are 118x40x40 mm and the power supply layout is shown in Fig. 6.

V. PASSIVE COMPONENTS

A. Boost Inductors

The high switching frequency of 400 kHz allows the boost inductor value to be reduced to 32 μ H, while still maintaining a maximum ripple current of 10% at the specified output power of 10 kW. The boost inductor is designed as a pair of 16 μ H inductors connected in series, thus giving the desired overall inductance. Each inductor pair is constructed from two planar EPCOS ELIP N87 cores, since these cores offer a low profile and a good high frequency performance (e.g. low losses, permeability). This series connection is selected in order to efficiently fill the converter volume. Each boost inductor has 6 turns manufactured out of a copper strip with dimensions of 3 mm x 0.8 mm. This winding construction is used in order to

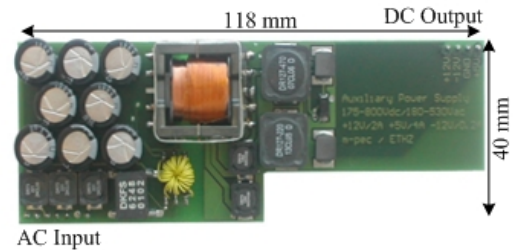


Figure 6. 45W Two-switch Forward Auxiliary Power Supply.

minimize the parasitic parallel capacitance. The capacitance is then limited to 10 pF, which still results in a capacitive current of 0.5 A for a voltage change rate of 50 kV/us. The core and winding losses are predicted, where the core losses are minimal at 0.09 W compared to 1.14 W for the copper losses (including DC and skin effect losses).

B. Capacitors

The dc link capacitors are typically used to reduce the output voltage ripple and to provide energy storage. The majority of the output capacitance is provided by low profile Panasonic 4.7μF 450V SMD electrolytic capacitors mounted near the output of the converter. This results in a dc output capacitance for the 800 V bus of 26μF. Since the rectifier is operated at a high switching frequency, it is important to minimize the inductance between the boost diodes and the output capacitors. Therefore an additional set of ceramic capacitors placed on a separate PCB that is directly mounted on the top of the module. Ideally some of these should be placed in the module, however this causes reliability problems. The capacitors are AVX 220nF 630V 2225 SMD type and a total of 5.5μF capacitance is placed directly on the module pins. This helps to reduce the drain-source voltage ringing of the switches. The overall dc output capacitance is 33μF (800 V).

C. EMI Filter

In order to meet compliance with the CISPR 22 class B conducted emission limits a volume optimized EMI filter is designed. The filter comprises of differential (DM) and common mode (CM) stages. The filter design and the subsequent optimization are based on the method introduced in [14]. An optimal design of the filters requires knowledge of the estimated emission levels. The attenuation required for the filters is derived through post processing of the equivalent voltage waveforms obtained by circuit simulations with a mathematical description of a quasi peak detector, which is used in measurement receivers during EMC compliance measurements.

In order to achieve the smallest possible volume for the DM filter, a numerical procedure minimizing the total volume is implemented. An automatic calculation of the relevant parameters for inductors and capacitors based on their datasheet values is implemented in the optimization.

Combining the component parameters with constraints, such as required attenuation at switching frequency, into a procedure, the first order parasitic components of inductors and capacitors can be automatically calculated including their dependency with frequency. These parameters are used to calculate the attenuation of a filter for a given circuit topology. For the case at hand, the DM filter is designed as a three stage LC filter. As a result of the optimization of the 3 stage DM filter topology the smallest total inductance and capacitance values are achieved if their values are the same for each filter stage.

The CM filter design procedure determines the required attenuation from circuit simulation results. Since the CM source impedance is not well defined it was set to a maximum of 10nF, including the sum of all capacitances from the power module to earth via the heat sink and from load to earth. The total CM filter capacitance per phase should not exceed 44 nF in order to ensure less than 3.5 mA of earth leakage current at mains frequency. The same approach as for the DM filter is used, which leads to a three stage CM filter. For a sensible reduction of the required attenuation the strategy of connecting the output of the rectifier to a star point of the input DM capacitors was applied. Damping resistors are included into the design in order to prevent oscillations at the resonance frequencies.

The complete filter structure including DM and CM stage and the equivalent values for the components is shown in Fig. 7. The filters are designed for a high degree of compactness by using low profile components while keeping a good high frequency performance. The magnetic materials, VAC Vitroperm500F for the CM and Magnetics Molypermalloy for the DM, are known to present the smallest volume for a given inductance for their class of power filtering, while being highly thermally stable. The capacitor values were changed slightly due to the availability of standard values for the SMD capacitors and the necessity of including passive damping in the last DM filter stage, in order to have a stable current controller over a wide bandwidth.

VI. OPTIMIZED HEAT SINK

From the total semiconductor power losses and the physical module size the heat sink design is undertaken. The total semiconductor power loss is 195 W and it is assumed that the

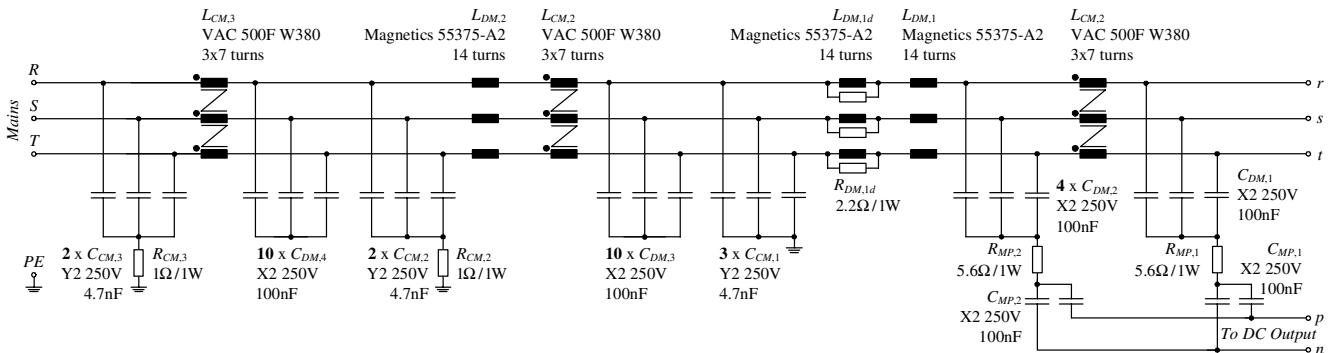


Figure 7. Final EMI Filter Structure including Differential and Common Mode Stages, Connection of Start Point and additional Damping.

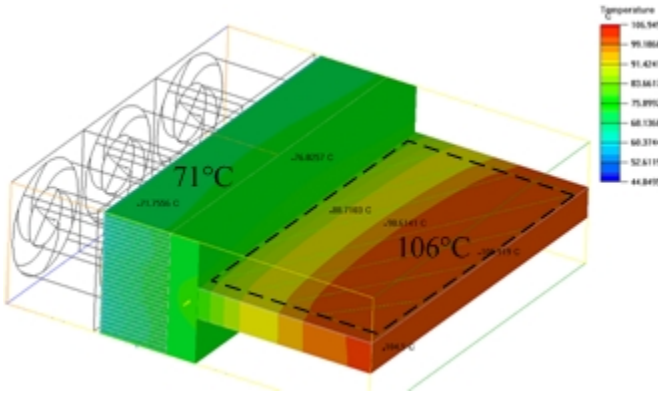


Figure 8. Finite Element Simulation Result for Optimized Heat sink, assuming 195W of power loss in the module and an ambient temperature of 45°C.

rectifier is operated at a maximum ambient temperature of 45 °C. Alternative heat sink shapes for the air-cooled system were considered in order to produce the smallest volume, while still keeping the maximum junction temperature under 125 °C. The selected heat sink design, shown in Fig. 8, occupies a small volume and has a maximum surface temperature of 107 °C. The power module is mounted in the middle of the top flat plat. The number of fins, the fin thickness and spacing have been optimally calculated [12] and then confirmed by 3-D finite element simulation (Fig. 8). The design uses three high speed, high pressure San Ace fans to force the air over the fins and then out both sides of the heat sink. A partition in the middle of the heat sink helps ensure an even flow of air out both of the sides. The heat sink is constructed from a block of aluminum and the fins are formed using spark erosion due to their small 0.75 mm thickness and spacing of 0.75 mm.

VII. CONTROL

A. Average Current Mode Control

The control of the high frequency rectifier system is based on average current mode control implemented in a purely digital controller. The controller structure consists of a cascaded controller with the current controller in the inner loop and a voltage controller in the outer loop. Due to the connection of the load to the full output voltage an additional symmetry controller is used to balance the voltage between the output capacitors. The average phase current is obtained by sampling the current sensor signal at the switching frequency. The current controller is executed at half the switching frequency (5 μ s), and takes approximately 1 μ s to be fully processed. The output voltage controller runs every 320 μ s and an additional feed forward control variable based on the mains input voltages is added into the current controller.

B. Digital Implementation

The design of the controller is an equally important issue due to the high switching frequency. The controller is implemented in a high-speed digital processor that samples the analog signals, calculates the controls and generates the PWM switch signals. To successfully implement a fully digital controller requires a very-fast processor and a dedicated control board

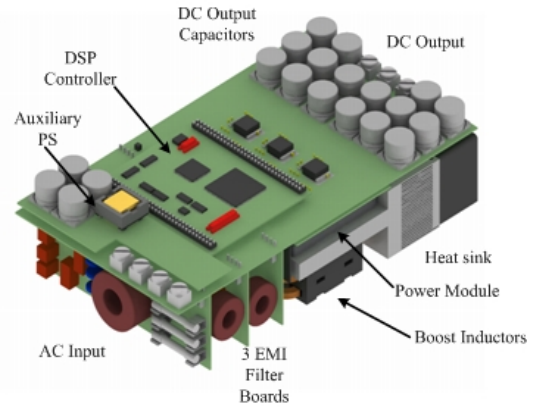


Figure 9. 3D CAD Drawing of Ultra Compact Rectifier.

has been designed based on an Analog Devices ADSP2199x DSP. This DSP has an 80 MHz internal clock, which limited the 400 kHz PWM resolution to 6.8 bits.

The rectifier control algorithms are implemented using Analog Devices' assembler language to ensure the minimum processing time. The different timing control loops of the controller are implemented by using interrupts.

VIII. HARDWARE CONSTRUCTION

A. Layout Concept

The layout concept of the rectifier depends heavily on the previous choices of power module, ceramic capacitor board, cooling system and EMI filter design. In order to have the fastest possible switching the gate driver circuits are placed directly on top of the module on an interconnecting power board. As the switching loss measurements show, the layout of the gate driver circuit is crucial in order to achieve a low loop inductance. The DSP board is placed as closed as possible to the gate drive circuits in order to reduce signal run times and effective loop inductance. The width of the system is given by dimensions of the three 40 mm x 40 mm heat sink cooling fans. Additionally the height should not exceed the standard 1U dimension.

B. Trade-off between cooling and electrical aspects

A 3-D CAD representation of the final rectifier is shown in Fig. 9. As it can be seen, the input EMI filter occupies approx 30% of the volume, while the cooling system occupies an additional 30%. The boost inductors, power module and interconnection and control boards occupy the remaining volume. The 4-layer main PCB carries the current from the input terminals, through the EMI filter boards and current sensors to the boost inductors and the power module. Ceramic output capacitors are mounted on a separate PCB that is placed directly on top of the power module. This minimizes the output inductance between the boost diodes and the output capacitors. Additionally, electrolytic SMD output dc capacitors are mounted on top of the main PCB. The gate drivers for the six MOSFETs and three thyristors are mounted underneath the digital controller board. The three high-bandwidth magneto-resistive current sensors are placed vertically between the boost

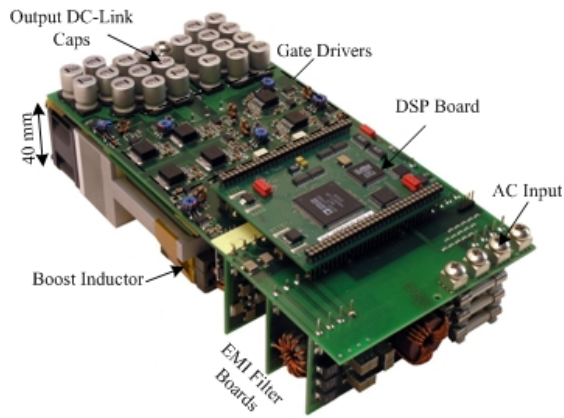


Figure 10. Top View on Rectifier with three EMI Daughter boards, DSP Board, Gate Drivers, Electrolytic dc output Capacitors.

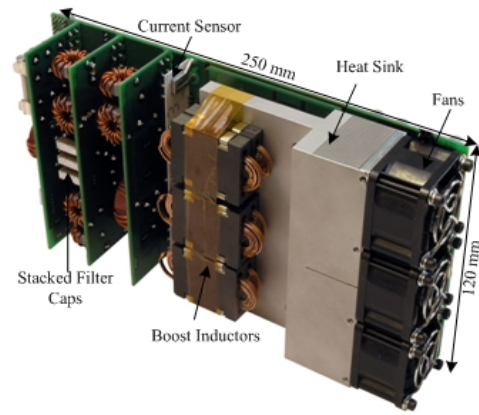


Figure 11. Bottom View on Rectifier with EMI Daughter boards, Current Sensors, Boost Inductors fixed on Heat Sink and three Fans.

inductors and the last EMI daughter board. Input and output voltage measurement circuitry is also mounted on the main PCB.

C. Final construction

Based on the results of the design process the components, such as boost inductors and EMI inductors, were constructed and compared to the design data. The top and bottom final hardware construction views are shown in Figs. 10 and 11. The design of the five rectifier PCBs (1 power PCB, 3 EMI filter PCBs and 1 ceramic capacitor PCB) was carried out, starting with the PCB having the lowest degree of freedom, which is the capacitor board since it is sitting directly on top of the power module. Since the dimensions of the capacitor board are fixed by the heat sink, as many capacitors as possible were placed on it. The EMI filter was implemented on three daughter boards, following certain design rules to reduce the interaction between the filter elements and to have a straight line forward current flow. The power board contains the gate drivers, gate drive supplies, thyristor drivers, measurement electronics and the DSP board. The current flows from the input terminals through all EMI filter boards, the current sensor and the boost inductor, which finally links it to capacitor board. From the capacitor board the current flows through the power

module directly into the output capacitors.

IX. EXPERIMENTAL PERFORMANCE

The first verification of the rectifier performance has been carried out. Fig. 12 shows the three phase input currents and one input phase voltage when the rectifier is operated with a 230 V phase voltage, a 680 V output voltage and an output power of 4 kW. The line current has a value of 5.8 A_{RMS} shows and a THD of 4.75% (up to the 20th harmonic). As can be seen in the current waveforms there is additional distortion caused at the zero crossings of the phase current. This distortion then causes distortion in the other phase currents. The controller is being refined in order to remove any sensitivity on the measurement of the phase voltage and current.

Fig. 13 shows the drain to source voltage of one of the lower CoolMOS devices at a drain current of 7 A and at a switching frequency of 360 kHz. As can be seen the output voltage rise is relatively slow and there is minimal overshoot. The turn on is much faster and there is a small amount of ringing in the voltage.

The behavior of the outer dc voltage controller can be seen in Fig. 14. In this case the rectifier is switched off and the line current is just flowing through 3-phase bridge rectifier. When the rectifier is switched on the phase currents immediately

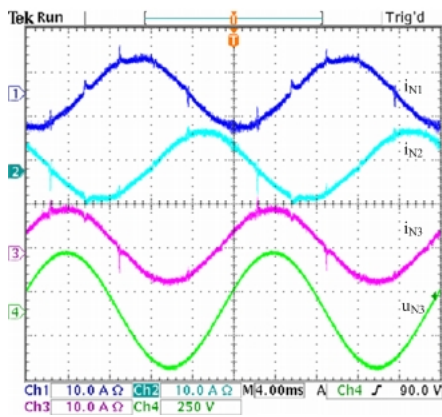


Figure 12. Current Waveforms (Ch1 – Ch3) and Phase T Input Phase Voltage at Operation of 230 V Phase Voltage and an Output Power of 4 kW.

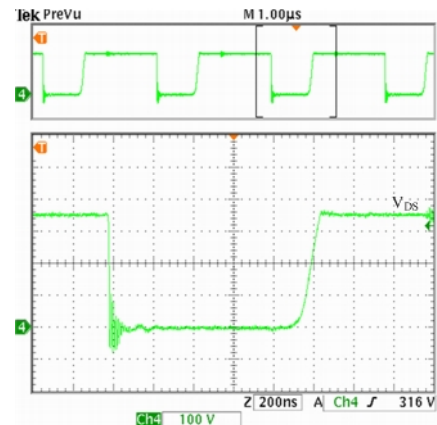


Figure 13. Switching Waveform of Drain-to-Source Voltage of Lower Switching Phase S at 5 A

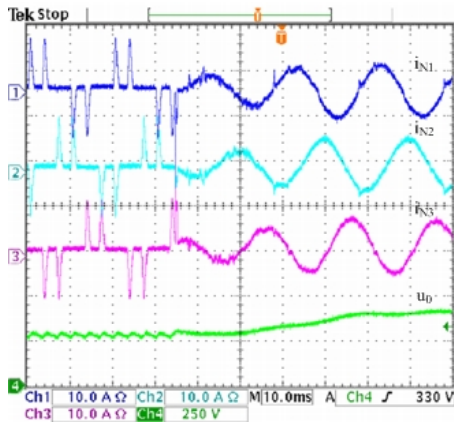


Figure 14. Input Phase Currents (Ch1 – Ch3) and Output Voltage at Transition from passive Rectification to Active Power Factor Correction.

become sinusoidal and the dc voltage begins to rise. The dc voltage has a relative slow response since the rectifier is also design to operate during a mains phase loss condition where the output voltage would then contain a large amount of 100 Hz ripple. For applications that only require operation from 3-phase mains, then the response of the dc voltage controller can be made much faster.

X. INCREASING POWER DENSITY TOWARDS 20 kW/LITER

To further increase the power density of the rectifier system towards 20 kW/liter requires significant steps to reduce the volume occupied by the EMI, since it consumes 30% of the volume. The EMI filter can be made smaller by increasing the switching frequency, although there is an increase in the switching losses. The size of the boost inductors can be reduced to a single core. A new 20 kW/liter Vienna Rectifier (Fig. 15) is in the design phase, in which the switching frequency will be increased to 2.5 MHz. At this frequency the EMI filter would be reduced to a single daughter board. The power module losses will increase by factor of three and the cooling system will be changed to a liquid cooling system. The optimized water cooler occupies the same volume as the cooling plate of the heat sink of the air-cooled system and only requires a low pressure, low flow rate pump. A new digital controller, based on a TMS320F2808, is under construction that is able to generate the modulation, with significantly higher resolution, at 2.5 MHz.

XI. CONCLUSIONS

This paper has presented the design and experimental performance of an ultra-compact, 3-phase 10kW PWM rectifier that has a power density of 8.5 kW/liter (139 W/in³). The rectifier topology is based on a 3-level, 6-switch Vienna Rectifier topology that allows the use of CoolMOS switches even when operated from a 400 V_{RMS} mains supply. The switching frequency is up to 400 kHz in order to reduce the volume of the passive components and a fully digital controller is implemented that is sampling the phase current at the switching frequency. The rectifier draws sinusoidal currents and has an efficiency of greater than 95%. An optimized forced

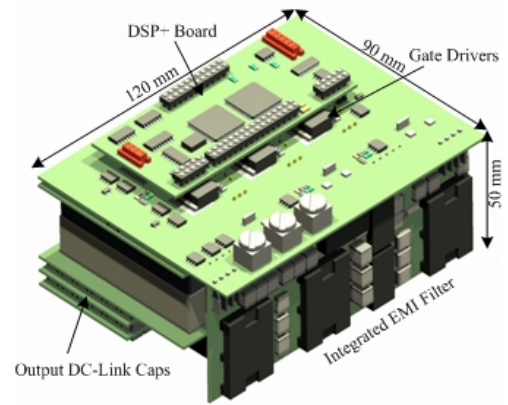


Figure 15. Layout Concept for 2.5MHz, 20 kW/liter Active Rectifier.

air-cooled heat sink and EMI filter design is implemented in order to achieve the ultra-compact design. A new design concept has been introduced that further increases the power density by increasing the switching frequency towards 2.5 MHz.

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