# 2D Materials

# Ultra-low contact resistance in graphene devices at the Dirac point

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## Abstract

Contact resistance is one of the main factors limiting performance of short-channel graphene field-effect transistors (GFETs), preventing their use in low-voltage applications. Here we investigated the contact resistance between graphene grown by chemical vapor deposition (CVD) and different metals, and found that etching holes in graphene below the contacts consistently reduced the contact resistance, down to $23\,\Omega \cdot \mu$m with Au contacts. This low contact resistance was obtained at the Dirac point of graphene, in contrast to previous studies where the lowest contact resistance was obtained at the highest carrier density in graphene (here $200\,\Omega \cdot \mu$m was obtained under such conditions). The 'holey' Au contacts were implemented in GFETs which exhibited an average transconductance of $940\,S\,m^{-1}$ at a drain bias of only $0.8\,V$ and gate length of $500\,nm$, which out-perform GFETs with conventional Au contacts.

## 1. Introduction

Large intrinsic mobility and saturation velocity of charge carriers in graphene [1] have made this material attractive for applications in high-frequency electronics in which the absence of a band gap is not detrimental to circuit operation. However, conventional ohmic contacts between graphene and various metals exhibit rather large contact resistance $R_c \sim 500\,\Omega \cdot \mu$m (normalized by the contact width $W$) which significantly reduces the apparent mobility of contacted graphene and prevents it from reaching its true potential in high-frequency applications [2, 3]. This occurs because the contact resistance is comparable to the gateable channel resistance in high-frequency short-channel graphene field-effect transistors (GFETs) and therefore suppresses transconductance and gain. Different strategies [4–11] have been adopted in order to reduce the contact resistance of graphene/metal contacts to $\sim 50\,\Omega \cdot \mu$m, which is a typical contact resistance in high-frequency transistors, e.g. InP transistors exhibiting maximum frequency of oscillation $f_{max} > 1\,THz$ [12]. In the most successful of these strategies, the contact resistance is reduced by modifying the contact area to increase

the charge injection through graphene edges at the expense of injection through the graphene surface [7, 8, 11]. Contact resistances down to $23\,\Omega \cdot \mu$m have been obtained in this way [11].

Common to all strategies used to reduce the contact resistance in graphene devices is that the lowest contact resistance is obtained at very high carrier densities in graphene [13]. At lower carrier densities, the density of states (DOS) of graphene decreases and consequently the contact resistance increases [14], typically becoming several times larger at the charge neutrality (or Dirac) point of graphene. Such behavior of the contact resistance leads to several problems in the investigation of graphene electronic devices and circuits. In graphene devices, the physical phenomena close to the Dirac point could be obscured by a very large contact resistance. In complex (i.e. realistic) graphene electronic circuits, graphene channels of unbiased GFETs should be in the charge-neutrality state to allow in/out signal matching and therefore cascading of different transistor stages [15]. However, the contact resistance has a maximum in this state which could deteriorate the performance of graphene multi-stage circuits at low voltages.

This problem could be mitigated with different doping of graphene at the contacts and in the chan-
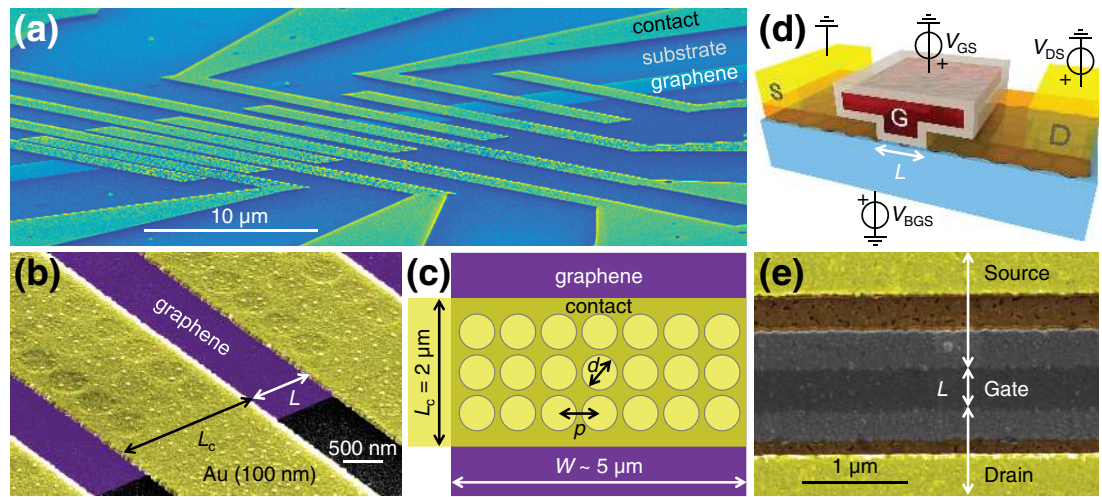
**Figure 1.** TLM devices and GFETs. (a) Scanning electron microscopy (SEM) image (in false colors) of one of the fabricated TLM devices. (b) Zoomed-in SEM image (in false colors) of a part of a TLM device with holey contacts. The holes etched in graphene are visible below Au (100 nm) contacts. The distance between the contacts is $L$ and the length of the contacts is $L_c = 2\,\mu$m. (c) Schematic of the contact layout. All holes have the same diameter $d$ and were patterned with a pitch $p$. (d) Schematic of a GFET used to test the holey contacts. Thin source (S) and drain (D) contacts (dark orange) were deposited on top of the part of the graphene channel (black) in which the holes were etched (there were no holes between the contacts). The gate (G) was made of Al (red core), which was covered by a native insulating layer of AlOx (gray shell). The thick source and drain contacts (yellow) provide a robust access to the device. The entire GFET was fabricated on a SiO$_2$ substrate (blue). Both GFETs and TLM devices were biased as indicated by the voltage generators. $V_{BGS} = 0$ V was used in GFETs while $V_{GS}$ was not used in TLM devices (they do not have a top gate). (e) SEM image (in false colors) showing the top view of the central part of one the fabricated GFETs with the gate length $L = 500$ nm. The color scheme corresponds to the schematic in (d).

nel (in addition to the already existing small doping difference caused by the metal contacts), which is typically addressed by using the back-gate to dope the contacts and the top-gate to drive the channel. However, required back-gate voltages are usually large and therefore not available in most integrated circuit technologies. They also set the channel type to the type of the contacts because the opposite type would require a very large top-gate voltage possibly causing the breakdown of the top-gate oxide. Therefore, in chips with a single (global) back gate, GFETs of only one type could be operated at the lowest contact resistance. Finally, use of any type of a back gate in high-frequency applications is prohibited because it significantly increases parasitic capacitances and therefore degrades high-frequency response of transistors.

Here we demonstrate a method for reducing the contact resistance of graphene contacts below $30\,\Omega \cdot \mu$m at the Dirac point of graphene. The method consists of etching holes in the contact area of graphene prior to deposition of metal contacts. The presence of holes increases carrier injection through the edges of holes in graphene and was found to consistently decrease the contact resistance between graphene and Au, Pd/Au, Ag, Au/Al, and Ni/Al. The lowest contact resistance at the Dirac point was obtained with pure Au contacts: $200\,\Omega \cdot \mu$m in conventional contacts (without holes) and $23\,\Omega \cdot \mu$m in holey contacts. We found that in contrast to conventional contacts, the contact resistance of holey contacts decreased as the carrier density is decreased. We also demonstrated application of this method in top-gated GFETs, finding that the average transconductance in GFETs with

holey contacts was $g_m = 940$ S m$^{-1}$ compared to $g_m \sim 600$ S m$^{-1}$ obtained in GFETs with conventional contacts, longer gates, and larger biases.

## 2. Methods

Monolayer graphene was grown by chemical vapor deposition (CVD) on Cu from CH$_4$ precursor and then transferred to highly p-doped ($>10^{19}$ cm$^{-3}$) Si substrates with a 300 nm thick top layer of SiO$_2$ by a wet process [15]. The back of the Si substrates was metallized and used as a global back-gate, if needed. The devices were entirely patterned by electron-beam (e-beam) lithography using poly(methyl methacrylate) resist. The graphene channels (width $W \sim 5\,\mu$m) and holes in channels below the contacts (in devices with holey contacts) were defined by e-beam lithography followed by reactive ion etching in oxygen plasma.

The contact resistance was investigated by the transmission line measurement (TLM) method. This method was chosen because it can extract the contact resistance from a series of scaled transistors without modifying the transistor geometry [16]. The TLM devices comprised a series of contacts separated by different channel lengths $L$, ranging from 0.3 to 4.16 $\mu$m (not the same range was used in all samples), as shown in figure 1(a). The TLM contacts were defined by e-beam lithography followed by e-beam evaporation (at a base pressure of $\sim 10^{-6}$ mbar) of a contact metal. The contacts were placed on top of the etched parts of the graphene channel in holey devices, as shown in figures 1(b) and (c). The following metals were used for the contacts: Au (100 nm thick), Pd/Au (5/95, 25/75,

and 30/15 nm), Ni/Au (15/85 nm), Ag (100 nm), Au/Al (20/40 nm), and Ni/Al (15/45 nm). Here the first metal in the stack was in contact with graphene. The entire fabrication process (apart from the holes) corresponds to that of our high-frequency GFETs [17–19], hence the contact length was fixed to $L_c = 2\,\mu$m (figure 1), the samples were not annealed (because we found that the annealing deteriorates the electrical properties of the GFETs), and we used only large-area (i.e. CVD-grown) graphene. After electrical characterizations, the exact length $L$ of each pair of the contacts and the width $W$ of the graphene channel were precisely measured by a scanning-electron microscope (SEM).

The holey contacts were also implemented in GFETs, as shown in figures 1(d) and (e). After etching the graphene channels and holes in the contact areas, thin Au contacts (13 nm) were realized by e-beam lithography and e-beam evaporation. Subsequently, the top gates were patterned by e-beam lithography followed by e-beam evaporation of 100 nm of Al. The top gates overlapped the thin Au contacts, resulting in a self-aligned T-gate structure which eliminated the access resistances (resistances of the ungated parts of the channel between the gate and source/drain contacts). Although evaporated Al initially makes an ohmic contact with Au, we found that Al at the interface with Au oxidized after a few days in air ambient resulting in an insulating contact. This required a thickness <15 nm of the thin Au contacts and small overlap between Au and Al. Similarly, a thin (∼4 nm) native layer of AlO$_x$ was formed at the surface of Al in contact with graphene [20–24] resulting in an AlO$_x$/Al gate stack with a top-gate oxide capacitance $C_{ox} = 1.37\,\mu$F cm$^{-2}$ [17, 24]. In the final step, thick Au contacts (100 nm) were fabricated by e-beam lithography on top of the thin contacts to provide reliable access to the GFETs. The GFETs had top gate length $L = 0.5\,\mu$m and the same channel width $W \sim 5\,\mu$m as the TLM devices.

The TLM devices were characterized in dc by measuring the resistances between each pair of neighboring contacts (drain and source) at different back-gate voltages $V_{BGS}$ in air ambient. The dc measurements were performed by keeping the voltage between the contacts constant, typically $V_{DS} = 10$ mV (we also performed the control measurements at $V_{DS} = 1$ mV and obtained the same results), while $V_{BGS}$ was swept in a range large enough to drive graphene from p to n type regime, as shown in figure 2(a). The back-gate sweeps revealed that the Dirac point (at which the resistance between the contacts is at a maximum) was not reached at the same $V_{BGS}$ in all pair of contacts in a single TLM device. This was caused by inhomogeneities of the CVD graphene used in device fabrication. To compensate for the inhomogeneities, the resistances between the contacts were not compared at the same $V_{BGS}$, but at the same back-gate voltage overdrive $\Delta V_{BGS} = V_{BGS} - V_{B0,i}$, i.e. at the same gate-induced carrier density $n = C_{Box}\Delta V_{BGS}/e$, as

shown in the same figure. Here, $V_{B0,i}$ is the Dirac voltage of the $i$th pair of contacts, $C_{Box} = 11.5$ nFcm$^{-2}$ is the oxide capacitance of the back-gate oxide, and $e$ is the elementary charge. To determine the contact resistance $R_c$ at a given back-gate voltage overdrive $\Delta V_{BGS}$, the resistances in a single TLM device corresponding to the selected $\Delta V_{BGS}$ were plotted as a function of the channel length $L$, as shown in figure 2(b). Assuming the resistance between the contacts $R(L) = 2R_c + R_{sh}L/W$, where $R_{sh}$ is the sheet resistance of graphene, the contact resistance can be calculated as $R_c = R(0)/2$, where $R(0)$ is the $y$-intercept of the linear fit of the discrete data set $R(L)$.

## 3. Results

The contact resistance of conventional contacts (without holes) was investigated as a reference. The contacts were made of large work function metals Au, Pd, Ni, and Ag because they were expected to provide lower contact resistance due to their smaller reactivity compared to small work function metals [25, 26]. The measured contact resistances of conventional contacts at the Dirac point are shown in figure 3. Pd has been previously found to provide some of the lowest contact resistance to graphene, in the range 69–185 $\Omega \cdot \mu$m [10, 13]. Here, Pd was used in combination with the top Au layer deposited in the same evaporation step. Au was added to reduce the series resistance of the contacts, because pure Pd resistivity is ∼4 times larger than that of Au and Al. Three different Pd/Au combinations were used: 5/95, 25/75, and 30/15 nm. We found that the contact resistance to graphene decreased as the thickness of the Pd layer was decreased. The average contact resistances were 550 $\Omega \cdot \mu$m, 490 $\Omega \cdot \mu$m, and 320 $\Omega \cdot \mu$m for the Pd thicknesses of 30, 25, and 5 nm, respectively. The slightly smaller contact resistance of the 25/75 nm stack compared to the 30/15 nm stack can be attributed to a slightly smaller lead resistance of the former stack which has thicker Au layer. However, the reduction of the contact resistance from the 25/75 nm stack to the 5/95 nm stack cannot be explained by the reduction of the lead resistance (which was negligible). Such reduction was probably a consequence of the nonuniformity of the 5 nm thick Pd layer leading to a mixed Pd and Au contact to graphene and therefore reduced contact resistance with respect to that of pure Pd contacts.

The lowest contact resistance of conventional contacts was obtained with pure Au contacts without any adhesion layer. The average contact resistance was 270 $\Omega \cdot \mu$m, excluding the three TLM devices with the contact resistance >500 $\Omega \cdot \mu$m. These three samples had much larger back-gate Dirac voltage ($V_{B0} > 100$ V) than the other investigated samples, in which $V_{B0} \sim 70$ V. Back-gating of samples with a large $V_{B0}$ was found to lead to unreliably large contact resistances because of the drift of the transfer curves at large $V_{BGS}$ [17]. To reduce the Dirac voltage, Au was also tested in combination with a top
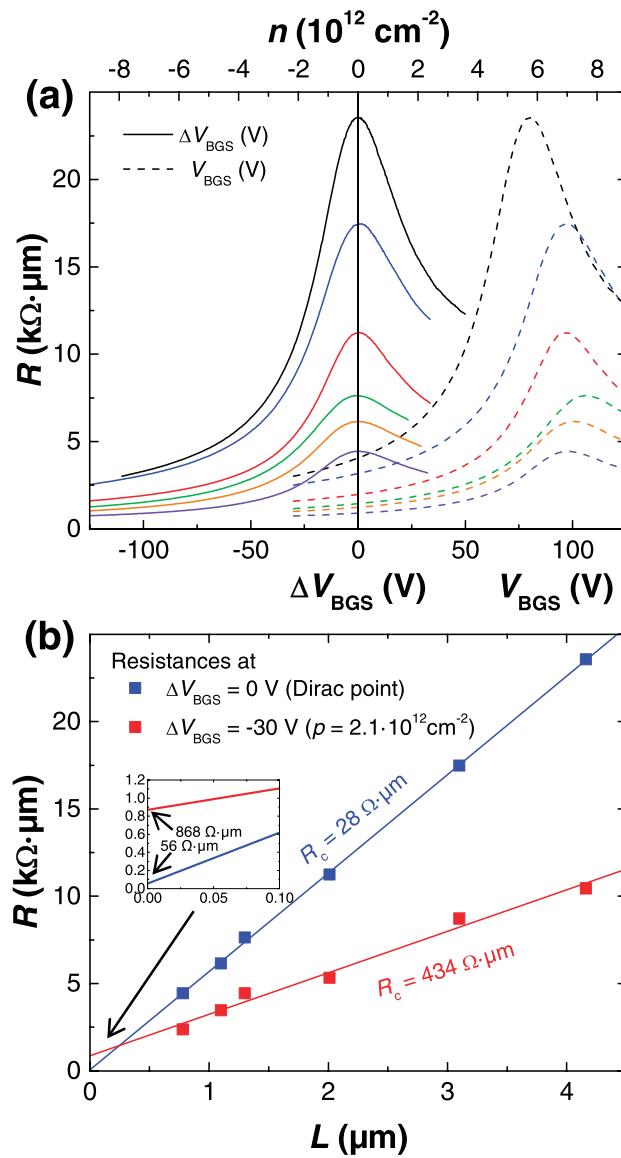
**Figure 2.** Contact resistance in TLM devices. (a) As measured resistances (the dashed lines) of 6 pair of contacts in a single TLM device biased at $V_{DS} = 10\,mV$. The resistances are normalized by the contact width $W = 4.7\,\mu m$. The channel lengths between the contacts are (from bottom to top) 0.78, 1.1, 1.3, 2.01, 3.1, and 4.16 $\mu m$. The measured resistances are also plotted (the solid lines) as a function of the back-gate voltage overdrive $\Delta V_{BGS}$, i.e. the carrier density $n$ ($n < 0$ corresponds to the hole density $p = -n > 0$). This is simply obtained by shifting each curve so that its maximum resistance is at zero voltage. (b) The measured resistance $R$ (normalized by the contact width $W$) as a function of the channel length $L$. The squares represent the data points $(L, R)$ extracted from the solid curves in (a) at two different overdrive voltages $\Delta V_{BGS} = 0\,V$ (at the Dirac point where $n = 0$; blue) and $\Delta V_{BGS} = -30\,V$ (in the hole regime with $p = 2.1 \cdot 10^{12}\,cm^{-2}$; red). The lines are the linear fits of the data points and they cross the resistance axis (magnified in the inset) at $R = 2R_c$.

Al layer, which was found to reduce the Dirac voltage in devices with Ni contacts, as discussed further below. However, although the introduction of the Al layer reduced $V_{B0}$ to $\sim$35 V, Au/Al (20/40 nm) contacts exhibited much larger contact resistance, $\sim$1150 $\Omega \cdot \mu$m in average. Au contacts have also been previously tested in combination with a thin Ti adhesion layer [17] due to the poor adhesion of pure Au to most substrates. The introduction of a thin Ti layer increased the contact resistance [17], similarly to the contact resistance of Pd/Au contacts.

Ni has also been previously found to provide a low contact resistance to graphene [9]. Similarly to Pd, it was tested here in combination with Au and Al because it has $\sim$3 times larger resistivity than Au and Al.

However, we found that the contact resistances with Ni/Au (15/85 nm) and Ni/Al (15/45 nm) contacts were 830 $\Omega \cdot \mu$m and 1490 $\Omega \cdot \mu$m, respectively, and thus much larger than that of Au and Pd/Au contacts. This could be explained by the oxidation of Ni in the e-beam evaporator as the evaporation was not performed in ultra-high vacuum [27]. The higher contact resistance of the Ni/Al contacts compared to the Ni/Au contacts was a consequence of a worse quality of graphene used in former contacts which also had an impact on the contact resistance. However, even under such conditions, holey Ni/Al contacts exhibited lower contact resistance compared to the conventional Ni/Al contacts. The investigations of TLM devices with Ni/Al contacts also showed that they
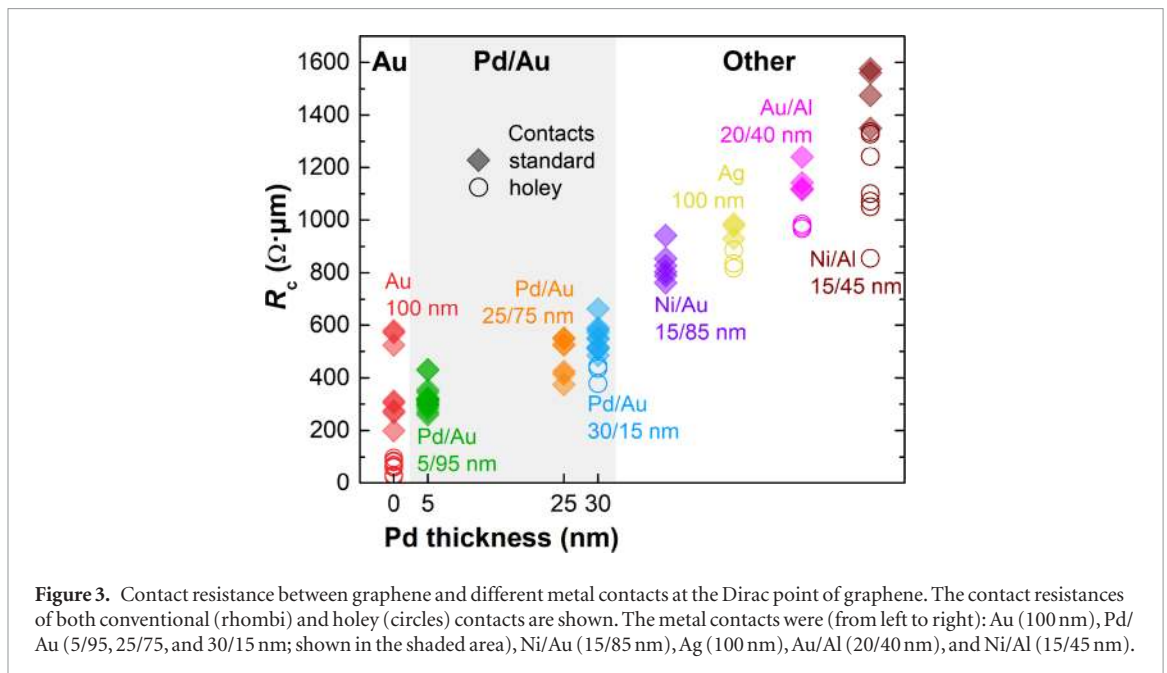
**Figure 3.** Contact resistance between graphene and different metal contacts at the Dirac point of graphene. The contact resistances of both conventional (rhombi) and holey (circles) contacts are shown. The metal contacts were (from left to right): Au (100 nm), Pd/Au (5/95, 25/75, and 30/15 nm; shown in the shaded area), Ni/Au (15/85 nm), Ag (100 nm), Au/Al (20/40 nm), and Ni/Al (15/45 nm).

exhibited n-type doping ($V_{B0} < 0$) in contrast with all other devices investigated in this work. For this reason, Au/Al (20/40 nm) contacts were also investigated, as described above.

Finally, pure Ag was tested because Ag has the lowest resistivity of all metals and therefore it is a good candidate for the contacts with the smallest series resistance. However, the average contact resistance of Ag contacts was found to be very large (in average $960\,\Omega \cdot \mu$m), thus nullifying the advantage of the low resistivity of Ag.

The holey contacts were made of the same metal combinations used to realize the standard contacts described above. The corresponding contact resistances at the Dirac point are also shown in figure 3. In all investigated cases, the holey contacts were found to decrease the contact resistance at the Dirac point due to increased charge injection through graphene edges. The lowest contact resistance at the Dirac point was obtained with pure Au holey contacts. In this case, the average contact resistance at the Dirac point was $62\,\Omega \cdot \mu$m with 30% of devices with $R_c < 30\,\Omega \cdot \mu$m. The average contact resistances at the Dirac point with Pd/Au (30/15 nm), Ag (100 nm), Au/Al (20/40 nm), and Ni/Al (15/45 nm) contacts were $420\,\Omega \cdot \mu$m, $850\,\Omega \cdot \mu$m, $980\,\Omega \cdot \mu$m, and $1140\,\Omega \cdot \mu$m respectively.

Closer investigation of the Au holey contacts showed that most of the devices with the smallest contact resistance at the Dirac point ($R_c < 30\,\Omega \cdot \mu$m) had the largest edge length to surface area ratio. This was obtained in devices in which holes with a diameter of $d = 550$ nm were spaced by 50 nm, as shown in figure 1(c). By reducing the diameter of the holes to $d = 470$ nm while keeping the pitch constant at $p = 600$ nm, the contact resistance was spread between $<30\,\Omega \cdot \mu$m and $\sim90\,\Omega \cdot \mu$m. The largest contact resistance was obtained in devices with $d = 470$ nm in which the holes were not patterned

across the entire channel, as shown in supporting figure S1 (stacks.iop.org/TDM/5/025014/mmedia).

In general, it is expected that the actual contact resistances are even smaller than those obtained here, because the measured values also included the series resistance of the leads. However, the smallest measured contact resistances also had the largest standard errors, as illustrated in supporting figure S2. There were several reasons for such large errors. In many samples large back-gate voltages were used in the measurements, which led to the drift in the measured resistances. The TLM method also assumes that all devices have the same sheet resistance $R_{sh}$ (i.e. the same charge carrier mobility) which was not always the case due to the inhomogeneity of the CVD graphene on SiO$_2$ in ambient air [19]. Finally, the contact resistance of a contact shared by two neighboring devices was not the same if two different back-gate voltages had to be applied to induce the same carrier density in the devices.

## 4. Discussion

The contact resistance of the conventional contacts was expectedly found to increase as the back-gate voltage overdrive $|\Delta V_{BGS}|$ (i.e. the carrier density) was decreased (supporting figure S3). This is a consequence of the limited DOS of graphene at the Dirac point which limits the transmission of carriers from the metal contacts to graphene below the contacts and from there to the graphene channel [14]. However, we found that the contact resistance of the holey contacts exhibited the opposite behavior. Figure 4 shows the contact resistance of the Au holey contacts to graphene, which was the smallest at the Dirac point and increased as the overdrive voltage was increased. The contact resistance of the holey contacts at the Dirac point was also smaller than the contact resistance of the corresponding standard contacts
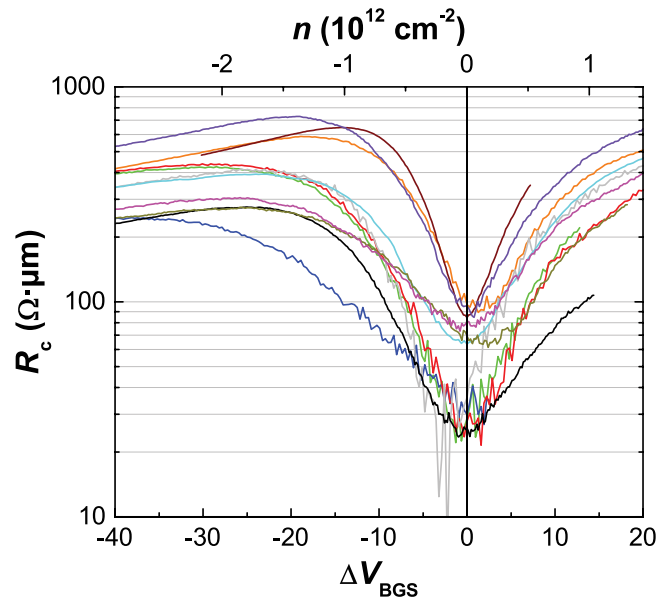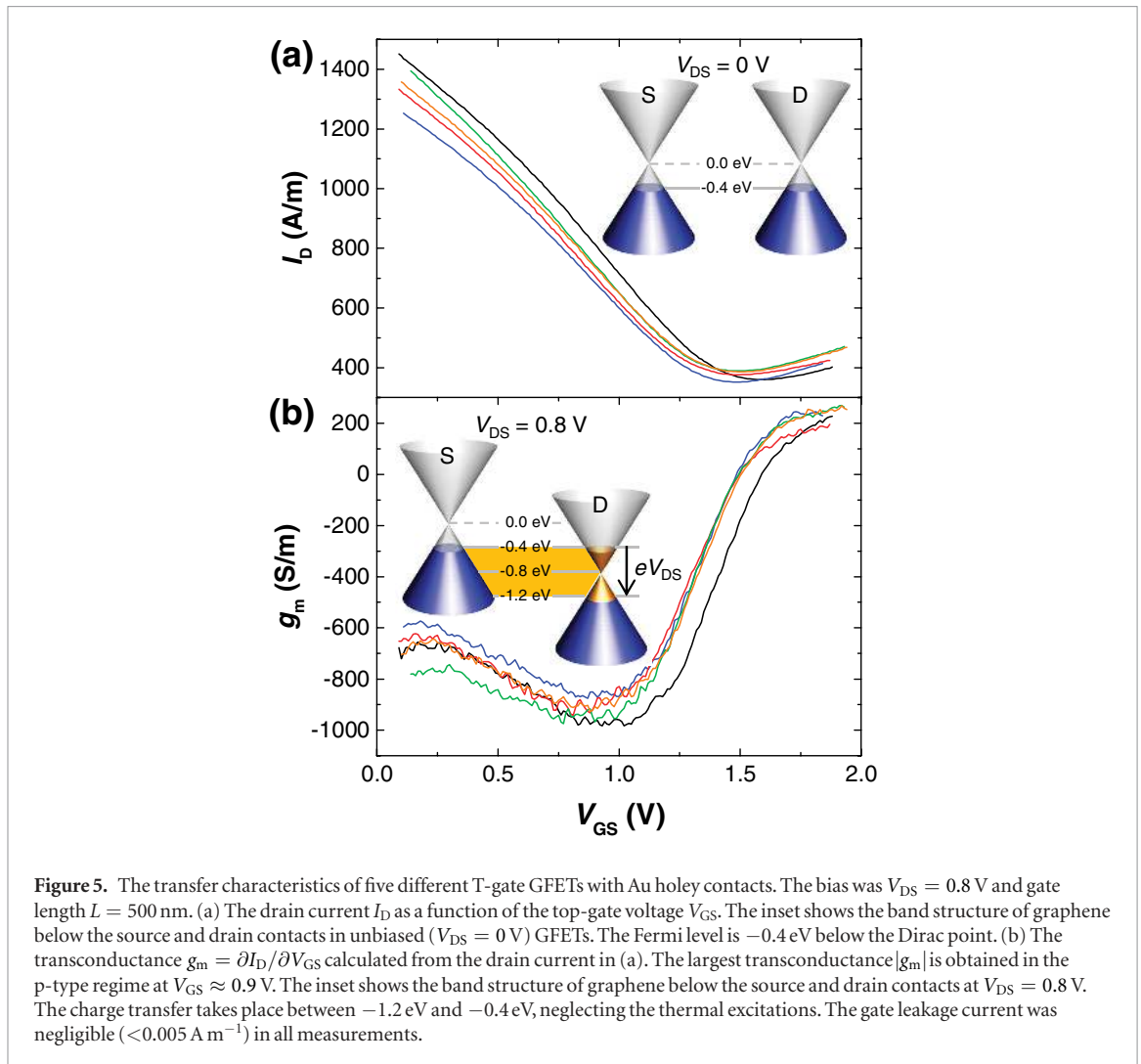
**Figure 4.** The contact resistance obtained from 11 different TLM structures with holey Au (100 nm) contacts as a function of the back-gate voltage overdrive. The bias was $V_{DS} = 10$ mV. The contact resistance in each TLM structure was determined as described in figure 2.

at any overdrive $\Delta V_{BGS}$. This indicates that the transmission of charge carriers from the metal contacts to the edge states of graphene [7, 8, 11] dominates (and therefore significantly reduces) the contact resistance of the holey contacts in the vicinity of the Dirac point. This is especially true in case of weakly interacting metals (such as Au used here) which form chemical bonds with graphene defects (i.e. edges) decreasing the contact resistance [26].

The obtained results imply that, as the overdrive voltage is increased from zero, the contact resistance of the holey contacts increases because of the suppression of the charge transfer from the metal to the graphene edges. Such behavior has not been observed in pure one-dimensional (1D) contacts in which the contact resistance decreased as the overdrive voltage was increased [8], similar to the conventional contacts. This is because the 1D contacts comprise the external edges of graphene [8] whose DOS is usually negligible at the Dirac point [28], similar to that of graphene in conventional contacts. However, our holey contacts comprise internal edges (point defects) which often exhibit a flat band, i.e. a very high (almost singular) DOS at the Dirac point [28]. Because of this, the contact resistance of the holey contacts at the Dirac point is dominated by a low contact resistance to the graphene edges and it increases as the overdrive voltage is increased due to a steep reduction of the DOS of the edges. However, as the overdrive voltage is increased even more, the contact resistance to the edges becomes very large and the decrease of the contact resistance to the unetched parts of graphene starts to dominate the overall contact resistance, which then begins to decrease as in case of the conventional contacts. This can be observed in figure 4 at larger $|\Delta V_{BGS}|$.

In order to demonstrate the advantages of the holey contacts, a series of GFETs with holey contacts was fabricated, as described in the Methods section. The unbiased ($V_{DS} \approx 0$ V) GFETs had the top-gate Dirac voltage $V_0 \approx 1.4$ V which corresponds to the Fermi level at $\approx 0.4$ eV below the Dirac point (at the hole density $p \approx 8 \cdot 10^{12}$ cm$^{-2}$), as shown in figure 5. When the GFETs were biased with $V_{DS} = 0.8$ V, the Dirac point on the drain side was lowered half way between the Fermi levels in the source and drain (figure 5). In the conduction interval ($-1.2$ eV, $-0.4$ eV) on the source side, the charge is transferred from the states far away from the Dirac point ($p > 8 \cdot 10^{12}$ cm$^{-2}$). This process is therefore dominated by the charge transfer from the unetched parts of graphene and the corresponding contact resistance is relatively low, i.e. similar to that of the conventional contacts biased far away from the Dirac point. On the drain side, the contact resistance is the smallest around the center of the conduction interval where the Dirac point is located. This resulted in even smaller contact resistance on the drain side, because the contribution of the contact resistance minimum at the Dirac point was not completely canceled out by that of the contact resistance maxima surrounding the Dirac point (figure 4). This is also evident from observing that the transconductance of the GFETs with holey contacts was larger than that of the GFETs with conventional contacts. Namely, the largest measured transconductance averaged across different GFETs with holey contacts was $|g_m| = 940$ S m$^{-1}$ (figure 5). This was measured at relatively low $V_{DS} = 0.8$ V in short-channel GFETs ($L = 500$ nm). In contrast, in GFETs with conventional contacts, but otherwise made of identical material combination, the average value was $|g_m| = 600$ S m$^{-1}$ and it

**Figure 5.** The transfer characteristics of five different T-gate GFETs with Au holey contacts. The bias was $V_{DS} = 0.8$ V and gate length $L = 500$ nm. (a) The drain current $I_D$ as a function of the top-gate voltage $V_{GS}$. The inset shows the band structure of graphene below the source and drain contacts in unbiased ($V_{DS} = 0$ V) GFETs. The Fermi level is $-0.4$ eV below the Dirac point. (b) The transconductance $g_m = \partial I_D / \partial V_{GS}$ calculated from the drain current in (a). The largest transconductance $|g_m|$ is obtained in the p-type regime at $V_{GS} \approx 0.9$ V. The inset shows the band structure of graphene below the source and drain contacts at $V_{DS} = 0.8$ V. The charge transfer takes place between $-1.2$ eV and $-0.4$ eV, neglecting the thermal excitations. The gate leakage current was negligible ($<0.005$ A m$^{-1}$) in all measurements.

was obtained at longer gate lengths ($L = 1$ $\mu$m) and larger biases ($V_{DS} \sim 1.5$ V) [17–19]. Further reduction of the gate length ($L < 1$ $\mu$m) in GFETs with conventional contacts did not result in increased transconductance which was limited by the contact resistance [19]. This result indicates that the holey contacts reduce the overall contact resistance in GFETs because a higher transconductance at lower biases and shorter gate lengths is obtained compared to that of GFETs with conventional contacts. Finally, the obtained transconductance in GFETs with holey contacts was found to be larger than that of the state-of-the-art GFETs exhibiting $f_{max} = 105$ GHz in which $|g_m| < 800$ S m$^{-1}$ was obtained at $L = 100$ nm and $V_{DS} = 1$ V [29].

In terms of the high-frequency response, we expect that the transit time in GFETs with holey contacts is similar to that of the conventional GFETs, apart from the smaller RC time constant in the holey contacts due to their smaller contact resistance. This is because only the holes near the contact edge contribute to the charge transfer (the resistance of the metal contacts is much smaller than that of the etched graphene underneath), similar to current crowding in the conventional contacts. The reduction of the contact resistance of the

holey contacts is therefore not linearly proportional to the total circumference of the etched holes because not all holes are involved in the charge transfer.

## 5. Conclusions

We investigated the contact resistance between graphene and Au, Pd/Au, Ag, Au/Al, and Ni/Al contacts, with and without holes in graphene below the contacts. We found that the contact resistance of holey contacts was smaller than that of the conventional contacts (without holes) made of the same materials. In contrast to conventional contacts, which exhibited the smallest contact resistance at the highest carrier density in graphene, the holey contacts exhibited the smallest contact resistance at the Dirac point of graphene due to the charge injection through the hole edges. The smallest contact resistance was 23 $\Omega \cdot \mu$m and it was obtained in holey Au contacts. This value was smaller than that of the conventional Au contacts at any doping level and also below 50 $\Omega \cdot \mu$m which is required for high-frequency applications. The holey contacts are expected to benefit low-voltage applications which require GFETs exhibiting high transconductance, which was confirmed here by

realizing GFETs exhibiting average transconductance $|g_\mathrm{m}| = 940$ S m$^{-1}$ at $V_\mathrm{DS} = 0.8$ V and gate length $L = 500$ nm.

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## References

[1] Yamoah M A, Yang W, Pop E and Goldhaber-Gordon D 2017 *ACS Nano* **11** 9914–9
[2] Hsu A, Wang H, Kim K K, Kong J and Palacios T 2011 *IEEE Electron Device Lett.* **32** 1008–10
[3] Watanabe E, Conwill A, Tsuya D and Koide Y 2012 *Diam. Relat. Mater.* **24** 171–4
[4] Moon J S *et al* 2012 *Appl. Phys. Lett.* **100** 203512
[5] Franklin A D, Han S-J, Bol A A and Perebeinos V 2012 *IEEE Electron Device Lett.* **33** 17–9
[6] Li W *et al* 2013 *Appl. Phys. Lett.* **102** 183110
[7] Smith J T, Franklin A D, Farmer D B and Dimitrakopoulos C D 2013 *ACS Nano* **7** 3661–7
[8] Wang L *et al* 2013 *Science* **342** 614–7
[9] Leong W S, Gong H and Thong J T L 2014 *ACS Nano* **8** 994–1001
[10] Zhong H, Zhang Z, Chen B, Xu H, Yu D, Huang L and Peng L 2015 *Nano Res.* **8** 1669–79
[11] Park H-Y *et al* 2016 *Adv. Mater.* **28** 864–70
[12] Lai R *et al* 2007 Sub 50 nm InP HEMT device with Fmax greater than 1 THz *Int. Electron Devices Meeting* pp 609–11
[13] Xia F, Perebeinos V, Lin Y-M, Wu Y and Avouris P 2011 *Nat. Nanotechnol.* **6** 179–84
[14] Nagashio K and Toriumi A 2011 *Japan. J. Appl. Phys.* **50** 070108
[15] Rizzi L G, Bianchi M, Behnam A, Carrion E, Guerriero E, Polloni L, Pop E and Sordan R 2012 *Nano Lett.* **12** 3948–53
[16] Schroder D K 2006 *Semiconductor Material and Device Characterization* (Hoboken, NJ: Wiley)
[17] Guerriero E, Polloni L, Bianchi M, Behnam A, Carrion E, Rizzi L G, Pop E and Sordan R 2013 *ACS Nano* **7** 5588–94
[18] Bianchi M, Guerriero E, Fiocco M, Alberti R, Polloni L, Behnam A, Carrion E A, Pop E and Sordan R 2015 *Nanoscale* **7** 8076–83
[19] Guerriero E *et al* 2017 *Sci. Rep.* **7** 2419
[20] Miyazaki H, Li S, Kanda A and Tsukagoshi K 2010 *Semicond. Sci. Technol.* **25** 034008
[21] Guerriero E, Polloni L, Rizzi L G, Bianchi M, Mondello G and Sordan R 2012 *Small* **8** 357–61
[22] Lu C-C, Lin Y-C, Yeh C-H, Huang J-C and Chiu P-W 2012 *ACS Nano* **6** 4469–74
[23] Yeh C-H, Lain Y-W, Chiu Y-C, Liao C-H, Moyano D R, Hsu S S H and Chiu P-W 2014 *ACS Nano* **8** 7663–70
[24] English C D, Smithe K K, Xu R and Pop E 2016 Approaching ballistic transport in monolayer MoS2 transistors with self-aligned 10 nm top gates *Int. Electron Devices Meeting (San Francisco, CA, USA)* pp 5.6.1–4
[25] Nagashio K, Nishimura T, Kita K and Toriumi A 2009 Metal/graphene contact as a performance killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance *IEEE Int. Electron Devices Meeting* pp 1–4
[26] Ma B, Gong C, Wen Y, Chen R, Cho K and Shan B 2014 *J. Appl. Phys.* **115** 183708
[27] English C D, Shine G, Dorgan V E, Saraswat K C and Pop E 2016 *Nano Lett.* **16** 3824–30
[28] Fujii S, Ziatdinov M, Ohtsuka M, Kusakabe K, Kiguchi M and Enoki T 2014 *Faraday Discuss.* **173** 173–99
[29] Feng Z, Yu C, Li J, Liu Q, He Z, Song X, Wang J and Cai S 2014 *Carbon* **75** 249–54