Ultra-low power circuits for power management

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Abstract

Recent developments in energy harvesting techniques allowed implementation of completely autonomous biosensor nodes. However, an energy harvesting device generally demands a customized power management unit (PMU) in order to provide the adequate voltage supply for the biosensor. One of the key blocks within this PMU is a regulation DC-DC converter.
In this Master Thesis, the most relevant switched-capacitor DC-DC converter topologies that are suitable for biosensors are compared. The topology that can achieve the best efficiency and has the minimum area is chosen and designed. In order to maintain the supply voltage of the biosensor constant when the input voltage and the output current vary, a traditional Pulse-Frequency-Modulation (PFM) control is employed. An ultra-low-power PFM control circuit is designed to operate in weak inversion region. The post-layout simulations show that the designed DC-DC converter can provide an output voltage of 900mV when the output current varies between 5µA and 40µA. Additionally, the post-layout simulations of the entire system, which includes the DC-DC converter and PFM control, show that the selected topology can achieve 87% peak efficiency, when the control losses are included. The main advantages of the proposed topology are its smaller chip area and its high efficiency during processing ultra-low power levels.

List of Abbreviations

ULP	Ultra-Low-Power
CR	Conversion Ratio
DVS	Dynamic Voltage Scaling
WBAN	Wireless Body Area Network
BASN	Body Area Sensors Network
WSN	Wireless Sensor Node
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
LDO	Low-DropOut
FSL	Fast Switching Limit
SSL	Slow Switching Limit
PFM	Pulse Frequency Modulation
LS	Level Shifter
VCO	Voltage Controlled Oscillator
NOC	Non-Overlapping Clock
OTA	Operational Transconductance Amplifier
SCM	Self-Cascode MOSFET
SBS	Self Biased Structure

Chapter 1

Introduction

1.1 Background

1.1.1 Low Power Design Techniques

Over the years, electronic devices experienced a gradual decrease in their size, together with a simultaneous increase of their performances. This fact has been accurately predicted by the Moore's law, which states that the performance would double every eighteen months while the size would be halved. The market has always required electronic systems with continuously reduced dimensions, such as portable devices, implantable systems, etc. Therefore, it is an immediate need to reduce the power consumption, leading to the development of ultra-low-power systems.

If the dissipated power of the circuit stays roughly the same while the size is reduced, the power dissipation per unit area increases, which could lead to a violation on the design constraints [1]. Therefore, the power dissipation must also be reduced with the size. In addition, the battery of portable devices must also be scaled, otherwise the overall effect of reduction on area of the circuit might be only marginal. Besides, using batteries for powering becomes unpractical in some applications. In these situations, energy harvesting and energy scavenging techniques can be utilized to provide power to the system (issues regarding the battery will be discussed later).

The total power in the CMOS technology is roughly equal to the sum of three components:

- the dynamic dissipated power during the charging and discharging of the (usually parasitic) capacitances,
- the power dissipated during the time when both the NMOS and the PMOS conduct

- the losses due to a non-zero current of the MOS transistors in the off-state for digital circuits or to a biasing current for analog circuits.

The power dissipation in digital circuits depends quadratically on the supply voltage. Indeed, this race against power dissipation has led to reduce gradually the supply voltage in order to minimize the energy per operation $E_{/op}$. This quantity is an important figure of merit for comparing different types of logic circuits and can be calculated as the product of the time taken by an inverter to perform a given logic operation times the power dissipated during this time within the inverter. Specifically, in the MOS technology the energy per operation is affected by two components of drain current: the active current and the leakage current. The first decreases exponentially as the voltage increases, while the second increases quadratically. This opposite trend places the minimum of the $E_{/op}$ at approximately 0.4V supply voltage[29]. Therefore, ULP (Ultra-Low-Power) circuits are designed with a low supply voltage. This also ensures a greater margin of safety from breakage of the thinner oxide (after the scaling) [2].

Furthermore, other several design techniques for ULP circuits are several, such as [2-8]:

- MOSFET operating in weak inversion region. The channel current of an NMOS transistor in weak inversion is given by:

$$I_{DS} = I_S e^{\frac{V_{GS}-V_T}{nV_t}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) \tag{1.1}$$

where $I_{D0} = 2n\mu_n C_{ox} \frac{W}{L} V_t$, while $n = 1+\frac{C_{ox}}{C_{js}} \approx 1.5$ is the slope factor. Moreover, the exponential dependence on V_{DS} can be eliminated more easily compared to the strong inversion where the current was directly proportional to V_{DS} for the effect of the channel-length modulation.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_T} \tag{1.2}$$

Another feature of the weak inversion operation is that the transconductance g_m in the weak region depends linearly on the current and no longer according to the square root.

Since the current is smaller in weak inversion, also the transconductance is smaller, then the gain is sacrificed. The advantage is that the power consumption is significatively reduced, and also by increasing the size of the transistor the reduction of the gain is avoided. For instance, in Ref. [5] it is shown that $\frac{g_{m,weak}}{g_{m,strong}} \approx 0.26$ for a NMOS transistor in 0.13μm technology with a V_T equal to 0.4V.

This technique will be explained in detail in section 4.2, because it is used widely in this master thesis.

- Bulk-driven transistor. The MOS is biased in saturation mode while the input signal drives the bulk terminal, removing the threshold voltage requirement from the signal path. Therefore, the transistor operates as a depletion type device. However,

the small signal transconductance of a bulk-driven MOSFET is about 30% of a MOSFET controlled by the gate, and the bulk-driven MOSFETs need to be fabricated in a different well (worse matching between devices).

- Self-cascode structure. Due to the technological shrink, which increase the effect of the channel length modulation, the output resistance of the MOSFET becomes smaller. Therefore, to obtain high gains, a cascode structure should be used, although it cannot be used in ULP applications. The self-cascode structure has the same advantages as the cascode structure while the output voltage is comparable to a non-cascode structure.
- Level shifter techniques. MOS Transistors are operating in saturation or in sub-threshold region in order to achieve a rail-to-rail swing both at the input and the output.
- Floating Gate techniques. Floating gate Transistors are used for EPROM and EEPROM memories but, also as circuit elements.

In addition, the decrease of the supply voltage leads to the deterioration of the drive strength because reductions in the threshold voltage are limited by the noise margin (lower VT leads to a lower SNR) [2].
The majority of digital circuits does not need to operate always at maximum speed. This is the reason why the dynamic voltage scaling (DVS) and Ultra Dinamyc Voltage Scaling (U-DVS) are applied to reduce the power consumption in digital circuits. DVS is a technique based on the idea that the circuits do not always need the best performance. Using this technique, the supply voltage is not constant but increases or decreases according to the current needs.

1.1.2 Implantable Systems and Biosensors

The technological development has led to the extensive research on new monitoring techniques for medical purposes, in particular, for the implantable systems. These techniques should be minimal invasive, should have a reduced occupied area and a small weight.
The Wireless Body Area Network (WBAN), which offers a good opportunity for remote health monitoring [9-14], is a network of many in-body or on-body connected wireless sensor nodes, called Body Area Sensors Network (BANS). It monitors human body for medical purposes, while the transceivers of each sensor node allow the data transfers to a hospital emergency alarming system. Moreover, a hypothetical transducer, using those information could solve any health problem independently.

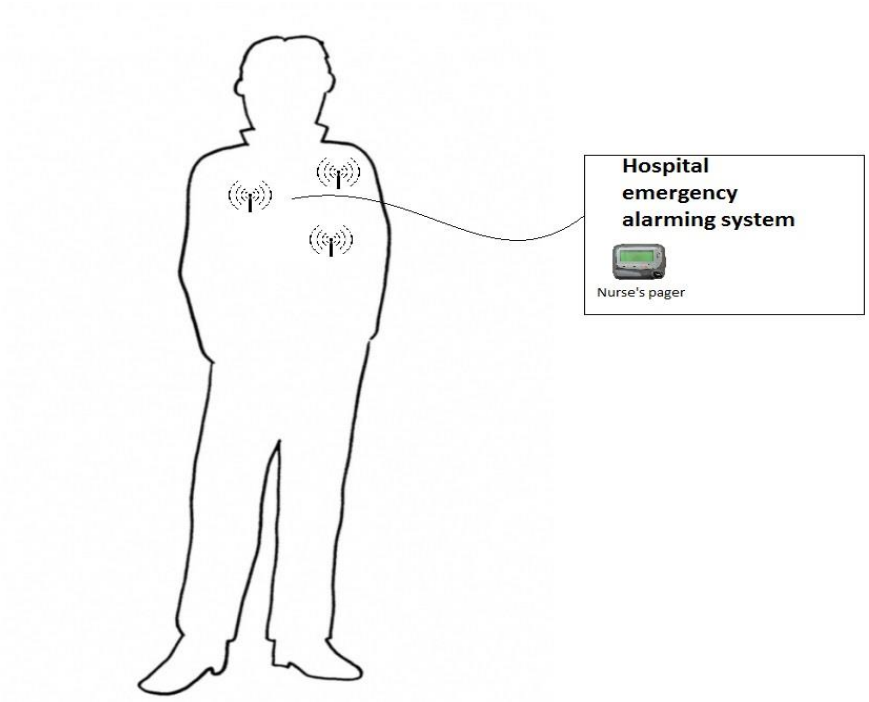

Figure 1.1: Implantable system for health monitoring

In particular, the WBANs have been originally developed for a wide range of applications including entertainment, interactive video-games, for military applications, sport-related devices and then, it found very broad use in the medical field.
Each BANS can provide useful information like ECG (electrocardiogram), EEG (electroencephalogram), glucose level in the blood, etc.. BANSs have a similar structure to the WSNs (wireless sensor node) and can be divided into three classes:

- Ambient sensors, measuring the environment behaviors. The sensors of light, sound, humidity, temperature and similar belong to this class.
- Physiological sensors, which measure body behavior. The glucose monitoring sensors for diabetic patient, blood pressure and other belong to this class.
- Biokinetic sensors, such as accelerometer, gyroscope, which measure body movement and position, or angular position.

A WBAN always contains a block for transmission of the measured data and it may, also, contain a block of signal processing. A signal processing block adds more complexity to the system but it is useful to reduce the amount of information, which must be transmitted, without altering the fidelity of the information. A reduction of the data-rate determines a reduction also in power consumption. In the work [12], the average power dissipated by a WBAN (for various communication protocols) varies depending on the traffic information. It can reach a few hundred of microWatt if the information traffic is heavy, while at rest does not exceed 1μW. For instance, the WBAN, presented in [11], has a CDT (Continuous data transmission) protocol, in UMC 0.18μm 1P6M CMOS technology, it occupies an overall area of 1.5mmx0.95mm and it is powered by 1.5V. The clock frequency is set to 20MHz during data transmission with duty cycle of 1.7%. In these conditions it consumes an average power of 2.1 μW.

The WBANs must be minimally invasive, therefore, they must be smaller, because they are inside or over the human body, and very efficient. As explained in the previous chapter, the energy saving is the most important issue for WBANs, and, in general, for all the implantable devices.

1.1.3 Energy Harvesting

As the size and the weight of the WBAN sensor node, the size and weight of the battery should be also scaled down. Nevertheless, it is currently a rather underdeveloped part of the system. One of the most popular batteries in portable devices is the Li-ion based battery, which has a volumetric energy density of 300-500 W/l. Scaling down the dimensions of the battery the stored energy, and so the battery lifetime, decreases. Moreover, the lifetime of the battery is another critical parameter of implantable systems, it must be as long as possible, because the replacement of the battery require a surgery. Lately, elegant solutions have been developed to avoid the replacement of the battery such as ways to recharge the battery or battery-free systems. On the other hand, the biosensor node still needs energy to operate and this energy could be supplied by an energy harvester. Thus, it is possible to take out the battery and replace it with an energy harvester and an energy storage.
The energy harvester is a device, which is able to collect and convert the energy present in the environment, such as the temperature difference into electrical energy that will be stored in the energy storage element and used to power the circuits.
From the human body you can extract, in fact, some amount of energy in the form of:

- Kinetic energy. The movement of the human body produces kinetic energy that could be collected by vibration energy harvesters. There are three mechanism to convert kinetic energy to electrical energy: electro-magnetic, electrostatic and piezoelectric.
- Thermal energy. In particular, the human body tends to maintain an internal temperature around 36 ° C. A temperature difference could provide a voltage difference thanks to a thermocouple.
- RF Energy. By using of inductors, coils and transformers it is possible to exploit the available environmental RF energy, which is very low. In the same way it can provide power using an artificial RF source with a remote powering. This cannot be considered an energy harvester, but it can be very useful for an implantable medical device because it is possible recharge the battery without operate the patient.
- Biochemical energy. The energy stored in chemical bonds can be converted into electrical energy.

In the work [15], the authors compare a kinetic energy harvester with a thermal one. It shows that, in a theoretical case, the kinetic one is more efficient both in a running patient as in a walking patient (it is obtained 300μW/cm^3 for a walking patient e 30μW/cm^3 for running patient while thermal harvester only 20μW/cm^3 e 10μW/cm^3). However, the

performances of the current implementations of the kinetic harvester are poorer than the thermal one: they achieve only 1% of the theoretical limit, compared with 70% in the case of thermal harvester. Then it shows that for a patient walking the thermal harvester can extract more energy. In a running patient, low-volume occupied by the device, the thermal harvester remains the best, but for the high-volume kinetic harvester is the most powerful.
The thermal harvesting system bases its operation on the Seebeck effect. In the presence of a temperature gradient, the free electrons due to thermal agitation, will tend to move in a direction opposite to the temperature gradient, creating a potential difference that resists to this trend. To use this difference in potential, as known, two different materials, which form a thermocouple, are necessary (Fig. 1.2).
The corresponding voltage is given by:

$$V = S_1 \Delta T - S_2 \Delta T \tag{1.3}$$

Where S_i is the Seebeck coefficient of the material i, and it is negative for a N-type materials, in such way, for the thermocouple in figure the two terms are summed.

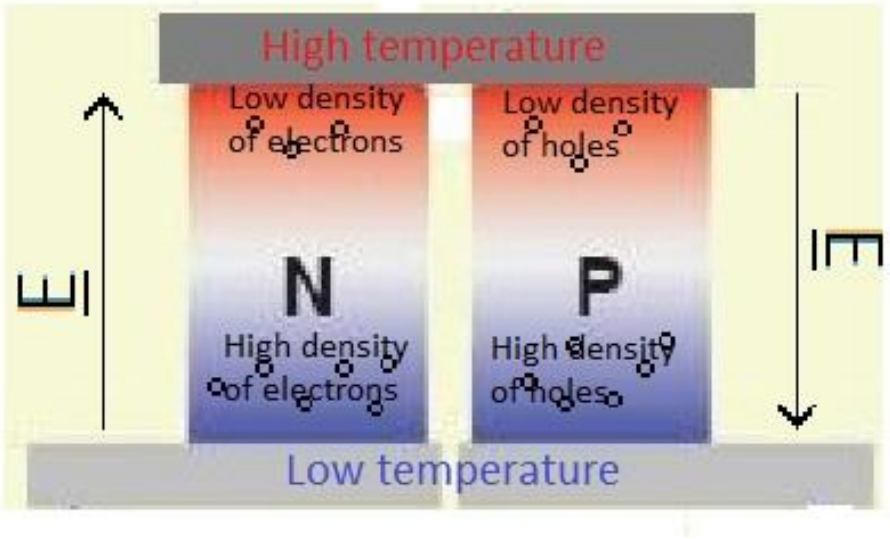

Figure 1.2: Seebeck effect

Usually the thermal harvester are made of many thermocouple. As the voltage generated between the opposite sides of the n thermocouples is Vg = (nSΔT), the available power is given by:

$$P_g = \frac{Vg^2}{4R_{gen-el}} = \frac{(nS\Delta T)^2}{4R_{gen-el}} \tag{1.4}$$

where R_{gen-el} is electrical resistence between the terminals of generator, S the Seebeck coefficient, while ΔT, which is the temperature difference between opposite sides, can be calculate by virtue of thermal model (Fig 1.3):

$$\Delta T = \frac{R_{gen-th}}{R_{gen-th}+(R_{source}+R_{sink})}(T_{body} - T_{ambient}) \quad (1.5)$$

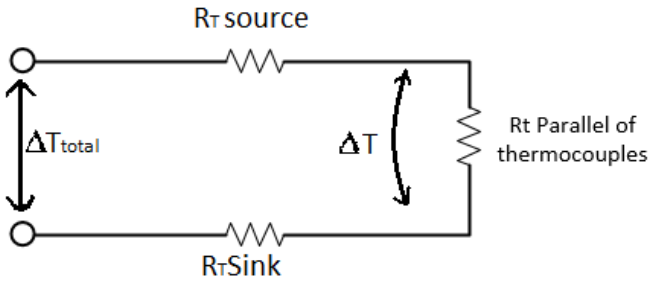

Figure 1.3: Thermal model of the system

The maximum electrical power can be achieved when R_{gen-th} is equal to the sum of parasitic thermal resistance. A problem is the placement of those energy harvesters to maximize energy production. For instance, the thermocouple is placed in proximity of the skin where the temperature gradient is higher (within 2-3 cm is present a variation of 5K). A vibration harvester is placed in an area where the kinetic energy produced is higher.
The main problem is that the energy consumed by the biosensor node must be less than that provided by the energy harvester. In other words, the charge of the storage element must be stronger than its discharge. This problem can be overcome, since two monitoring action (or other possible action for some systems implantable medical) may be interspersed with a long idle time.
Reasoning with average powers:

$$P_{av,gen} \geq P_{av,dis} \quad (1.6)$$

Where $P_{av,gen}$ is the average power provided by the energy harvester and $P_{av,dis}$ is the average power consumed by the biosensor.
In general, if you want to relax on the specific powers you can increase the time between two measurements. In fact, the biosensor is not always consuming its maximum power P_{active}, but only for a small percentage D (duty cycle) of its cycle T. Thus, the average power dissipated is equal to:

$$P_{av,dis} = (1 - D)P_{idle} + D \cdot P_{active} \quad (1.7)$$

Hence, to satisfy the formula (1.6):

$$D \leq \frac{P_g - P_{idle}}{P_{active} - P_{idle}} \quad (1.8)$$

The figure 1.4 shows that, during the idle state, the energy is stored by the storage element, while during the active state, the energy transferred to the biosensor prevails, but the average harvested energy is still greater than the average consumed energy.

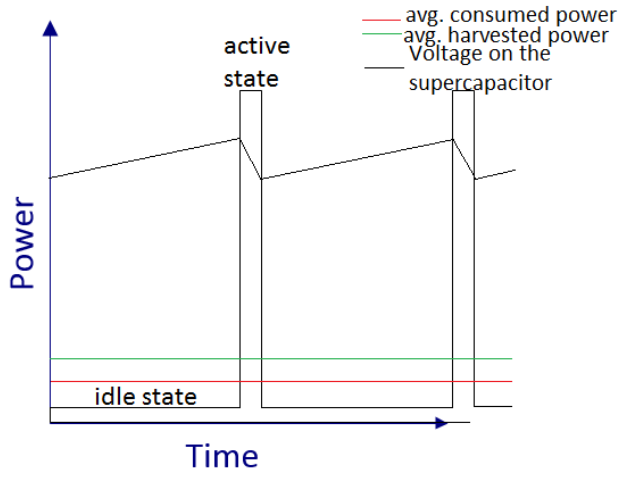

Figure 1.4: Operation mode of the system

It is also need a storage element that allows to store the energy harvested, in fact, it is not constant and, sometimes, may not be enough to power the system. Possible candidates are the thin film batteries, rechargeable batteries and supercapacitors.

1.2 Power Management System

The energy derived from transducer must be maximized. The biasing point of the load and the environmental conditions affect the harvested power from the transducer, therefore, the load of the transducer must be biased in such a way that it is maximized. This operating point is called maximum power point (MPP). Recent researches [31] have developed many algorithms for MPP tracking (MPPT). We briefly describe the most relevant:

- Voltage-based MPPT. The biasing point of the load has a constant voltage, which is a portion of the maximum voltage(the open circuit voltage V_{OC} of the transducer)

$$V_{MPP} = K_V V_{OC} \tag{1.9}$$

- Current based MPPT. The load drains a constant current, which is a portion of the maximum current (the short circuit current I_{SC} of the transducer)

$$I_{MPP} = K_I I_{SC} \tag{1.10}$$

- Perturbation and Observation. The operating point, as shown in the figure 1.5, is perturbed continuously, in the direction of the gradient of the power

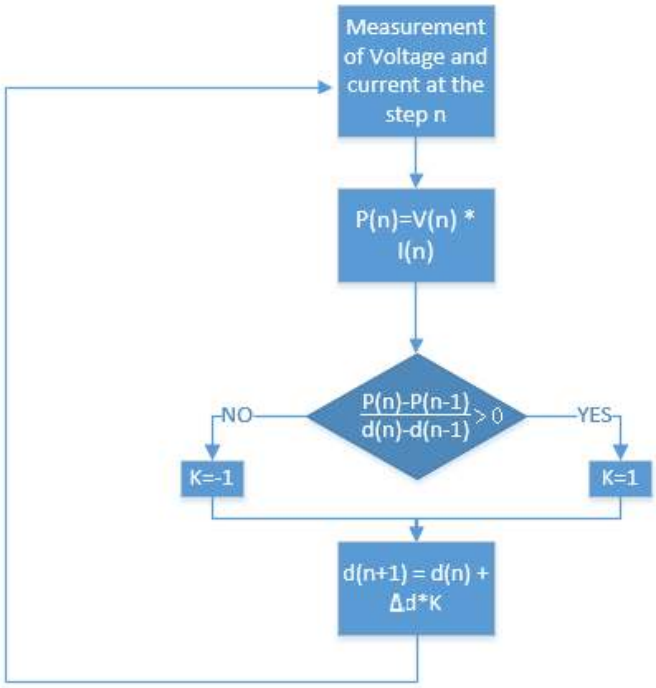

Figure 1.5: Perturbation and Observation Algorithm

The voltage from the thermal harvester is very small (50÷75mV) [28], noisy and dependent on the MPPT. For all of these reasons it is not suitable to feed any circuit, analog or digital, present in the WBAN node, but it needs to be changed by means a Power Management units (PMU) in figure 1.6.
The first DC-DC converter serves as an appropriate load for the transducer, and so, it allows to extract the maximum power from the environment, as in the [30]. Then, as discussed above, the energy is stored in a storage element. Since the voltage on that storage element is different from the required one, a second DC-DC converter is necessary to provide the right supply voltage for the load.
However, the voltage across this super-capacitor varies depending on the power available from the energy harvesters and power consumed by the biosensor node. As shown in fig. 1.5, the super-capacitor C is charged when the biosensor node is in idle state and is discharged during the biosensor operations. In this system, the voltage drop V_{STORE} on the supercapacitor varies between 1.8V and 2V. Therefore the second converter should also solve this problem.
The diagram of the complete system is shown in figure 1.6.
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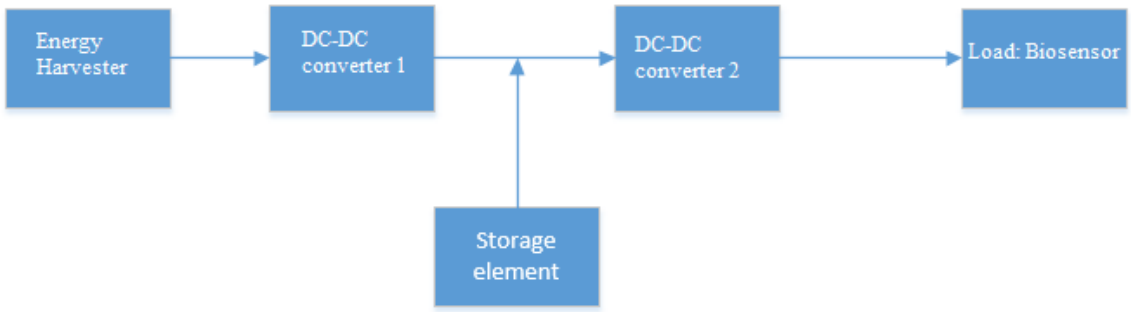

Figure 1.6: PMU for energy harvesting system

1.3 Thesis Goal

For the biosensor node two voltages are required:

- A voltage of 1.8 V for powering analog circuits, which must be stable and noise free.
- A voltage of 1 V, for powering digital circuits, which can be noisy

The present Master thesis focuses on the design of a part of the PMU discussed in the previous section and shown in figure 1.6. In particular, we investigate and design an efficient voltage regulation circuit to supply the digital circuits of the biosensor node from the super-capacitor. Aiming at this goal, we explore different solutions determining their advantages and disadvantages.

Particular care has to be provided in order to satisfy the equation (1.6) without increasing the duration of the idle mode. Therefore, the efficiency of the circuit remains a key parameter. Since the design is ultra-low power, transistors operating in subthreshold region will be used. Moreover, since the system must be implantable, the overall area is also important, so, the best trade-off between size and performance should be found.

In integrated circuits, where the use of inductor switching DC-DC converter is not allowed because of their excessive area occupied, switched-capacitor DC-DC converter could be suitable. Effectively, their occupied area is not limited by the presence of inductors, however, it can reach an efficiency (>80%) [27] not comparable to that of switched-inductor (≈ 97-99%), but higher than voltage-regulator. Moreover, contrary to the LDO, its efficiency remains high even if the required output voltage is distant to the input voltage. This is one of the reasons that make SC DC-DC converter more suitable than LDO regulators to supply the analog circuits of the biosensor node, which requires a voltage of 1V, too distant to the input voltage (1.8-2V).

1.4 Thesis Organization

In the chapter II we present an overview of the switched capacitor DC-DC converters, their advantages and disadvantages and their theoretical model. Then, in chapter III we analyze various topologies of switched-capacitor DC-DC converters, both theoretically and numerically using the commercial tool Cadence. At the end of this chapter, we choose the most suitable topology to supply the digital part of the biosensor. Then, in chapter IV we investigate the control circuits needed to provide an output voltage regulation. In the chapter V we present the layout design and post layout simulations. Finally, in chapter VI we draw the conclusion of this work.

Chapter 2

Switched-Capacitor DC-DC Converters

2.1 DC-DC Converter Architecture

The dc-dc converter consists of two parts (Fig. 2.1):

- the conversion block
- the control block

The conversion block is the core of the circuit and it is responsible for the conversion ratio V_{out}/V_{in}. The control block feedbacks an output variable (current or voltage) in order to stabilize the output voltage around the desired value.

The output of the switched capacitor DC-DC converter is in fact very sensitive to variations of the input and of the required output current. The control block, thus, improves the line and load regulation.

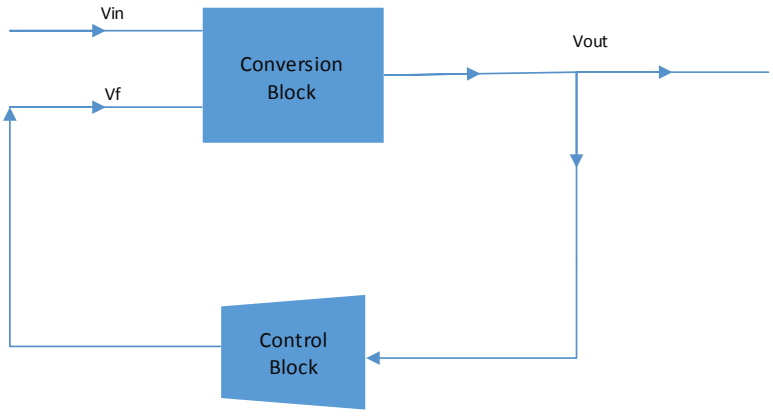

Figure 2.1: Block Diagram of the SC DC-DC converter

The operations of the core of the SC converters can be distinguished in two parts, corresponding to the two phases of the clock that drives the switches.

During one phase of the clock (φ_1), in every circuit of this family, a capacitor *C_charge* at the input, composed by some independent flying capacitor, is loaded to the input voltage according to the equivalent circuit shown in figure 2.2(a).

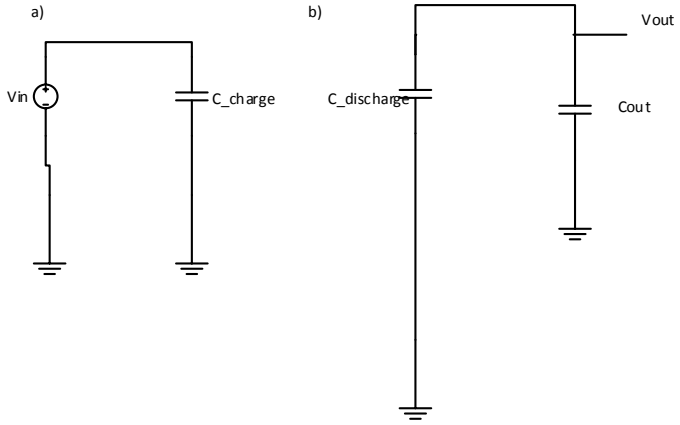

Figure 2.2: charge(a) and discharge(b) circuit of the SC DC-DC converter

During the second phase of the clock those flying capacitors, constituting the input capacitor change their position(Fig.2.2(b)). Due to this transformation, the voltage drop on the total capacitor *C_discharge*, which now is in parallel to the load, is different from the input voltage. Moreover, it will transfer a part of its charge to the load capacitor, which in steady state will reach the voltage drop due to the charge transferred from *C_discharge*.
This voltage drop, and so the voltage Conversion Ratio (CR) of the DC-DC converter is setted by choosing how the flying capacitors change their position.

2.2 Voltage Conversion Ratio

Depending on the topology of the circuit, the voltage across the flying capacitors varies.
That is a measure of the possibility to set different conversion ratio for the circuit. In general:

$$V_{out} = CR \cdot V_{in} \tag{2.1}$$

In particular, Makowski and Maksimovic settled almost all the possible conversion ratio, showing that they are a countable infinity. If number N of the capacitors is known [16][17]:

$$CR = \frac{P[k]}{Q[k]} \tag{2.2}$$

Where P and Q are the k-elements of the Fibonacci series, k is in the range of closed values [2,N+1], N is the number of capacitors used, including C_{out}. The remaining topology are described in the section 2.6.
To get a better understanding of the operation of the switched-capacitor DC-DC circuits, a basic circuit of this logic, i.e. a switched capacitors with CR=1/2, is shown in figure 2.3.

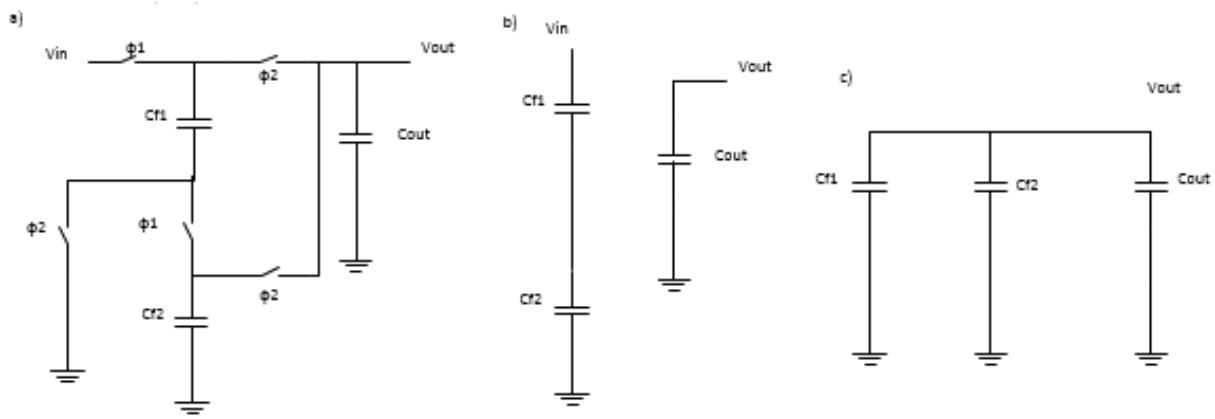

Figure 2.3: Divide by two circuit during both the phase

During the phase φ_1 (Fig. 2.3b), the input voltage charges the two flying capacitor in series (their series constitutes C_charge shown in figure 2.2). Since the two flying capacitances are the same, their voltage drop will be equal to $\frac{V_{in}}{2}$. In the phase φ_2 the flying capacitors are in parallel, then the output will be led to $\frac{V_{in}}{2}$ in steady state.

2.3 Average Model

A circuit, modeling the operations of the switched capacitor in steady state, is shown in fig.2.4.

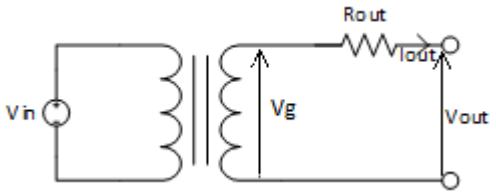

Figure 2.4: Average Model of the SC DC-DC converter

The voltage drop across the inductor is $V_g = CR \cdot V_{in}$. Since $I_L = 0$ the voltage drop on the resistence V_{Rout} is zero. Therefore, with no-load condition the output will be led to V_g, while in case the load is present, there exists a loss of delivered voltage with respect to the desired voltage $CR \cdot V_{in}$.
Seeman and Sander, in their work [18], provide a theoretical model for the R_{out} in case the duty cycle of the driving clock is 0.5. The R_{out} can be splitted in two components, R_{SSL} which predominates at low switching frequency, and R_{FSL}, which predominates at high switching frequency.

$$R_{out}=\sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.3}$$

In the calculation of R_{SSL} the conduction losses of the switches and wire are neglected because those provoked by charge-transfer prevails:

$$R_{SSL}=\sum \frac{a_{c,i}^2}{C_i f_{sw}} \tag{2.4}$$

where a_i are coefficients depending on the topology and the single flying capacitor, C_i is the flying capacitor and f_{sw} is the switching frequency. If all the flying capacitors are equal:

$$R_{SSL}=\sum \frac{a_{c,i}^2}{\mathrm{C} f_{sw}} =\frac{\mathrm{m}}{C f_{sw}} \tag{2.5}$$

where m is a figure of merit equal to $\sum a_{c,i}^2$.
You can intuitively understand this formula, by analyzing a simple DC-DC converter with a conversion ratio equal to 1 (Fig. 2.5).

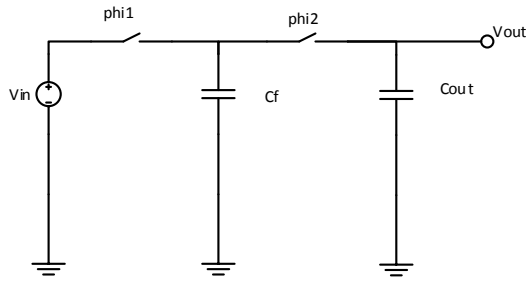

Figure 2.5: SC DC-DC converter with voltage conversion ratio equal to one

Assuming that, at the start of the phase φ_1, the voltage drop on the capacitor is Vo, The input source move in it a charge equal to $\mathrm{C}(V_i - V_o)$. This charge will be transferred, during the phase φ_2, in the output capacitor. Hence, the average current, in the period is:

$$I_{av} = \frac{\Delta Q}{T} = Cf\Delta V \tag{2.6}$$

which is the same current transferred by an equivalent resistor of $R_{eq}=\frac{1}{Cf}$.
On the other hand, in the high-frequency limit, the losses due to charge-transfer capacitors become negligible compared to conduction losses.
The parasitic series resistance of the flying and output capacitors, wire resistance and the on-resistance of the switches can be included in the conduction losses. At the beginning we consider only the ON resistance of the switches, while, the other parasitic resistances will be considered only in the post-layout simulations. Thus:

$$R_{FSL} = \sum_i 2R_i a_{ri}^2 \tag{2.7}$$

where the coefficients a_{ri} depend on the converter topology.
If the on-resistances are equal:

$$R_{FSL} = \sum_i 2R_{ON}a_{ri}^2 = 2 \cdot p \cdot R_{ON} \tag{2.8}$$

Where p is a figure of merit equal to $\sum_i a_{ri}^2$, which allows you to compare the different topologies. Note that, while R_{FSL} is independent of the frequency, R_{SSL} is inversely proportional to the switching frequency.

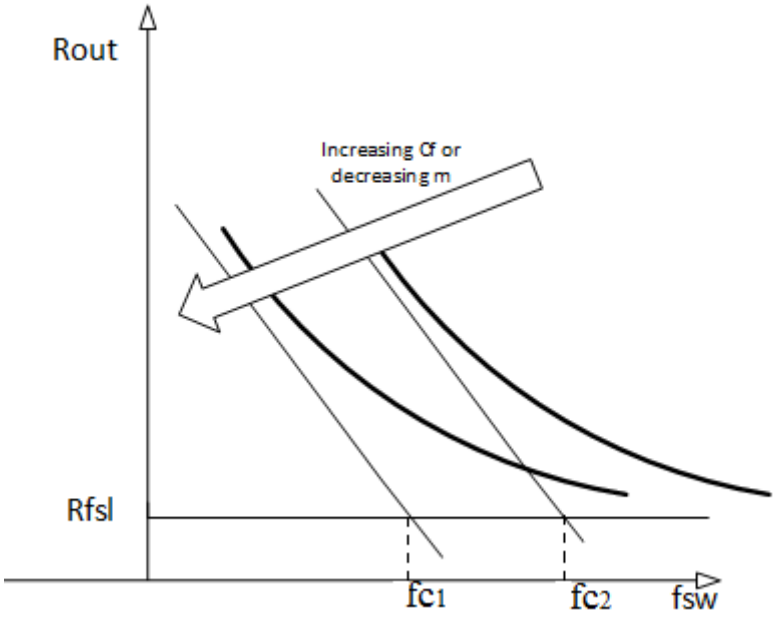

Figure 2.6: behavior of the output resistance by varying the switching frequency

The frequency where R_{FSL} is equal to R_{SSL} is called the corner frequency of f_c. Referring to the figure 2.6, we note that the maximum efficiency can be achieved only at infinite frequency (where $R_{out} = R_{FSL}$). However, after the corner frequency, the output resistance is very close to the minimum of the curve. The operative frequency will be chosen near the corner frequency, due to reasons explained in the next sections.

For this reason, we will try to minimize this corner frequency in order to work at low frequencies. By enlarging the flying capacitors, R_{SSL} decreases and the corner frequency moves to the left. Another way to decrease the f_c is to choose a topology that has smaller coefficients $a_{c,i}$.

In paragraph 3.1.1, the charge flow analysis (which is used to calculate the coefficients $a_{c,i}$ and $a_{r,i}$) will be presented and the charge balance analysis which is used to calculate the gain of the DC-DC converter in the presence and in the absence of load.

Other losses in the circuit are:

- *Bottom-plate parasitic capacitor losses.* This is probably the most significant energy loss.

  In the manufacture of the capacitors the existence of a parasitic capacitance C_{BP} between the bottom plate and the ground is inevitable. For a MIM capacitor, this parasitic effect is generated between the lower metal plate and the substrate, while

in the gate-oxide capacitors the bottom plate is the n-well and there is a parasitic junction capacitance between the p-substrate and the n-well.
For instance, in the divide-by-two circuits (Fig 2.2), during the phase φ_1, a parasitic capacitor is in parallel with the bottom capacitor. So, as the bottom capacitor, it is charged to the voltage $\frac{V_{in}}{2}$, accumulating a charge equal to $C_{BP} \cdot \frac{V_{in}}{2}$, which, during the phase φ_2, goes to ground. Therefore it is lost.
The bottom plate parasitic capacitance not always leads to a loss of energy. In the circuit in Fig2.2 the only parasitic capacitor worsening the efficiency is that due to the top-capacitor.
Since the parasitic capacitance of bottom-plate is often considered as fraction α of the flying capacitors ($C_{BP} = \alpha \cdot C_f$), the power loss can be written as:

$$P_{BP} = \frac{\alpha C_f f_{sw} V_{in}^2}{4} \tag{2.9}$$

- *Gate drive losses.* A portion of the power is dissipated by driving the switches. Assuming that the switches are implemented by MOS, the average power dissipated by driving each switch is:

$$P_{drive} = C_{ox} A_{sw} V_{in}^2 f_{sw} \tag{2.10}$$

Where $A_{sw}$is the gate area of the each switch. This power consumption must be calculated for each switch.
- *Leakage losses*. These are also present in idle state and are provoked by leakage current of the switches.
- *Control losses* are the losses in the control circuitry. Those can be splitted in dynamic and static losses of the control circuit.

$$P_{control}=N_G C_{avg} f_{sw} V_{BAT}^2 + I_{leak} V_{BAT} \tag{2.11}$$

Where N_G is the number of gates in the control circuit and C_{avg} the average capacitance switched in control circuit every period $\frac{1}{f_{sw}}$.

2.4 Efficiency

The efficiency of the switched-capacitor DC-DC converter can be written as [16]:

$$\eta = \frac{V_{out}}{M V_{in}} \tag{2.12}$$

This can be understood intuitively, analyzing the divide-by-two circuit. If, during the phase φ_1, the capacitors, now in series, draw from the source the charge q, that will be placed on

each flying capacitor. In the phase φ_2 the flying capacitors are in parallel, then the charge 2q goes to the output. Therefore, the efficiency will be[25]:

$$\eta = \frac{energy\ delivered\ to\ the\ output\ for\ period}{energy\ drawn\ from\ the\ source\ for\ period} = \frac{0.5 \cdot q \cdot V_{out}}{0.5 \cdot 2q \cdot V_{in}} \tag{2.13}$$

The maximum efficiency η_{max} is limited only by Rout and so, as mentioned, by the switching and charge-transfer losses:

$$\eta_{max} = \frac{V_o}{CRV_{in}} = \frac{CR \cdot V_{in} - R_{out} I_{out}}{CR \cdot V_{in}} \tag{2.14}$$

Considering also the other losses the efficiency becomes:

$$\eta = \frac{P_L}{\frac{P_L}{\eta_{max}} + P_{BP} + P_{Drive} + P_{Leak} + P_{control}} \tag{2.15}$$

Referring to the average model (considering only the conduction losses) the power dissipated is:

$$P_{cond} = V_{Rout} \cdot I_{out} = (CR \cdot V_{in} - V_o) \cdot I_{out} = R_{out} I_{out}^2 \tag{2.16}$$

The maximum achievable efficiency (2.14) is maximized by minimizing R_{out} (it takes into account only the conduction losses). However, the total efficiency is also affected by the control and other losses. Then, when we choose the gate-width of the switches, capacitances and switching frequency, we should find the right trade-off between all the listed losses.

In particular, in order to minimize the conduction losses you should keep, at constant flying capacitance, the frequency as high as possible to minimize the charge-transfer losses. While the gate-width of the transistors should be as high as possible in order to minimize the R_{out} in the fast switching-frequency limit. On the other hand, to reduce the switching losses you should keep a very low frequency and switches area as low as possible.

The output voltage V_O is equal to $CR \cdot V_{in}$ minus the voltage drop on the resistor. So if the value of the output resistor is R_L, V_O is given by:

$$V_O = CR \cdot V_{in} \cdot \frac{R_L}{R_L + R_{out}} \tag{2.17}$$

2.5 Loss Minimization

2.5.1 Frequency Selection

The switching frequency can be set a bit higher than the corner frequency. In this region, as the frequency increases (then increasing the control losses) R_{out} does not decrease further. The optimum frequency can be calculated either algebraically, as seen in [18] and in [19], or graphically, by means of a simulation of R_{out} to vary the switching frequency.
Another possible strategy is to set the f_{sw} as high as possible, making sure that losses in the control circuit are a reasonable portion of the output power [20].
In this system a frequency of 50KHz already exists, but it is not sufficient for achieving a very high efficiency, which is the main goal of this Master thesis. A way to achieve a very high efficiency at low frequency is to use a large flying capacitor. On the other hand, since the overall area is limited, the switches will be driven by a faster clock.

2.5.2 Selection of Switches and Capacitors

The gate-length of the switches will be set equal to the minimum possible in order to minimize the gate capacitance and so the gate-drive losses. On the other hand, the short channel effects is higher by using short transistors.
The reference [18] provides a theoretical model about the fine-tuning of the width of the flying capacitors and switches. A similar trial and error approach will be followed in this Master Thesis. The values of the gate-widths and flying capacitances will be set to minimize the conduction losses and to have an efficiency as high as possible.
In particular the optimization steps are:

- Select the switching frequency f_{sw}
- Select the load capacitance C_L
- Choose the length of switches as the lowest possible (since a 180um technology will be used L=180um)
- Maintaining the same frequency, the rise time and the fall time, find which value of flying capacitor achieves the desired output voltage (and an admissible maximum efficiency η_{max}). The value of the capacitors also affect start-up time.
- Maintaining the same frequency, the rise time and the fall time of the clock and flying capacitors, you set the width W the same for all switches. Then you vary the widths as long as the maximum efficiency is reached (note that the output resistence in the fast – switching limit is more affected by the transistors having an higher v_{gs}, which, in general, is different for different transistors)
- Re-optimize the value of the flying capacitor varying it between a minimum and a maximum.
- Optimize the thickness of each switch individually

The output capacitor will be set manually in order to have an acceptable ripple. Neglecting its parasitic series resistance, the relation between C_L and the ripple is:

$$V_{ripple} = \frac{I_{out}}{f_{sw} C_L} \tag{2.18}$$

2.6 Examples of Topologies

Resuming of paragraph 2.1 we can list some of the endless amount of the switched capacitor topologies. They can be classified into three categories:

• Series-parallel converter: During the first phase, the flying capacitors are connected in series between the input node and the output node and during the second phase are parallel output (Fig. 2.7).

• Ladder converter: This family of SC DC-DC Converters (Fig.2.8) consists of two strings of series capacitors which, passing from phase 1 to phase 2 slide over each other. It provides a conversion ratio of $\frac{2}{(n+3)}$, where n is the number of the flying capacitors.

The efficiency of these converters is very low because the output is loaded from multiple nodes and because the number of switches is very high.

• Fractional converter: they are the remaining converters. They do not belong to the previous categories, but their existence is testified by the formula (2.1).

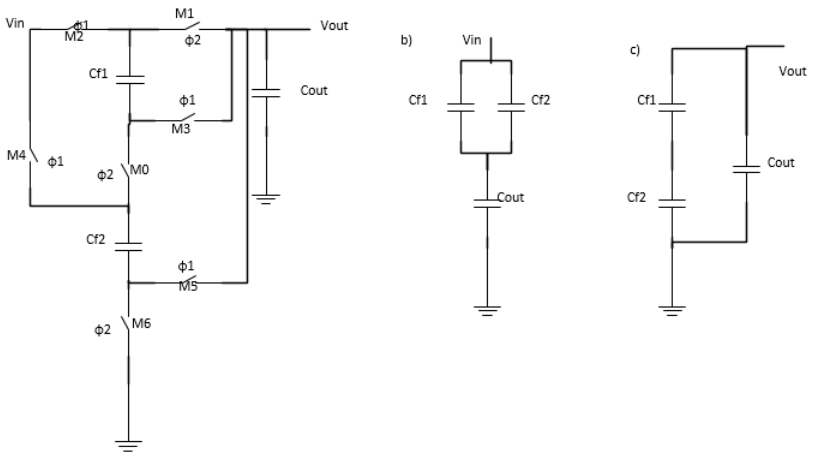

Figure 2.7: Example of series parallel converter

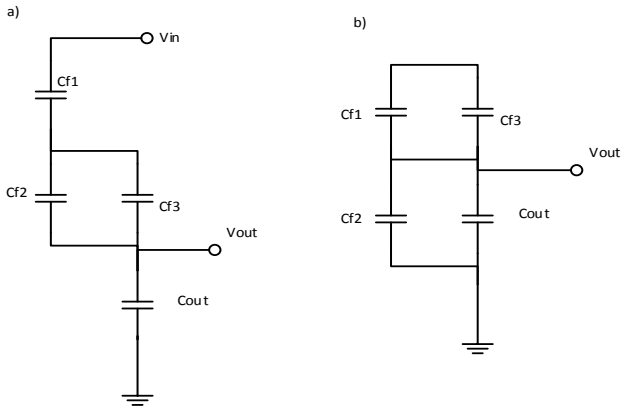

Figure 2.8: Example of ladder converter during its charge phase(a) and discharge phase (b)

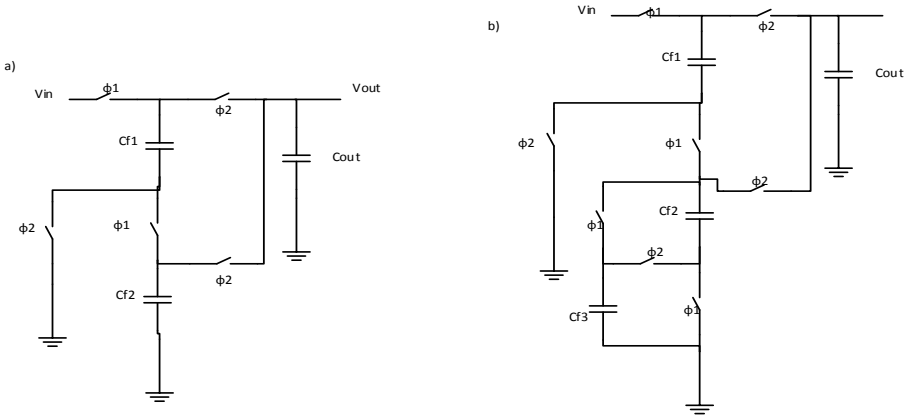

Figure 2.9: Various types of SC DC-DC converter with different CR i.e. (a) 1/2, (b) 2/3

In the figures 2.9, various types of gain setting are represented. For instance, a CR equal to 2/3, as the equation (2.1) suggest, has to be implemented with at least two floating capacitors.

Effectively, the figure 2.9b shows the implementation with three elementary capacitors. In the charging circuit (phase φ_1) there are 2 capacitors in series, which will be loaded to V_{in}. Assuming that the flying capacitances are equal, the bottom capacitors has a value of 2C, while the upper capacitance C. So the upper capacitor, at the end of φ_1, will get a voltage drop of $\frac{2V_{in}}{3}$, while the bottom capacitor of $\frac{V_{in}}{3}$. During φ_2, the bottom capacitors is divided into two capacitance C, which will be placed in series. The upper capacitor will be positioned in parallel to the series of these capacitors. Hence, the output will be led to the value $\frac{2V_{in}}{3}$.

An other possible CR is 3/5. That topology could be implemented with at least three elementary capacitors C.

Note that the same conversion ratio can be obtained with an infinite number of different circuits. These circuits, however, differ in R_{out}, due to changes of the vectors a_i and a_{ri} (see equations 2.3 and 2.5).

Table 2.1: Achievable conversion ratio with different numbers of flying capacitors

n° flying capacitors	Voltage Conversion Ratio
1	1/2; 1; 2
2	1/3; 1/2; 2/3; 1; 3/2; 2;3
3	1/5; 1/4; 1/3; 1/2; 3/5; 2/3; 3/4; 4/5; 1; 5/4; 4/3; 3/2; 5/3; 2; 5/2; 3; 4; 5
4	1/8; 1/7; 1/6; 1/5; 1/4; 2/7; 1/3; 3/8; 2/5; 3/7; 1/2; 4/7; 3/5; 5/8; 2/3; 5/7; 3/4; 4/5; 5/6; 6/7; 7/8; 1; 8/7; 7/6; 6/5; 5/4; 4/3; 7/5; 3/2; 8/5; 5/3; 7/4; 2; 7/3; 5/2; 8/3; 3; 7/2; 4; 5; 6; 7; 8

2.7 Output Voltage Control

Many applications, such as DVS and U-DVS, need to control the ratio V_{out}/V_{in}. In these applications, the desired power supply can vary depending on the performance needs. In other applications, as in the case of this thesis, the input voltage across the supercapacitor, or the output current, may also vary. This could lead to a poor quality of the line and load regulation.

There are many ways to adjust DC-DC conversion. Most of them are based on an increase in the output resistance R_{out} with consequent reduction of the efficiency [26]:

- Hysteretic. This is the only technique that does not lead to efficiency deterioration. Depending on the required voltage, the control changes the topology (then the conversion ratio) [20-24][29].
- Series LDO. An LDO regulator will be placed at the output of the SC DC-DC converter, in order to regulate the output voltage. This very common technique is useful for reducing the output noise.
  The whole regulator is constituted by the SC DC-DC converter, to achieve a coarse, but large, regulation, and, by an LDO to achieve finer regulations.
- Duty cycle control. This technique is based on the dependence of R_{FSL} from the duty-cycle. The main drawback of this technique is the highly nonlinear dependence.
- R_{on}modulation. As seen R_{FSL} depends on the on-resistance of the switches, then the output can be fed back through an error amplifier, which modulates the voltage V_{gs} of one or more resistances. The R_{ON} modulation can be also achieved by using segmented switch.
- Pulse frequency modulation (PFM). As mentioned above, by varying the frequency of the driving clock, the R_{SSL} varies. In particular, if the f_{sw} increases, R_{SSL} would decrease[18].

Chapter 3

Analysis of the Selected Topologies

The required voltage at the output is 1V. Since the voltage at the input of the switched capacitor is 1.8V-2V, we will analyze down-converters with a conversion ratio equal to ½ or slightly higher.
Among the infinite number of implementations, given by the series 2.2, only the ones that could fulfill the requirement will be selected and compared. Then we will choose the topology with the best efficiency, satisfying the flying capacitance limitations due to area constraints. Moreover, since the area occupied by the entire chip is limited, the maximum value of flying capacitances will be also limited (<60pF).

3.1 Divide-by-two with Two Charge Transfer Capacitors

The divide-by-two with two flying capacitors has been introduced in the previous chapter. A theoretical analysis, explained below, can help understand which factor affects the output voltage. By currently ignoring the losses due to the bottom-plate capacitor, to the gate-drive and to the control losses, only the output resistance of the equivalent model is responsible for the decrease of the maximum efficiency η_{max} (see the chapter 2). Referring to paragraph 2.3, we can also calculate the output resistance in the slow and fast switching-frequency limit with a simple analysis.

3.1.1 The Two Switching-Frequency Limits and the Charge Flow Analysis

3.1.1.1 Slow Switching-Frequency Limit

In the slow Switching-Frequency Limit (SSL), the predominant contribution of Rout is:

$$R_{SSL} = \sum_i \frac{a_{c,i}^2}{C_i f_{sw}} \tag{3.1}$$

The a_{Ci} coefficients are the ratio between the charge flowing, during a period in steady state, in the capacitor Ci and the charge flowing in the output capacitor in both phases:

$$a_C = [\frac{q_1}{q_{out}} \quad \frac{q_2}{q_{out}} \quad \dots \quad \frac{q_N}{q_{out}} \quad] \tag{3.2}$$

Where the q_i are the charge flowing, during the steady state, in the capacitor C_i.
To calculate them, current flow analysis is needed. You should consider that, in steady state:

- The charge flowing, during a phase, in a floating capacitor is equal and opposite to that flowing during the other phase.
- When the input is disconnected, the sum of the charges flowing in capacitors (including in the output capacitor) must be equal to zero.
- In slow switching-frequency limit, losses due to non-ideal switches are not considered.
- The output voltage is considered constant, since the output capacitor is much larger than the flying capacitor.

In this circuit, during the phase φ_1, the two flying capacitor are in series. Therefore, they draw the same amount of charge from the input supply. On the other hand, the output capacitor is not drawing charge because it is disconnected from the circuit.
During the phase φ_2, by defining the charge flowing in C_{out} as q, a charge $^q/_2$ flows in the capacitors C_1 and C_2, which are in parallel. Then:

$$a_{c,1} = a_{c,2} = \frac{1}{2} \tag{3.3}$$

Thus:

$$R_{SSL} = \frac{1}{4C_1 f_{sw}} + \frac{1}{4C_2 f_{sw}} \tag{3.4}$$

If the two capacitors are equal:

$$R_{SSL} = \frac{m}{C_f f_{sw}} \tag{3.5}$$

Where $m = \frac{1}{2}$.
Furthermore, by using this analysis, it is easier to understand formula 2.13. In a period, the charge drawn from the input source is q / 2, while the charge q is delivered to the output (for a generic topology the efficiency is $\frac{V_o}{\mathrm{CR} \cdot V_{in}}$)

3.1.1.2 Fast Switching-Frequency Limit

The predominant contribution of the output resistance in the fast-switching frequency limit is:

$$R_{FSL} = 2\sum_i a_{r,i}^2 R_{on} \tag{3.5}$$

The coefficients $a_{r,i}$ are the ratio between the charge flowing in the i-th switch, during the steady state, and the charge transferred to the output capacitor during the whole period. They, as the coefficients $a_{c,i}$, are calculated in steady state.
Once we have analyzed the circuit for the calculation of the quantity $a_{c,i}$, it is easy to see in which switch the charge flows and, therefore, to calculate the $a_{r,i}$ coefficients. For the circuit analyzed:

$$a_r = [\,\tfrac{1}{2}\ \ \tfrac{1}{2}\ \ \tfrac{1}{2}\ \ \tfrac{1}{2}\ \ \tfrac{1}{2}\,] \tag{3.6}$$

Since the Ron of the switches has the same weight factor in the sum (formula 3.5), the best way to optimize them is to make them the same. Thus, the optimal width will be higher in the MOS switches where v_{GS} is lower. For the analyzed circuit $p = \sum_i a_{r,i}^2 = \frac{5}{4}$.

3.1.2 Charge Balance Analysis

In order to calculate the conversion ratio of the surveyed SC DC-DC converters, we can use a steady-state analysis, called charge balance analysis. The assumption in the paragraph 3.1.1 are still valid.
The charge provided by the flying capacitors to the output capacitor is the same quantity of charge that must be dissipated in the output load during the period:

$$\sum Q_{c,i}^{(2)} = Q_{out} + \sum Q_{c,i}^{(2)} \tag{3.7}$$

This charge can be easily calculated by assuming that the voltage drops across the flying capacitor value known in both phases. For instance, considering the discharge circuit at the beginning of the phase φ_2 (Fig 3.2(c)), i.e. at the end of the charging phase, we could make sure that the CR of the circuit under test, without load, is ½. The voltage drop on the flying capacitors is Vin / 2, while, the voltage across the output capacitor is Vo. Thus, the charge transferred from the single capacitor is $C_f(\frac{Vin}{2} - V_o)$. In the absence of load, the charge drawn is $Q_{out} = 0$. Considering the point in the paragraph 3.1.1.1:

$$Q_{c,1}^{(1)} = Q_{c,2}^{(1)} = -Q_{c,1}^{(2)} = -Q_{c,2}^{(2)} \tag{3.8}$$

Therefore:

$$4 \cdot C_f \left(\frac{Vin}{2} - V_o\right) = 0 \Rightarrow V_o = \frac{Vin}{2} \tag{3.8}$$

If the output current is different from 0, there would exists a loss of delivered voltage with respect to the output voltage $M \cdot Vin$ without a load:

$$V_o = \frac{Vin}{2} - R_{out} I_L \tag{3.10}$$

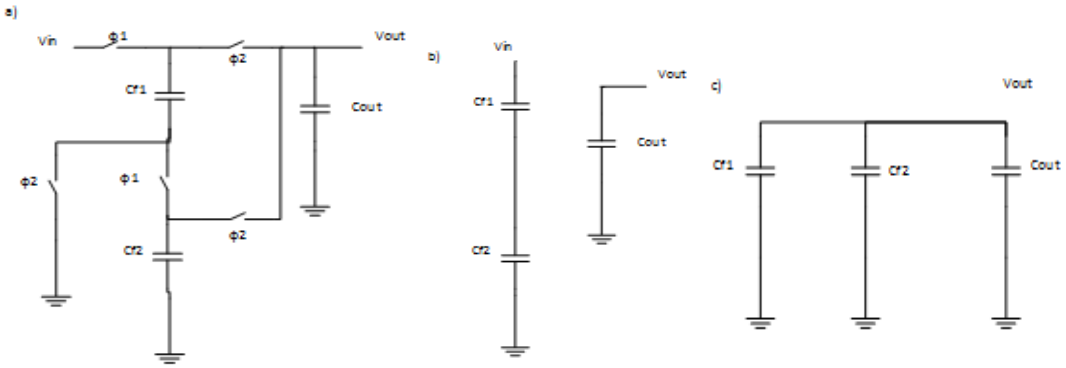

Figure 3.1: Divide-by-two with two flying capacitor. a)whole circuit b)charge circuit c)discharge circuit

3.1.3 Flying Capacitances and Transistor Sizing

The steps that will be followed during the loss minimizing and trade-offs are described in section 2.5.
A switched capacitor DC-DC converter could achieve very high efficiency, as we see from the first simulation (Fig. 3.2), but it should have a very large flying capacitor in order to keep low frequency and to reduce the driving losses (section 2.4). In particular, the simulation has been performed with a fixed frequency equal to 50KHz, while the biosensor at the output is modeled by a resistance of 100kΩ.
Furthermore, choosing an output capacitor of 100nF, form the equation 2.17 you can calculate the ripple of the output voltage:

$$V_{ripple} = \frac{I_{out}}{f_{sw} C_L} = 2mV \tag{3.11}$$

However, due to the area constraints, we cannot use large capacitor. Indeed, the overall area of the SC DC-DC converter is mainly affected by that of the flying capacitors. In particular, in the 180um technology, the used MIM capacitor has a density of 1.003fF/μm^2 (a 50pF capacitor occupies an area of $5 \cdot 10^4 \mu m^2$). The efficiency, when the flying capacitances are the admissible value 50pF, drops very quickly. Therefore, in order to use smaller capacitors the frequency must be higher. In this way, as discussed in the previous chapter, the RSSL

will rise, moving the corner frequency to the higher frequencies where the switching losses are higher.

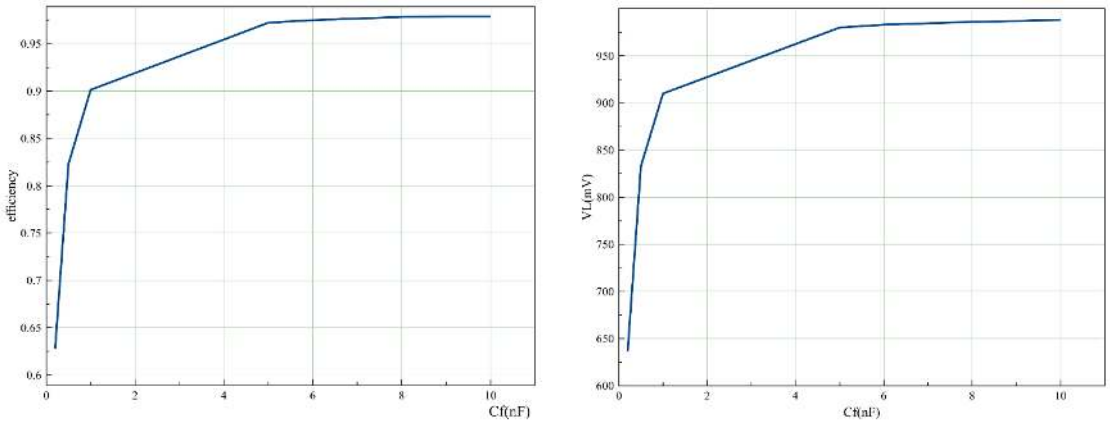

Figure 3.2: Efficiency and output voltage of the divide-by-two circuit with two flying capacitors by varying the flying capacitances

The figure 3.3 shows the behavior of the efficiency and the output voltage versus the frequency. We want to calculate the optimum frequency (maximizing the efficiency) for this topology using flying capacitances of 50pF. Frequency varies from 200KHz to 1MHz with a step of 100KΩ (W is fixed to 10 μm). Note that the overall efficiency is limited not only by Rout, but also by the gate-drive losses, which increase with the frequency. Because of this, the frequency that maximizes the total efficiency is different from an infinite frequency, which only minimizes losses due to the Rout. In this simulation also the losses of drivers are taken into account.

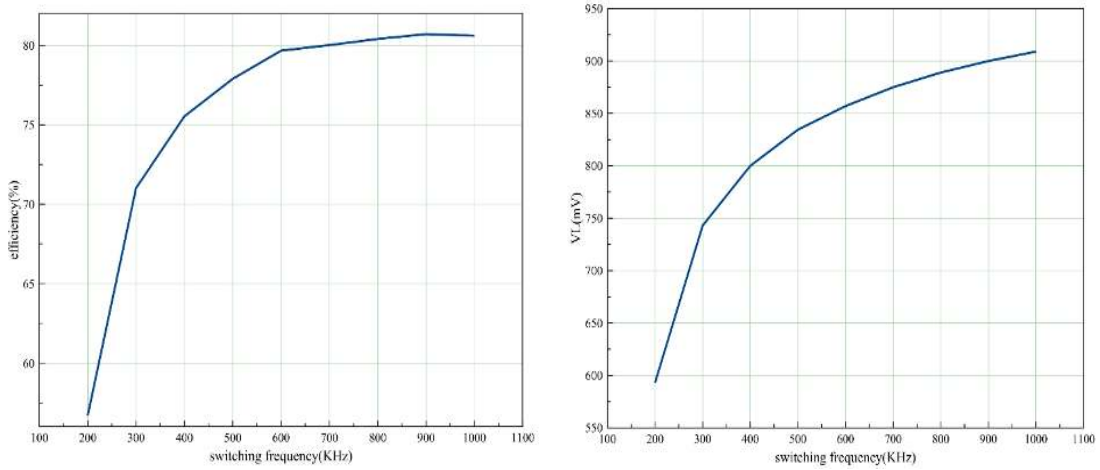

Figure 3.3: Efficiency and output voltage of the divide-by-two circuit with two flying capacitors(50pF) by varying the switching frequency

The output voltage V_L depends only on Rout, in particular, by increasing the switching frequency, it is monotonically increasing. The optimum frequency, for values of capacitance achievable on-chip (50 pF), is placed at too high frequencies. It is situated around 900KHz, but the efficiency is already stable around 600K.

The graph, shown in figure 3.4, is achieved by varying the gate width of the switches (which are MOS). Note that, by varying W, R_{ON} of switches varies, and that influences the R_{FSL}. This optimization of the width (minimizing the losses) is carried out at the previously found optimum frequency (so it was used a large capacitor to lower the corner frequency).
The trend of the efficiency, with the rise of W, is due to two effects:

- the decrease of Rout in fast-switching limit (which is proportional to Ron) and
- the increase of the gate-drive losses and leakage losses.

Indeed, by increasing W the delivered voltage at the output will grow, since the output resistance in the fast-switching limit decreases.
The gate-widths W are chosen equal to 4µm, where the delivered voltage is close to the maximum (903.5mV by using a width of 4µm and 907mV by using a width of 10u) and the efficiency is close to the maximum (88.1%).
It is necessary to find more efficient topologies, for which the factor m, and so the output resistance in the SSL, is smaller.

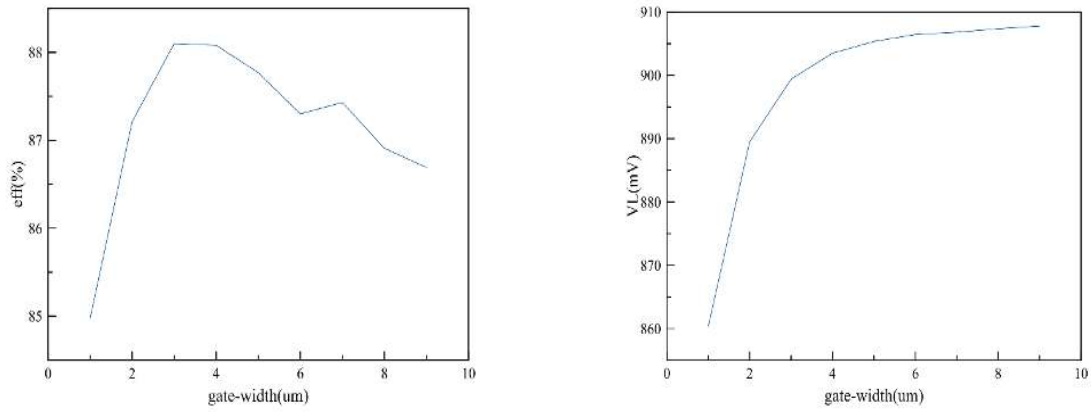

Figure 3.4: Efficiency and output voltage of the optimized circuit

3.2 Divide-By-Two with one Charge-Transfer Capacitor

3.2.1 Theoretical Analysis

As suggested by the formula 2.2 (Makowski and Maksimovic's formula), a divide-by-two can be also implemented with a single flying capacitor (figure 3.5).

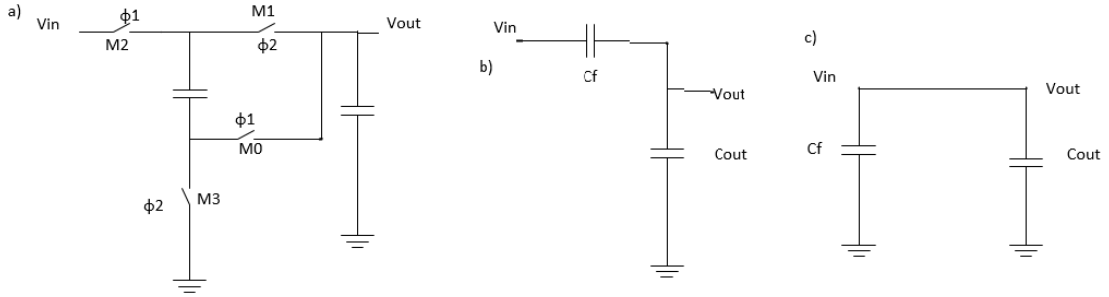

Figure 3.5: Divide-by-two with one flying capacitor a)whole circuit b)charge circuit c)discharge circuit

In order to calculate the conversion ratio of this circuit, charge balance analysis, presented above, must be done. The charge transferred into C_f during the charge phase (Fig. 3.5a) must be equal to the charge transferred from C_f to the load during the discharge phase (Fig. 3.5b). Assuming that Vo is constant during φ_1, the voltage drop across Cf changes from Vo (in fact, at the end of phi2, C_f is loaded to output voltage) to Vin-Vo. Therefore, the charge difference is $C_f(V_{in} - 2V_o)$.
The charge delivered to the load is equal to 0 in the absence of load, and then equating the two charges, we have:

$$V_{in} - 2V_o = 0 \Rightarrow V_{in} = 2V_o \tag{3.12}$$

then the conversion ratio of the topology is ½.
In order to calculate the factor m and the factor p, a charge flow analysis has been performed. During the phase φ_1 (Fig 3.5a) the charge flowing in the capacitor C_f is the same flowing in C_{out}. In phase φ_2, an amount of charge q_1 is trasferred from C_f to C_{out}. Therefore, the total charge flowing in C_{out} throughout the period is $2 \cdot q_1$, then the coefficient $m = a_{c,1}^2 = \frac{1}{4}$. While the coefficients $a_{r,1} = [\frac{1}{2}\ \frac{1}{2}\ \frac{1}{2}\ \frac{1}{2}]$. Then $p = 1$.

3.2.2 Advantages of this Topology

Comparing the second topology of divide-by-two circuit to the first one, we note that the factor m is much lower for the second topology. This means that the corner frequency is lower, and therefore the switching losses are reduced.

The flying capacitors are two in the first topology, while only one in the second, and then, the flying capacitance of the second topology can be doubled by keeping the occupied area constant. The switches are only four, so the load capacitance of the driving circuit is smaller, and the factor p is reduced (it is 1 instead of 5/4 of the first topology).

Table 3.1: Comparison between the different topologies with the same CR (1/2)

	Two flying capacitors	One flying capacitor
CR	0.5	0.5
Number flying capacitors	2	1
Number switches	5	4
m factor	½	¼
p factor	5/4	1
Efficiency max (with Cf=50pF)	88.1%	90.77%

3.2.3 Sizing and Simulations

In order to obtain a high efficiency with small flying capacitors, we have to properly design the capacitances and operating frequency. The circuit has been simulated using three different flying capacitors (25pF, 50pF and 60pF), which satisfy the area constraints. For each of these, the optimum frequency and the efficiency at this frequency is calculated. After that frequency you could not have great improvements of Rout but only deterioration of the gate-drive losses.
The simulation has been performed using Cadence tool, the output capacitor is set to 1nF, the width to 4µm and the load resistance, modeling the digital part of the biosensor, with 100kΩ. It is worth noting that also the driver's losses are taken in account.

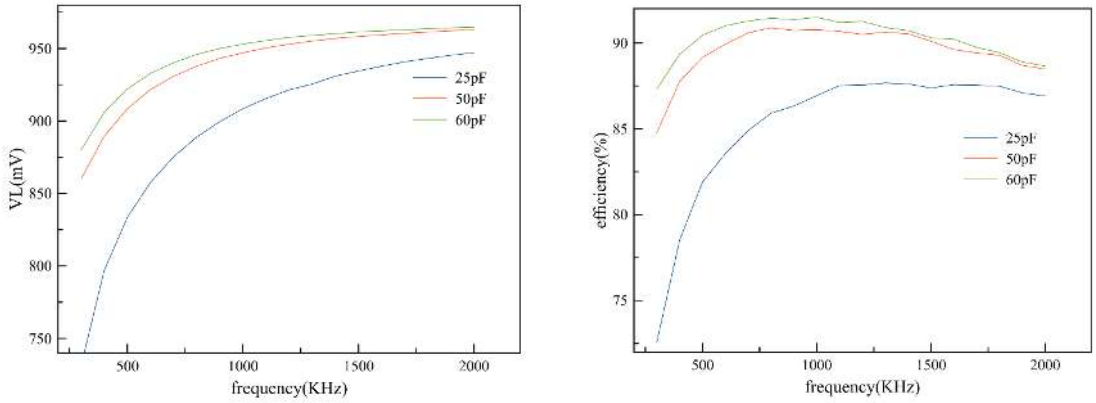

Figure 3.6: Efficiency and output voltage of the divide-by-two circuit with one flying capacitors by varying the switching frequency. The analysis has been performed with three different value of the flying capacitance: 25pF(blue), 50pF(red), 60pF(green)

Using a C_f = 25pF (five MIM capacitors 50µm x 100µm) the optimum frequency is placed around 1.3MHz (efficiency of 87.67%), i.e. in the SSL (the output voltage is 925.5V). Raising the frequency up to 2MHz output voltage could reach 947.2mV(efficiency of 86.91%).
Using a C_f = 50,15 pF the optimum frequency is 1MHz. It is less than the previous case and so the switching losses are reduced (in fact the maximum efficiency is 90.77%), while the output voltage is 947mV. At 2MHz the output voltage is 962.8mV, while the efficiency is 88.95%.
Using a C_f = 60,18pF the optimum frequency is at 1MHz (efficiency of 91.5% and output voltage of 953.1mV). After 1.5MHz frequency the output voltage is roughly constant and reaches (964.8mV), while an efficiency of 90.3%. We will then use the last value of flying capacitance, since the circuit respects the area constraint and can achieve a much higher efficiency than the other values.
Nevertheless, the efficiency and the output voltage could be enlarged by sizing the gate-widths of the transistors, following the steps described in the paragraph 2.5

3.2.4 Transistors Sizing

The primary goal is to increase the output voltage and efficiency. By increasing the width of the switches, the output voltage always increases, while the efficiency has a well-defined maximum.
Firstly, it was made a simulation at 1.5MHz, varying the width of the switches from 1µm to 10µm with a step of 1µm (Fig. 3.7). It turns out that (by setting all W equal) the W_{opt}, which minimizes the overall losses, is equal to 6µm (the simulation was carried out by with a load resistance of 100kHz).
Then, the gate-widths of the MOS Transistors have been varied individually, with steps of 0.25µm, reaching a right trade-off between the output voltage and the efficiency (Table 3.2).

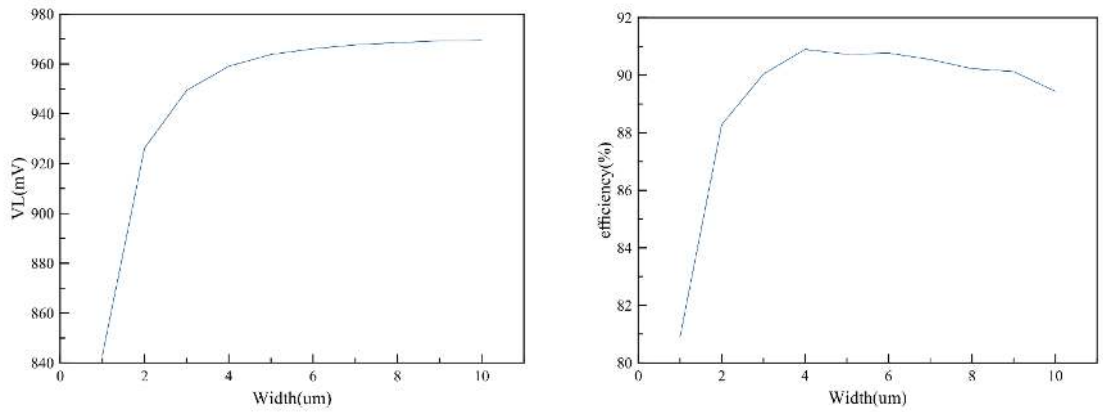

Figure 3.7: Behavior of the efficiency and output voltage by varying the gate-width of the switches

Since all the Ron have the same weight factors in the sum, which provides the R_{FSL}, the chosen width should be higher for that MOS having a low Vgs (M1 and M0), and, is the lowest for the NMOS. Note that the only NMOS used in this circuit is the switch with a terminal connected to the ground, in order to optimize its on-resistance.

Table 3.2: Optimization of the gate width of the four switches.

W0	W1	W2	W3	VL	Efficiency
6um	6um	6um	6um	966.1mV	90.77%
6um	6.25um	6um	6um	966.5mV	90.77%
6um	6.5um	6um	6um	966.65mV	90.77%
6um	6.75um	6um	6um	966.88mV	90.78%
6um	7um	6um	6um	966.95mV	90.81%
6um	7.25um	6um	6um	967.05mV	91.11%
6um	7.5um	6um	6um	967.12mV	91.09%
6um	7.75um	6um	6um	967.15mV	90.76%
6.5um	7.25um	6um	6um	967.6mV	90.65%
6.75um	7.25um	6um	6um	967.8mV	90.72%
7um	7.25um	6um	6um	967.95mV	90.81%
7.25um	7.25um	6um	6um	968.1mV	90.81%
7.5um	7.25um	6um	6um	968.2mV	90.74%
7.25um	7.25um	6um	5.75um	968mV	90.97%
7.25um	7.25um	6um	5.5um	968mV	90.91%
7.25um	7.25um	6um	5.25um	968mV	90.81%
7.25um	7.25um	6um	5um	968mV	91%
7.25um	7.25um	6um	4.75um	968mV	91.08%
7.25um	7.25um	6um	4.5um	968mV	90.65%
7.25um	7.25um	6um	4.25um	968mV	90.71%
7.25um	7.25um	6um	4um	968mV	90.79%
7.25um	7.25um	6um	3.75um	968mV	90.85%
7.25um	7.25um	6um	3.5um	968mV	90.91%
7.25um	7.25um	6um	3.25um	968mV	90.99%
7.25um	7.25um	6um	3um	967.9mV	91.05%
7.25um	7.25um	6um	2.75um	967.9mV	91.14%
7.25um	7.25um	6um	2.5um	967.9mV	91.17%
7.25um	7.25um	6um	2.25um	967.9mV	91.25%
7.25um	7.25um	6um	2um	967.9mV	91.22%
7.25um	7.25um	6um	1.75um	967.9mV	91.24%
7.25um	7.25um	5.75um	2.5um	967.8mV	91.34%
7.25um	7.25um	5.5.um	2.5um	967.7mV	91.27%
7.25um	**7.25um**	**6.25um**	**2.5um**	**968mV**	**91.17%**
7.25um	7.25um	6.5um	2.5um	968mV	91.03%
7.25um	7.25um	6.75um	2.5um	968mV	91.04%
7.25um	7.25um	7um	2.5um	968mV	91.01%

By choosing W0, W1, W2, W4 equal to 7.25u, 7.25u, 6.25u, 2.5u you reach an efficiency of 91.17%. This choice is the best trade-off between the maximization of the output voltage and efficiency.
We note that the optimum width of switches M0 and M1 are the same because they have two very similar driving voltage. The optimum width of the MOS M3, on the other hand, is lower because it is a NMOS. Furthermore, the variation of W3 has a little influence on the output resistance because the R_{ON} of the switch M3 is much lower than the others.
The achieved efficiency is 91.17% (taking into account also the losses of the drivers), while the output voltage is 968mV, this means that there is a loss of 32mV due to the output resistance.

3.3 Conversion Ratio equal to 2/3

3.3.1 Two Charge-Transfer Capacitors

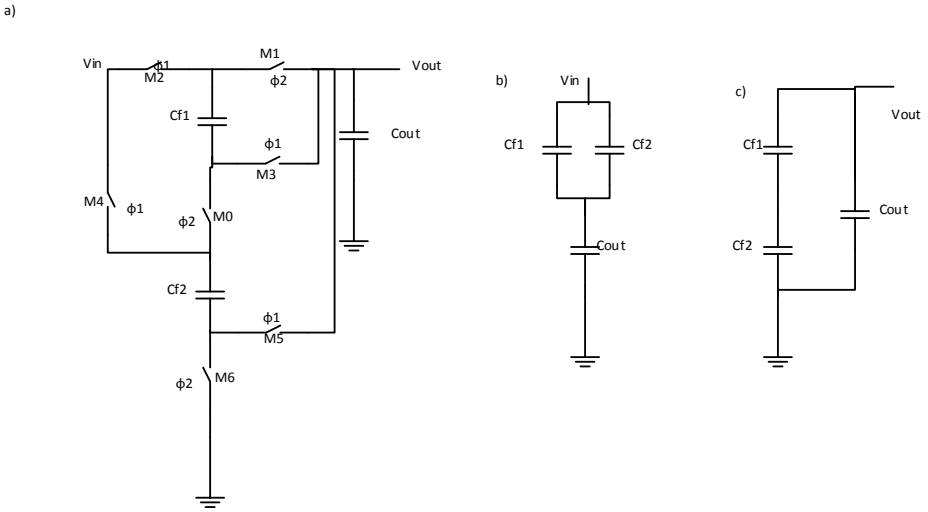

Figure 3.8. SC DC-DC converter with CR equal to 2/3 and with two flying capacitor. a)whole circuit b)charge circuit c)discharge circuit

By performing the same analysis done in the previous topologies, you could calculate the figures of merit m and p for the topology shown in figure 3.8.
A conversion ratio of 2/3, obtained from this topology, can be very useful in the case previous topologies fail to obtain an output voltage high enough. We could obtain the same conversion ratio with a number of capacitors greater than or equal to two. This paragraph describes the implementation with only two flying capacitors, while, the implementation with three flying capacitors will be shown in the next section. From the theoretical analysis we obtain

$$a_{c,1} = \left[\frac{1}{3}\ \frac{1}{3}\right] \tag{3.13}$$

$$a_{r,1} = [\frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}] \tag{3.14}$$

assuming that all the flying capacitors C_f and all the on resistance of the transistors R_{ON} are equal, p = 7/9 and m = 2/9.
The simulation in the figure was performed with C_f=50pF (we have 2), Cout = 5nF and W = 4µm.

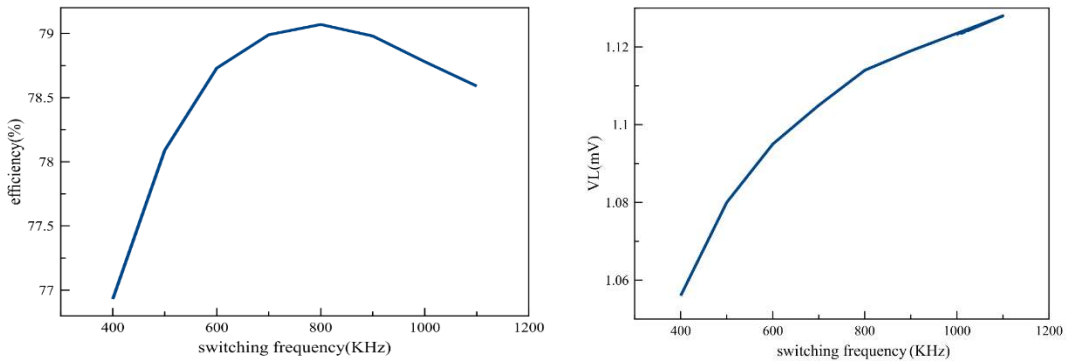

Figura 3.9: Efficiency and output voltage of the SC DC-DC converter with CR=2/3 with two flying capacitors by varying the switching frequency.

The optimum frequency is 800KHz (shifted to the right compared to the divide-by-two circuit with the same capacitance). From the graph of the VL(Fig.3.9(b)) we note that the corner frequency is moved much higher up.
The width of the MOSes has been optimized by following the steps already used in the previous paragraphs (Table 3.3). In particular, referring to the figure 3.8, the Ron that mainly influences the output resistance is due to the switch M0, because its Vgs is the lowest. Other widths, however, do not affect much the output voltage, but they are added to the load capacitances of the drivers.

Table 3.3: Optimization of the gate width of the seven switches.

5um	5um	5um	5um	5um	5um	5um	1.19	80.78
5um	5um	5um	5um	5um	5um	4um	1.19	80.8
5um	5um	5um	5um	5um	5um	3.5um	1.19	80.95
5um	5um	5um	5um	5um	5um	3um	1.19	80.76
5um	5um	5um	5um	5um	5um	2.5um	1.19	81.06
5um	5um	5um	5um	5um	5um	2.25um	1.19	81.19
5um	5um	5um	5um	5um	5um	2um	1.19	81.09
6um	5um	5um	5um	5um	5um	2.25um	1.127	81.47
7.5um	5um	5um	5um	5um	5um	2.25um	1.138	82.23
9um	5um	5um	5um	5um	5um	2.25um	1.146	83
10.5um	5um	5um	5um	5um	5um	2.25um	1.151	83.32

12um	5um	5um	5um	5um	5um	2.25um	1.158	83.82
14um	5um	5um	5um	5um	5um	2.25um	1.164	84.22
16um	5um	5um	5um	5um	5um	2.25um	1.169	84.39
18um	5um	5um	5um	5um	5um	2.25um	1.173	84.71
20um	5um	5um	5um	5um	5um	2.25um	1.177	84.92
22um	5um	5um	5um	5um	5um	2.25um	1.18	85.21
24um	5um	5um	5um	5um	5um	2.25um	1.183	85.3
26um	5um	5um	5um	5um	5um	2.25um	1.186	85.41
28um	5um	5um	5um	5um	5um	2.25um	1.188	85.63
30um	5um	5um	5um	5um	5um	2.25um	1.19	85.74
33um	5um	5um	5um	5um	5um	2.25um	1.193	85.85
37um	5um	5um	5um	5um	5um	2.25um	1.197	85.97
41um	5um	5um	5um	5um	5um	2.25um	1.2	86.23
45um	5um	5um	5um	5um	5um	2.25um	1.203	86.42
50um	5um	5um	5um	5um	5um	2.25um	1.206	86.38
40um	5um	5um	5um	5um	5um	2.25um	1.199	86.16
40um	4.50um	4.5um	5um	4.5um	5um	2.25um	1.199	86.26
40um	4um	4um	5um	4um	5um	2.25um	1.199	86.12
40um	3.5um	3.5um	5um	3.5um	5um	2.25um	1.199	86.16
40um	3um	3um	5um	3um	5um	2.25um	1.199	86.37
40um	2.75um	2.75um	5um	2.75um	5um	2.25um	1.199	86.23
40um	2.5um	2.5um	5um	2.5um	5um	2.25um	1.199	86.39
40um	2.25um	2.25um	5um	2.25um	5um	2.25um	1.199	86.63
40um	6um	6um	5um	6um	5um	2.25um	1.199	85.99
40um	7um	7um	5um	7um	5um	2.25um	1.199	85.92
40um	2.25um	2.25um	5um	2.25um	5um	2.25um	1.199	86.63
40um	2.25um	2.25um	5um	2.25um	4um	2.25um	1.198	86.65
40um	2.25um	2.25um	5um	2.25um	3.5um	2.25um	1.198	86.57
40um	**2.25um**	**2.25um**	**5um**	**2.25um**	**3um**	**2.25um**	**1.197**	**86.75**
40um	2.25um	2.25um	5um	2.25um	2.75um	2.25um	1.197	86.64
40um	2.25um	2.25um	5um	2.25um	2.5um	2.25um	1.197	86.58
40um	2.25um	2.25um	5um	2.25um	2.25um	2.25um	1.196	86.73

The chosen widths are highlighted. You can note that the efficiency is improved by about 6% .

3.3.2 Implementation with Three Flying Capacitors

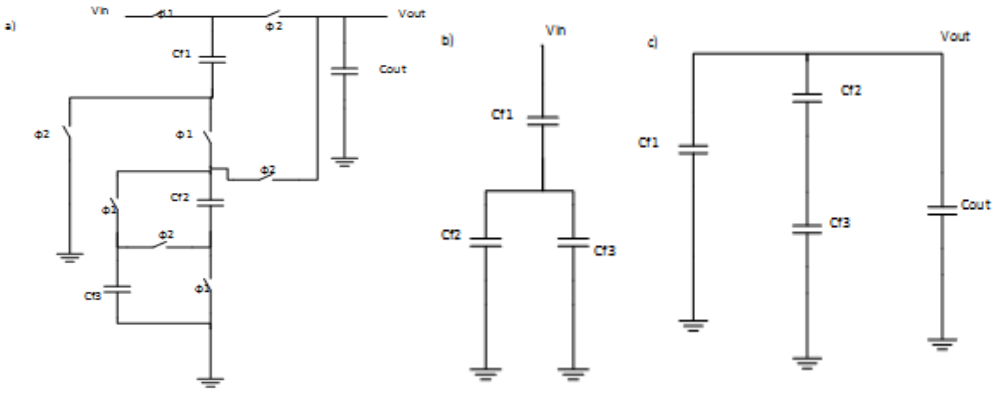

Figure 3.10: SC DC-DC converter with CR=2/3 with three flying capacitor a)whole circuit b)charge circuit c)discharge circuit

The figures of merit were calculated by using the theoretical analysis presented above:

$$a_{c,1} = [\frac{2}{3}\ \frac{1}{3}\ \frac{1}{3}] \tag{3.15}$$

$$a_{r,1} = [\frac{2}{3}\ \frac{2}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{2}{3}\ \frac{2}{3}\ \frac{1}{3}\ \frac{1}{3}] \tag{3.16}$$

Therefore m = 2/3 and p = 20/9.
The simulation in the figure was performed with C_f= 50pF (we have 3), C_{out} = 5nF and W = 4µm
The optimum frequency and situated around 1.6MHz (Fig 3.11). This circuit gets a maximum efficiency of 70%, which is worse than the previous circuits. Moreover, it can deliver a voltage less than the implementation with only two flying capacitors. Therefore we discarded it.

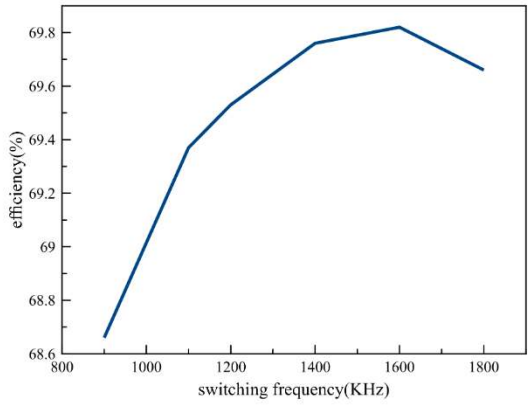

Figura 3.11: Efficiency of the SC DC-DC converter with CR=2/3 with three flying capacitors by varying the switching frequency

3.4 Conversion Ratio equal to 3/5

The last tested topology has CR equal to 3/5. It has a CR higher than ½ but not too much. In this way, it is able to obtain 1 V output from a 2V input, even in the case when the loss of delivered voltage, due to the output resistance, is high. However, this delivered voltage is very close to 1, more than the topology with a gain of 2/3, in order to make sure that the optimum frequency at normal load conditions, the output voltage is precisely 1V. This would avoid efficiency degradation to regulate better the output voltage. As seen from the section 2.7, the output voltage control is performed increasing the output resistance. To convert the two volts input to one volt output it is possible to use a DC-DC converter with a gain of 3/5. As seen in the previous chapter to get a switched capacitor DC-DC converter with CR equal to 3/5 must use at least three flying capacitors.
Applying the charge balance analysis:

$$3C_f(V_{in} - V_o) = Q_{out} - C_f \cdot V_o - 2 \cdot C_f \frac{V_o}{2} \tag{3.17}$$

If $Q_{out} = 0$, then

$$3C_f V_{in} = 5C_f V_o \quad \Rightarrow \quad \frac{V_o}{V_{in}} = \frac{3}{5} \tag{3.18}$$

While, the vectors $a_{c,i}$ and $a_{r,i}$ was calculated by means a charge flow analysis:

$$a_{c,1} = [\frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}] \tag{3.19}$$

$$a_{r,1} = [\frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}\ \frac{1}{3}] \tag{3.20}$$

Then, for this topology, m=1/3 and p=7/9
The topology is shown in figure 3.12.

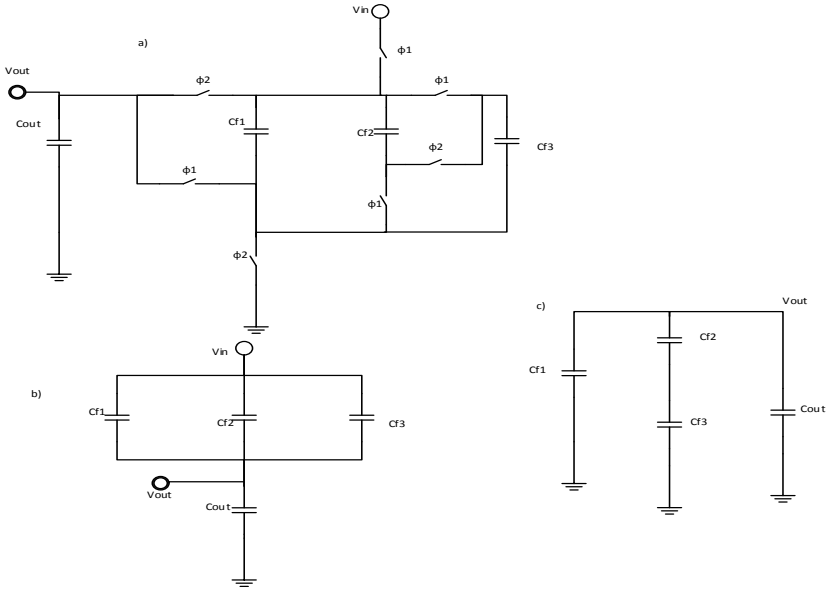

Figure 3.12: SC DC-DC converter with CR=3/5 with three flying capacitor. a) whole circuit b)charge circuit c)discharge circuit

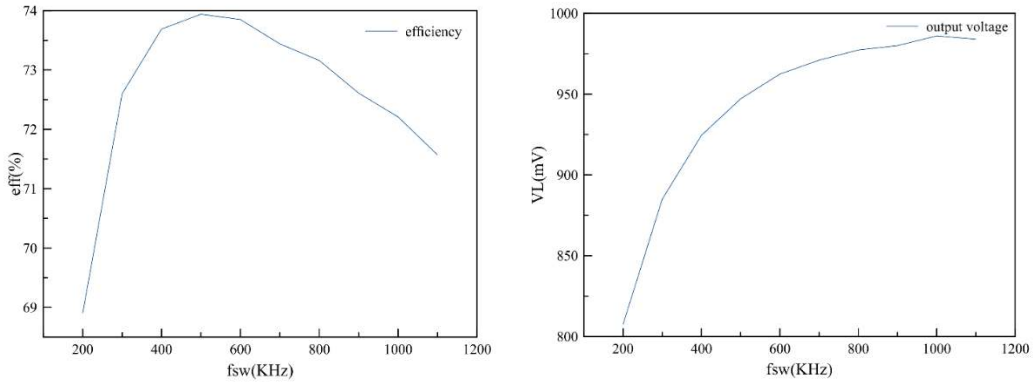

Figure 3.13: Efficiency and output voltage of the SC DC-DC converter with CR=3/5 with three flying capacitors by varying the switching frequency.

The measured output voltage is much less than the ideal (that with an input voltage of 2V should be 1.2V), while the maximum efficiency is reached at a frequency of 500 KHz and is equal to 74% (Fig 3.13).

3.5 Final Comparison

In this chapter, the figures of merit p and m were used to compare the different topologies of SC DC-DC converter. Referring to the table 3.4, we conclude that the best topology that shows the best performance is the 2nd one (CR=1/2 and only one flying capacitor).
We must also evaluate the dependence of the performances on the number of switches for two reasons:

1. in the case of a large number of switches the output resistance in the FSL, will be larger
2. the load capacitance of the drivers will be higher.

Moreover, if the topology has fewer on-chip capacitors, it is possible to use a larger capacitance on the same area, leading to an higher efficiency.
Although, we have numerically shown the superiority of the 2nd topology, this topology is not able to provide a 1V output voltage. In particular, for normal load conditions (Rout = 100KΩ) the delivered voltage is 968mV. While, in the presence of high currents (Rout=50KΩ) or when the input voltage drops below 2V, it may not provide a sufficient output. In the case when an output of 1V is needed, we show the best solution in column 3 of Table 3.4

Table3.4. Comparison of the surveyed topologies

	1/2 with 2 flying capacitors (1°)	**1/2 with 1 flying capacitor (2°)**	**2/3 with 2 flying capacitors (3°)**	**2/3 with 3 flying capacitors (4°)**	**3/5 swith 3 flying capacitors (5°)**
Conversion Ratio	1/2	1/2	2/3	2/3	3/5
Number flying capacitors	2	1	3	3	3
Number switches	5	4	7	8	7
m factor	1/2	1/4	2/9	2/3	1/3
p factor	5/4	1	7/9	20/9	7/9
Efficiency max (withCf=50pF)	88.1%	91.17%	86.75%	70%	74.5%
Measured output voltage(input of 2V and Rout=100K)	903.5mV	968mV	1.197V	-	≈1V

Chapter 4

Output Voltage Control

This section includes the design of the output voltage control. The aim is to obtain an output voltage close to 1V, which is necessary for the biosensor. As seen in section 2.7, there are several ways to achieve this goal. Most of these are based on the modulation of Rout. In this Master thesis, we use a Pulse-Frequency-Modulation (PFM), which is particularly effective when the SC DC-DC converter works in SSL where the output resistance is proportional to frequency.

As shown in the figure 4.1, the output voltage is compared with a reference voltage by means of an OTA, whose output is the control signal V_{error} proportional to the error between the desired voltage and the true output voltage. That signal controls the bias current of a VCO, which is necessary to generate the clock with an appropriate frequency for driving the switches of the DC-DC converter.

As discussed in the section 1.1, to decrease the power dissipation of the control circuitry, instead of the 2V supply, 1V is used, which has been generated using another regulator. In fact, since the power dissipation of the control circuitry is very low, a power regulator with a moderate efficiency is sufficient.

Also necessary are other circuits such as the Level Shifter (LS), to allow the communication between 2V and 1V supply circuits, and the Non-Overlapping Clock (NOC) circuit.

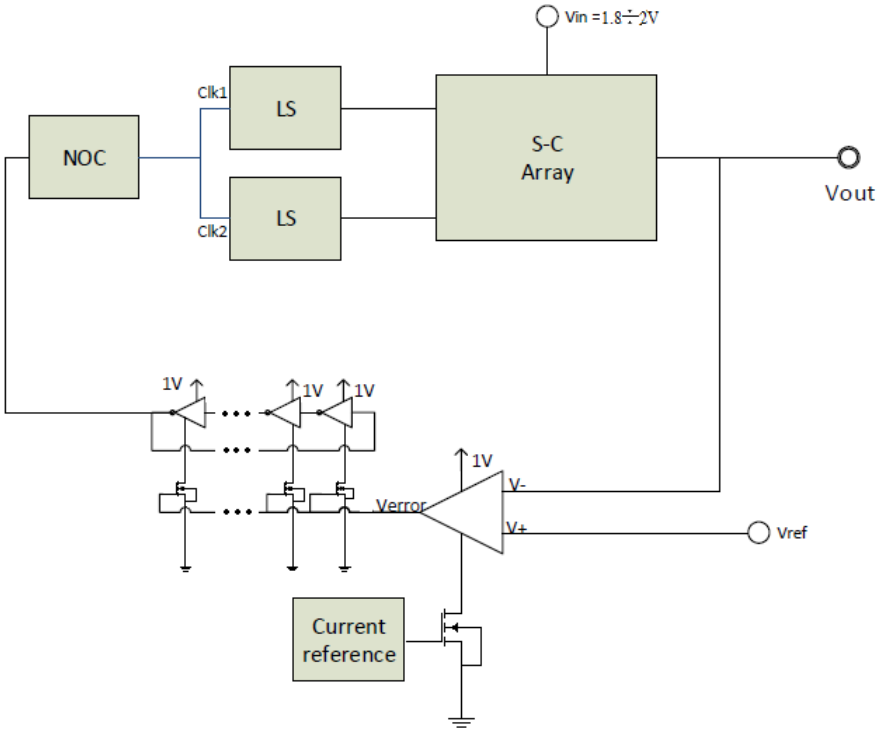

Figure 4.1: Schematic of the control circuitry

4.1 VCO

In slow-switching limit the output resistance is proportional to the frequency of the clock driving the switches. Therefore, to stabilize the output voltage the frequency of the generated clock must be controllable.
The voltage-controlled oscillator (VCO) is based on a ring oscillator, which does not have the disadvantage of LC tank oscillator, such as the large overall area. Moreover the phase-noise, in the LC-oscillator, is strongly influenced by the quality factor of the on-chip inductor.
The ring oscillator is a cascade of an odd number of inverters, among them the last one has an output connected to the input of the first inverter (see figure 4.1). Then the clock frequency is:

$$f_{clk} = \frac{1}{n \cdot T} \tag{4.1}$$

Where T is the delay of a single inverter, and n is the number of the stages.
Usually the frequency is set by varying the number of inverters in cascade or by adding an extra capacitor, or, even, an RC filter at the input of each inverter to increase T. If you use the first method, for a low frequency as 1MHz, with the technology used, would be needed tens of thousands of inverters with minimum dimensions. Therefore, this method is not the most appropriate; on the other hand, adding a capacitor too large at the input of each inverter involves a too high power dissipation.

The paper [34] proposes the use of inverters with a W minimized and a high gate-length to reduce the power dissipation by the reduction of crossconductance currents (when both the PMOS and the NMOS conduct). Therefore, the delay T is set by the choice of gate length. Moreover, due to the lower current the delay of each stage is higher, then, the number of the stages is lower, leading to several benefits. The paper [35] [36] and [37] propose the current starved ring VCO. The current flowing in each inverter, therefore, it is limited by a current source in series with the PMOS or the NMOS or both. We have used the last architecture, shown in figure 4.2. Thus, the power dissipation is reduced by biasing the circuit with a very low current (40-50 nA) and the delay T is set to an appropriate value by varying either the bias current and the capacitors at the input of each inverter. This architecture also allows the control of the frequency of the generated clock thanks to a voltage controlling the bias current(Fig.4.2).
The period of the generated clock is:

$$T = \frac{C_p V_{DD}}{I_{BIAS}} \tag{4.2}$$

Where the bias current can be calculated as:

$$I_{Bias} = \frac{1}{2} K_1' \frac{W_1}{L_1} [V_{ctrl} - I_{BIAS} R_d - V_{thn}]^2 \tag{4.3}$$

Combining the two expressions (4.2) and (4.3), it is possible to find out the frequency of the generated clock:

$$f_{ck} = \frac{1}{NT} = \frac{1 + K_1' \frac{W_1}{L_1} R_d (V_{ctrl} - V_{thn}) + \sqrt{1 + 2K_1' \frac{W_1}{L_1} R_d (V_{ctrl} - V_{thn})}}{N C_p V_{DD} K_1' \frac{W_1}{L_1} R_d^2} \tag{4.4}$$

Where W1 and L1 are the dimensions of the MOS M1(see the figure 4.2).

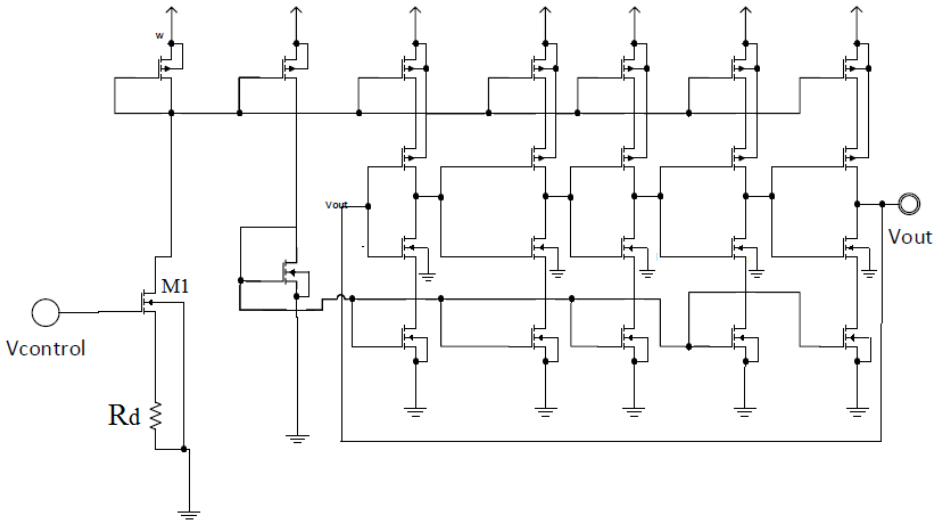

Figure 4.2: VCO architecture

The resistance R_d allows a linearization of the function $f_{ck}(V_{ctrl})$. Effectively, if the mosfet M1 is very large, the value of its Vgs is enough close to the threshold voltage. Moreover, since $V_{ctrl} - V_{gs} = R \cdot I_{Bias}$ and from the equation (4.1), the bias current is a linear function of the control voltage. Also the frequency of the clock is a linear function of the control voltage (Fig. 4.3).
The power dissipated by the VCO is equal to the sum of the power dissipated by each inverter:

$$P_{diss} = N \cdot f_{sw} \cdot C \cdot V_{DD}^2 \tag{4.5}$$

The power dissipation is reduced by decreasing the bias current of each stage. For instance, with 1V supply voltage, the power dissipated by the VCO, when it generates a 1.2MHz clock is around 100nW. The frequency of the clock has been calibrated by changing the load capacitance of each inverter. It is chosen in such a way the maximum frequency of the generated clock is 1.7MHz (when the control voltage is 1V). If we use a high switching frequency, as shown in the previous chapter, the output voltage of the SC DC-DC converter would not rise anymore, while, the efficiency will decrease. This would be a problem in case the output of the OTA saturates.

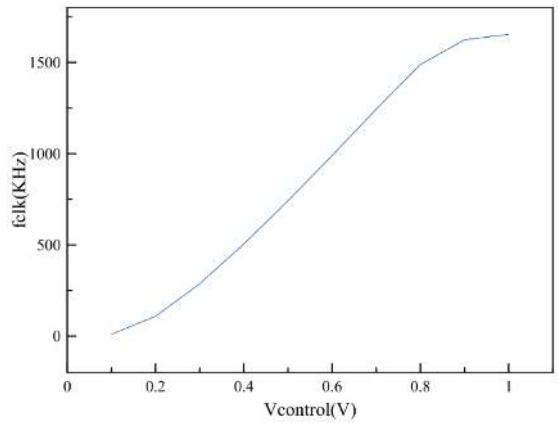

Figure 4.3: Relationship between Vcontrol and frequency

4.2 OTA

To drive the VCO you must generate an error signal. It is proportional to the difference between – output voltage achieved by the DC-DC converter and a reference voltage, which is close to 1V.
Since the output is capacitive, the amplifier can have a high output impedance, so it will be an OTA (Operational transcondutance amplifier). The requirements, that it must fulfill are:

- Low power consumption (less than 50nW)
- High DC Gain(if the gain is larger, the output of the DC-DC converter will be closer to the reference voltage, in particular a gain of 40dB is acceptable, in fact the amplifier output has a swing of 1V, therefore, with only 10mV at the input, it will saturate)
- High swing (a swing between 250mV and 1V is sufficient)
- Stability

To meet these specifications is sufficient a single stage differential amplifier with a load in the mirror (Fig 4.4).
The mos amplifiers are biased with a very low current (17nA see paragraph 4.3), and so, in weak inversion to reduce the power consumption. Therefore, this amplifier consumes a negligible power respect to the total power consumed by the control.
In order to analyze this circuit, we use the EKV model described in [4] and in [8] according to which, the current, in weak inversion, is equal to:

$$\mathrm{I}=I_F - I_R = I_S \cdot \exp[\frac{V_P}{U_T}]\{\exp\left[-\frac{V_S}{U_T}\right] - \exp[-\frac{V_D}{U_T}]\} \tag{4.6}$$

Where I_S is equal to:

$$I_S = 2n\mu C'_{ox}\frac{W}{L}U_T^2 \tag{4.7}$$

While:

$$V_P = \frac{V_G - V_{TO}}{n} \tag{4.8}$$

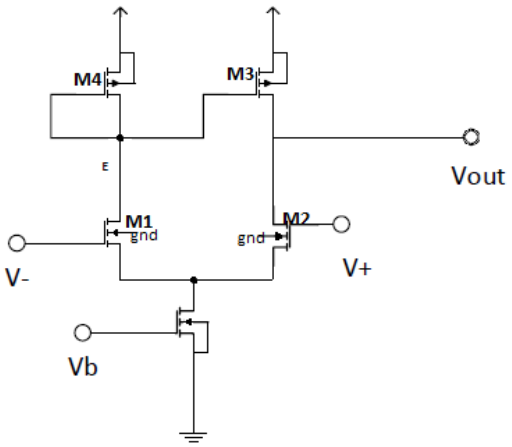

Figure 4.4: Schematic of the OTA

In the circuit there are five MOS Transistors, however, some of these have the same size (respectively M1-M2 and M3- M4) to obtain symmetry. Moreover, to avoid the problems of mismatch, L and W have been kept more than 1um for the MOS Transistors M1 , M2, M3 and M4 and to the current source M0 and M5.
As already said, the bias current is provided by the current reference (and it is equal approximately to 17nA).
The MOS M1 and M2 are sized according to the $\frac{g_m}{I_D}$ method [43] [45] valid in the entire operation region. Reference [45] calculates the relationship between the ratio $\frac{g_m}{I_D}$ and the normalized I_D $(\frac{I_D}{(W/L)})$. In particular, in the weak inversion [43] [8], the ratio $\frac{g_m}{I_D}$ is approximately constant as the normalized I_D increses and it is equal to $\frac{1}{nU_T}$. The ratio $(\frac{g_m}{I_D})_{1,2}$ influences the gain of the circuit [45], then that is independent of W, but only depends on the gate-length, through the output resistance of the circuit:

$$A_o = g_{m1,2} \cdot r_{outn} \,//\, r_{outp} = (\frac{g_m}{I_D})_{1,2} \cdot V_{AN} \cdot L_N \,//\, (V_{AP} \cdot L_P) \qquad (4.9)$$

Where V_{AN} and V_{AP} are the Early voltages of PMOS and NMOS.
The gain depends mainly on the two gate-length. Therefore, the dimensions W1 and W2 are chosen as small as possible to move the pole, due to the parasitic capacitance on node E, in the figure 4.4, to the highest frequency. At same time, the aspect ratio must be enough large, in order to keep the transistors in weak inversion, where $\frac{g_m}{I_D}$ reaches the maximum possible value.
The transistors M3 and M4 are needed only to replicate the current of a branch in the other, and then, also W3 and W4 are as small as possible to avoid the increase of the parasitic capacitance on the node E. On the other hand, the gate-lengths are chosen to obtain a gain of about 40 dB (Formula 4.9).

Once the current I_D is chosen, the dimension of the current mirror M0 are selected. The current influences the power dissipation and also the slew rate. In particular, the slew rate is given by:

$$SR = \frac{I_D}{C_L} \tag{4.10}$$

The circuit has been stabilized with an output capacitance (CL = 20fF). If it is not sufficient and the phase margin is less than 60 degrees, the output capacitance can be increased, worsening the cut-off frequency. Also the non-dominant pole on the node E, in figure 4.4, can be increased re-sizing the MOSFET M1, M3 and M4.
In the bode plot, he output pole is situated at:

$$f_{Tout} = \frac{1}{2\pi(r_{outn} \,//\, r_{outp})C_L} \tag{4.11}$$

While the parasitic pole:

$$f_{TE} = \frac{1}{2\pi(\frac{1}{g_{m1}})C_E} \tag{4.12}$$

Where C_E is the parasitic capacitance on the node E in figure 4.4.
In the Bode plot (Fig. 4.5) we can be seen how the frequency of the dominant pole (output node ie the cutoff frequency, is located at the frequency 10KHz and the Phase margin is sufficient (Table4.1).

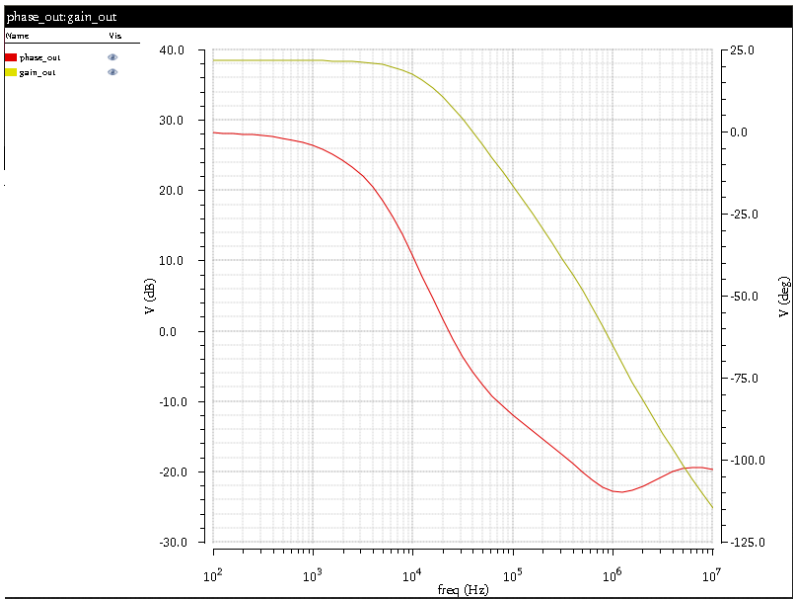

Figure 4.5: Bode plot (magnitude and phase)

Table 4.1: Features of the OTA

DC Gain	38.5dB
UGB	42.33KHz
CL	20fF
PM	71.45°
Slew rate	875V/ms
Output Swing	[155mV,1V]
Power Supply	1V
Power dissipation	20nW

4.3 Current Reference

The OTA needs to be biased by a current source of 17nA. In addition to the classic features of immunity to power supply noise (PSRR), it must have a negligible power consumption(<100nW) .
The conventional source reference is the self biased circuit source (SBCS) shown in Fig.4.6 It is based on a double current mirror, therefore the current in the left branch is equal to the current in the right branch. Usually the value of current is fixed thanks to a resistance of one of the two branches.

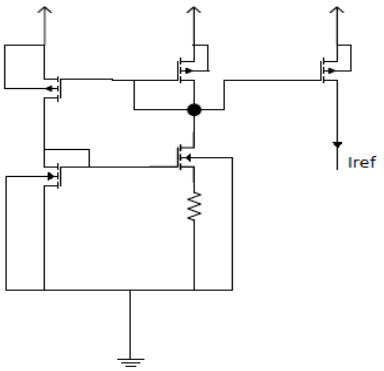

Figure 4.6: Conventional current source

The works [38] uses, for the current reference, long devices to reduce the effect of the threshold variation with the process, in fact, it is slightly constant if the channel longer than 1 µm. In the work [47] a MOS working in the triode region has been used instead to resistor, which, for achieve very low current, must be large. The current reference presented in [46] and in [48] use the self-cascode MOSFET (SCM) shown in figure 4.7. It works in moderate inversion and its intermediate node X of the SCM, in [46] is biased by an SBS(self-bias structure). For the calculation of the drain current of the mos M1 and M2 and further details refer to [46] and [49]:

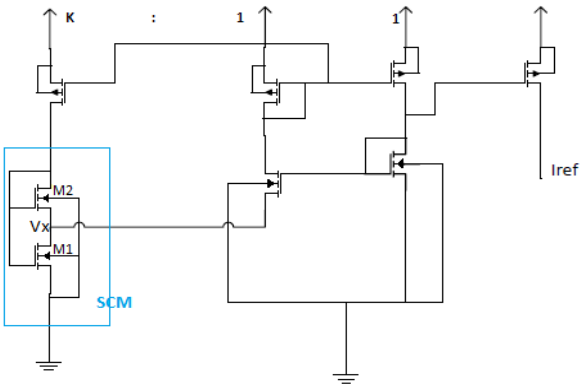

Figure 4.7 SCM+SBS(whole circuit)

In this Master thesis, a conventional current reference, with a supply of 1V, has been used (Fig. 4.8). To reduce the effect of channel modulation the NMOS mirror has been designed cascode. Applying Kirchhoff's laws to the loop M1-M2-Rs, we have:

$$V_{GS1} - V_{GS2} = R_S I \tag{4.13}$$

Since M1 ed M2 are biased in weak inversion, the relationships mentioned in the paragraph 4.2 are valid:

$$I_{D1,2} = I_{S1,2} \cdot \exp[\frac{V_{GS1,2}-V_{TO}}{U_T}]\{1 - \exp[-\frac{V_{DS1,2}}{U_T}]\} \tag{4.14}$$

Dividing the currents with each other:

$$\frac{1-\exp[-\frac{V_{DS2}}{U_T}]}{1-\exp[-\frac{V_{DS1}}{U_T}]}\frac{I_{D1}}{I_{D2}} = \frac{I_{S1}\cdot\exp[\frac{V_{GS1}-V_{TO}}{U_T}]}{I_{S2}\cdot\exp[\frac{V_{GS2}-V_{TO}}{U_T}]} \tag{4.15}$$

Since $I_{D1} = I_{D2}$, by setting $L_1 = L_2$, and approximating $\frac{1-\exp[-\frac{V_{DS2}}{U_T}]}{1-\exp[-\frac{V_{DS1}}{U_T}]}$ to 1:

$$V_{GS1} - V_{GS2} = U_T \ln(\frac{W_2}{W_1}) \tag{4.16}$$

By substituting the expression 4.4.1, we have:

$$I_{out} = \frac{U_T \ln(\frac{W_2}{W_1})}{R_S} \tag{4.17}$$

If W_2 is chosen two times W_1, the current flowing in both the branches is setted by the resistance R_S.

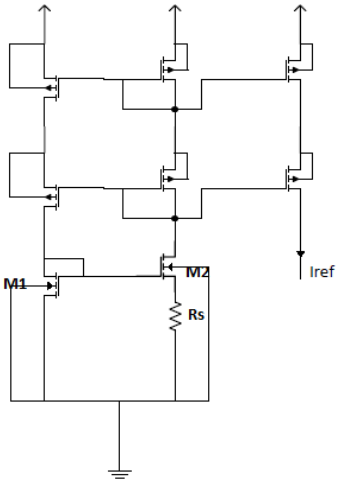

Figure 4.8: Used current source

4.4 Level Shifter

The level shifter is used for chips having some parts with different supply voltage to allow the communication between those parts.
Since the VCO has a 1V supply voltage, it generates a clock ranging from 0V to 1V, while the maximum voltage in the dc-dc converter is 2V. If we use that clock, the step-down converter would be led to a malfunctioning. Because of this reason, the level shifters are required to shift the clock from 1V to 2V and to drive the switches connected to the input voltage.
In some work, [32] and [33], the clock that drives these switches (M1 and M2 in the figure 3.5) is ranging from 1V (ON-state) to 2V (OFF-state); then the range of the gate voltage is reduced to one volt in order to avoid to exceed the oxide break down voltage ([32] uses a 32nm technology). The technology of 180nm, used in this master thesis, has not the same problems of oxide breakdown below 2V.

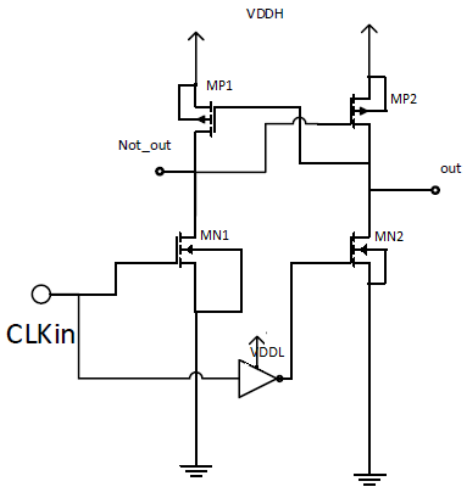

Figure 4.9. Architecture of the level shifter

The conventional level shifter, shown in the figure 4.9, is based on a SRAM cell [55-61] [26]. When the input is VDDL, MN1 is on and MN2 is off. Thus, the node NOT_OUT drops to zero and MP2 is turned on. Then, the node OUT is pushed to VDDH, turning off MP1.
The problem of this circuit is that the output nodes are driven by both the NMOS and the PMOS. For instance, focusing on the left branch, if the current of MP1 (see the figure) is larger than that of MN1, the node NOT_OUT cannot drop to zero. Therefore, the MOSFET must be sized appropriately. Furthermore, this circuit cannot be used for subthreshold logic, because the current of the NMOS transistors in weak inversion is much smaller than that of PMOS.
The output clock in the conventional shifter varies from 0 volt to VDDH while in the work [56] and [26] two clocks were generated, the first from 0 to VDDL, the second from (VDDH-VDDL) to VDDH.

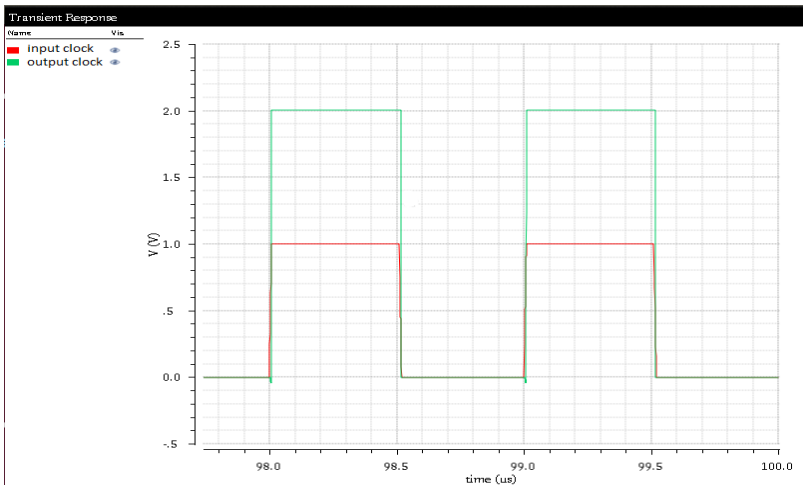

Figure 4.10. Input signal(red) and output signal(green) of the level shifter

4.5 Non-Overlapping Clock Circuit

Due to the non-zero rise and fall time and of the clock and its skew and jitter, both phase may be zero at the same time, hence, in the SC converter the output node may be short-circuited with the input node, then it is necessary to design a non-overlapping clock.
The block diagram is shown in figure 4.11[50-53].

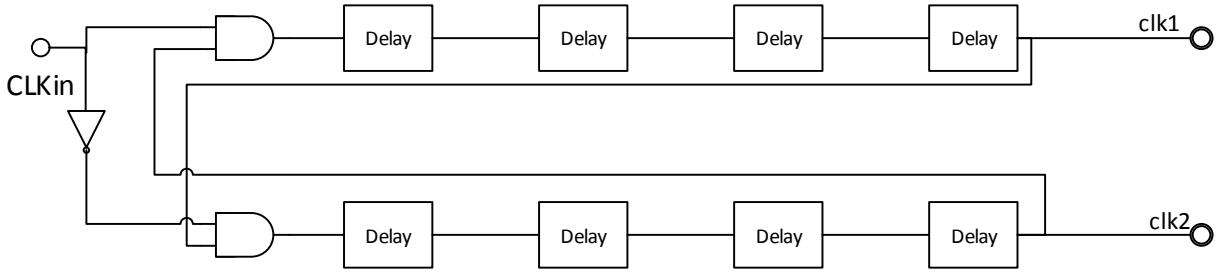

Figure 4.11: Non-overlapping clock diagram

The delayed clock will be an input of the NAND, while, the other input is the not clocked. When both signals are equal to zero, the output of the NAND is one, otherwise, the output signal will be equal to zero.

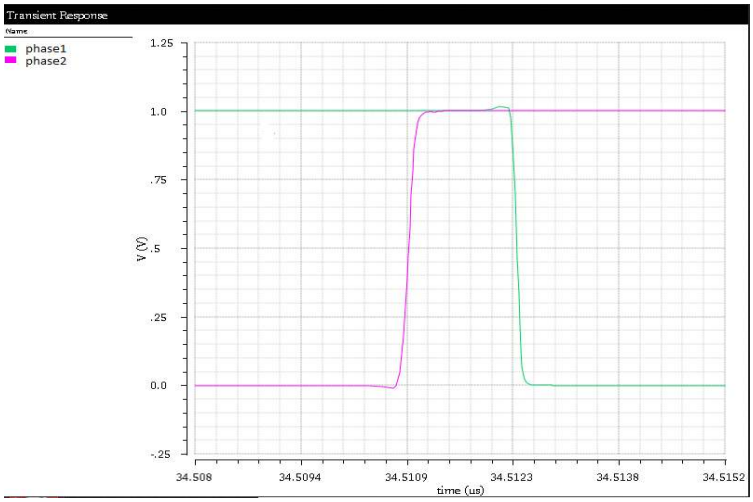

Figure 4.12: Non-overlapped clocks. Note that those clock drive PMOS, which are on when the clock is low.

In order to create the delayed clock, the Ref. [50] listed and compared some possible delay element:

- *The transmission gate*. It provides a delayed signal of 1ns. One of its advantages is that the signal input and output are connected to the source or drain, while, the positive and negative supplies are connected to the gates of the two MOS transistors, leading to a low power consumption. The disadvantage is the significant deterioration of signal integrity. This delay element is also used in [51]
- *Cascaded inverters*. It provides delay of about 1-3ns, with a better rise and fall time of the output signal. On the other hand, it consumes a power higher than the transmission gate. Both, the transmission gate and the cascaded inverters have a small area occupied.
- *Tryristor* is used for large delays (from 2.6ns to 76ms). The disadvantage are the power dissipation and the high occupied area.
- *Voltage-controlled delay element.* It is a cascade inverter with a NMOS as active load, which is need to make the delay controlled from the outside. The features are similar to the cascaded inverters but the signal integrity is worsened.
- *Transmission gate cascaded with Schmitt trigger.* The delay and the signal integrity are better than the transmission gate, however, the area and power dissipation are comparable with the other elements.

It is also possible to use, as delay element, an inverter followed by a RC filter to slow down the signal, however, the dissipation would be too high.
Other tests have been done simply using a cascade of inverters or a transmission gate, as delay element, cascade with an inverter, to improve the signal integrity.

The efficiency obtained by the dc-dc converter all the types of non-overlapping clock have been compared. The lowest power dissipation is obtained by using as a delay element only the transmission gate (the circuit, however, is followed by two inverters needed to improve the signal integrity). The simulation was performed with a divide-by-two with one flying capacitor of 25pF, and with a gate width of 4µm, and supplying the NOC circuit with 1 Volt. Then the level shifter presented in the previous section is needed to shift the level of both clock from 1V to 2V. Indeed, you have two choices:

1) The NOC may precede the level shifter (which should be two, one for either the non-overlapping clocks)
2) The NOC could follow the level shifter (and then be fed to 2Volts).

Simulations has confirmed that the first choice is more advantageous in terms of power consumption.

Note that, if the area of the driven MOS is large, an inverter sizing is needed. You can calculate the capacitance of the output of the non-overlapping clock circuit (the sum of the gate capacitance of the switches) with a DC simulation with virtuoso ADE (tools-> result browser -> dcOpInfo-info). This allows to easily size any buffer, in such a way they have the same fan-out. For example, if we use 8 inverters the fan out of each inverter must be the same for every stage, i.e.:

$$Fan\text{-}out = \sqrt[8]{F} = \sqrt[8]{\frac{C_L}{C_{in}}} \tag{4.18}$$

This calculation is only useful when you want to control the capacitance more than 10^{-14}F, i.e. when the width of the driven switches is very high.

In the figure 4.12, you can note that, after the phase change, there is a small overvoltage or undervoltage. This is due to the opening of the MOS-switch, when the charge under the channel is injected in both directions and it is positioned on the output capacitor, however if the overvoltage does not exceed the threshold voltage, that is not a problems. Furthermore, the designed circuit, at the output, provides also the phase not_φ_2, which is useful to drive any NMOS.

4.6 Final Simulation Results of the Complete System

Once each block is designed, the whole system can be built according to the figure 4.1. The chosen solution is to use the DC-DC converter with a conversion ratio equal to ½ and only one flying capacitor, which can achieve the highest efficiency, but an output voltage which is lower than 1V. Therefore, if that output voltage is not high enough for our application, we could use the DC-DC converter with a conversion ratio equal to 2/3.

Four simulations are presented on the first converter. The first one has a current demand of 9 µA. In this simulation the voltage reference is set at 960mV. In this way, the SC DC-DC converter works at the optimum frequency (1.2MHz) where the efficiency of the system is 94% as provided in the simulation of the previous chapter.

The second simulation (Fig.4.13) was performed with a reference voltage of 930mV while the output resistance is equal to 50KΩ, in order to verify the behavior of the circuit in case of high current required by the load. The voltage Vref is set equal to 930mV because the losses of the delivered voltage caused by the output resistance of the converter are doubled. Another simulation (Fig 4.13) was performed with low output currents (9.3uA) but with a reference voltage of 930mV in order to see the behavior that would have the converter in the case of low output currents with a reference voltage that we are going to use (930mV). The converter works with a frequency lower than the optimal one, and then it has a lower efficiency.

In the case where the input voltage drops from 2Volts to 1.8 Volts also the output fall to 90% of the previous value (968mV) and then in the case of low currents, the maximum delivered voltage will be $968mV \cdot 9/10 = 871.2mV$ as seen from the simulations (table 4.2). The table compares the efficiencies of the circuit for various load conditions and the reference voltage.

In conclusion, if you want to use this topology, the Vref should be set at 900mV, otherwise, for high current demands and for low input voltage, the DC-DC converter fails to reach the request output voltage.The maximum efficiency achieved is 93 .65%.

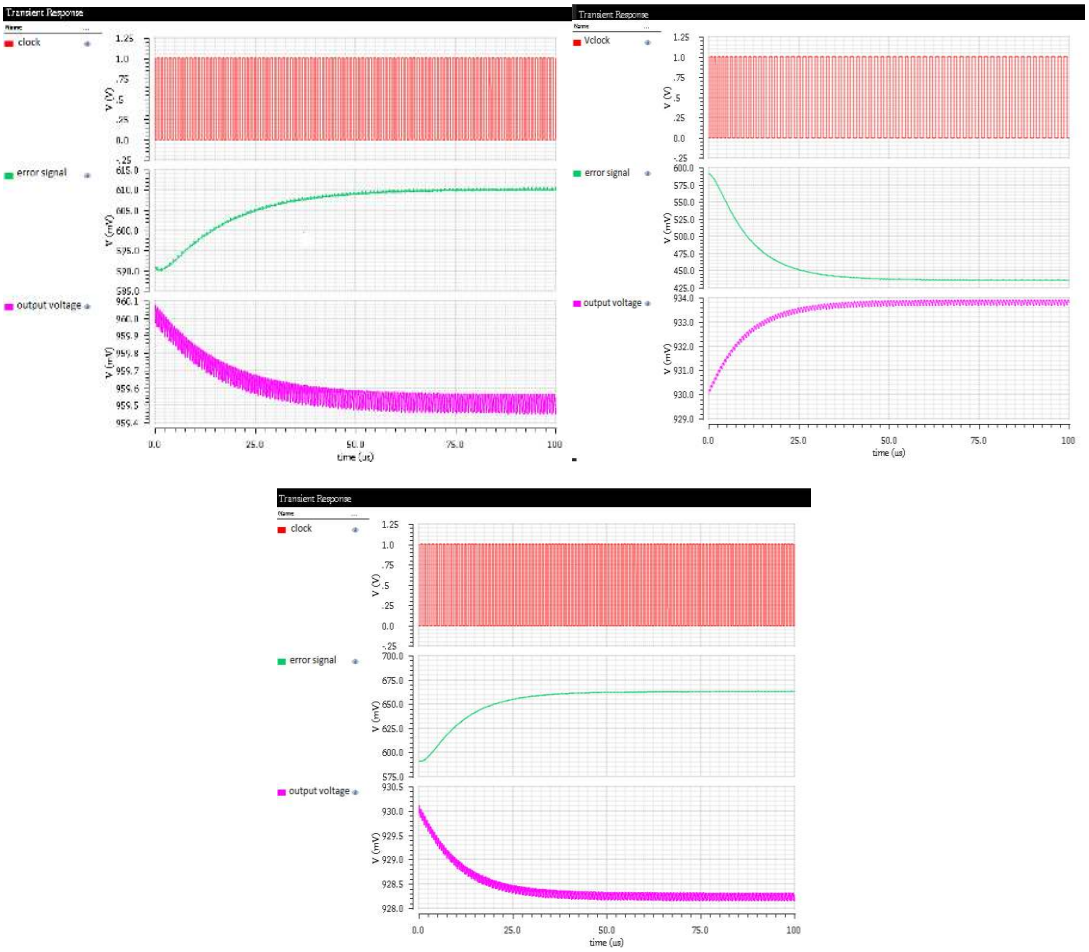

Figure 4.13: Simulation for different load current and reference voltage

Table 4.2. Power dissipation of the DC-DC converter (with the CR= 1/2)

Vref	Vout	Vin	IL	Pin(2V)	Pcontrol(1V)	Pout	Eff
960mV	960mV	2V	9.60µA	9.873µW	262nW	9.247µW	93.65%
930mV	930mV	2V	9.30µA	9.676µW	193.4nW	8.755µW	90.48%
930mV	930mV	2V	18.6uA	19.05µW	230nW	17.26uW	90.6%
900mV	871mV	1.8V	8.7uA	8.299uW	371.3nW	7.59uW	91.44%

The load regulation and line regulation of the converter are tested and the results are shown in plots 4.14 and 4.15. When the output current varies from 9µA to 18µA (at 30µs), the output voltage remains almost the same (decreases by about 5mV). The curve in green is the error signal that controls the frequency of the generated clock. It is higher in case the output distances from the reference voltage. This is sufficient for the VCO, which will generate a clock at a higher frequency. In particular, referring the graph Vcontrol-Fck, a control voltage of 625mV leads to the generation of a clock of 1MHz.
The behavior is similar to a variation of input voltage from 2 volts to 1.9 volts. The error signal increases leading to higher frequency of the clock. The output voltage remains almost constant.

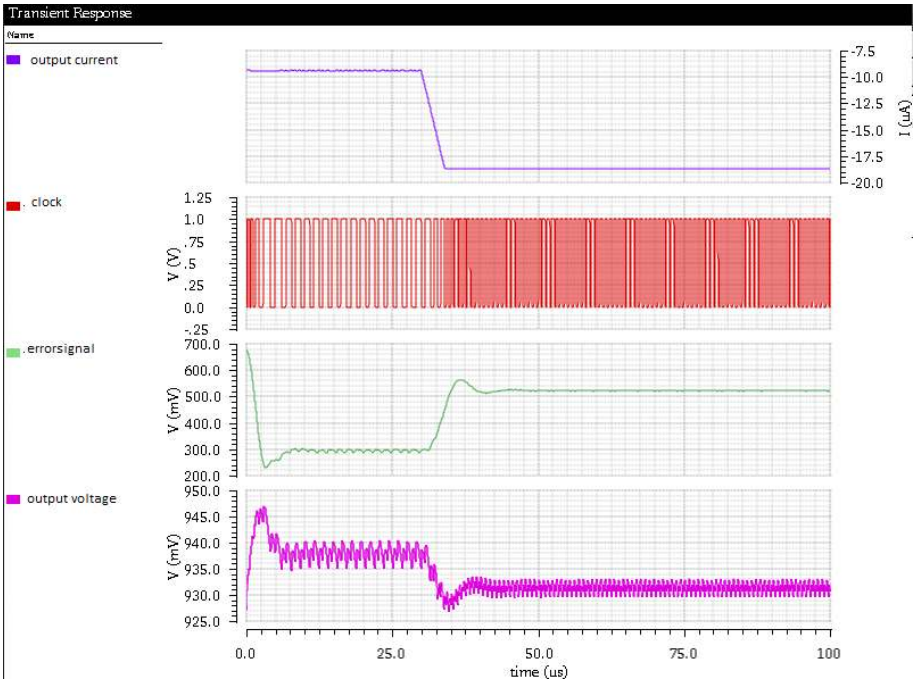

Figure 4.14: Test for the load regulation of the circuit. Vcontrol(green),Vclk(red), Vout(purple)

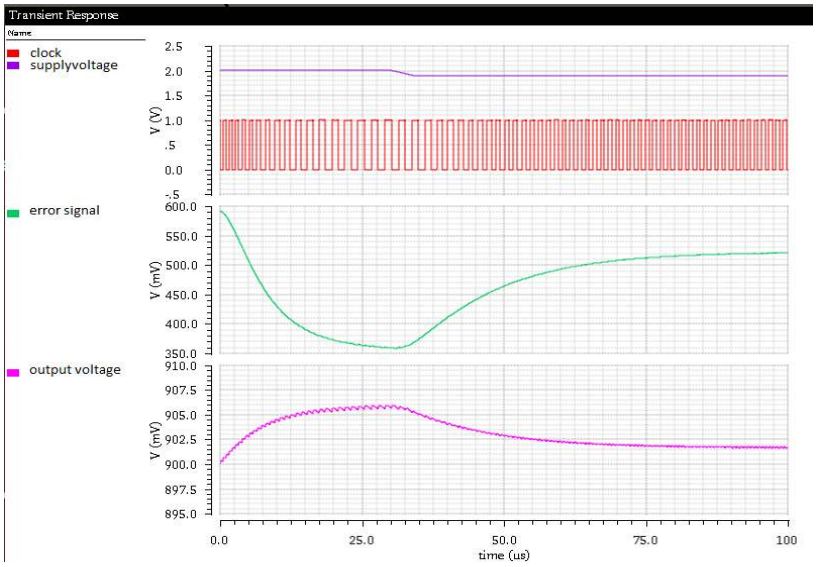

Figure 4.15: Test for the line regulation of the circuit. The input voltage varying from 2Voltsto 1.9Volt. Vcontrol(green),Vclk(red), Vout(purple)

In the case when the output voltage must be compulsorily equal to 1V, you must use a voltage converter with conversion ratio higher than (2/3 or 3/5).
Among them the greater efficiency is reached by the SC DC-DC converter with CR = 2/3 and with only one flying capacitor (peak efficiency of 87%). Its behavior, in various conditions, is represented in the table 4.3, while, the load and line regulation in the figures 4.16 and 4.17.

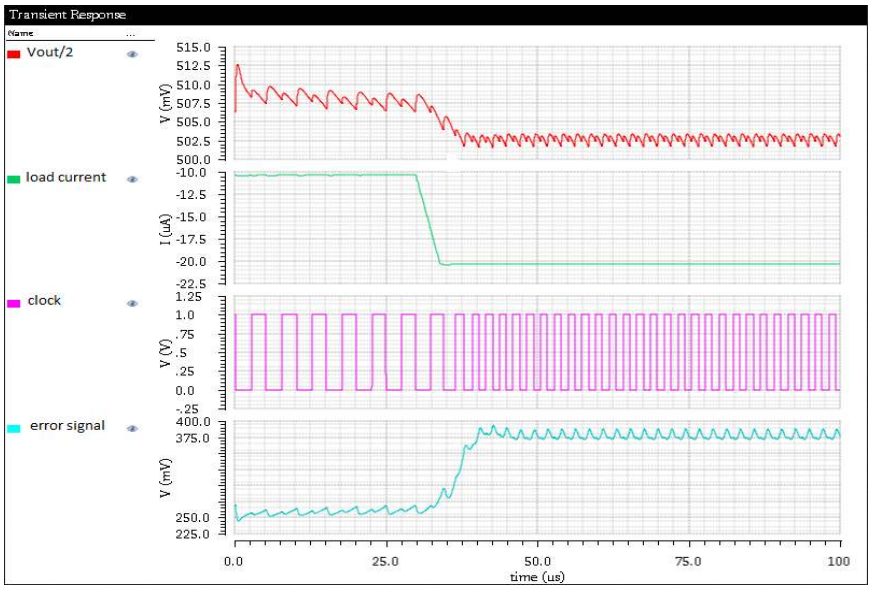

Figure 4.16: Test for the load regulation of the DC-DC converter with a gain of 2/3. Output current(green), generated clock(purple), Vcontrol(cyan blue), output voltage(red)

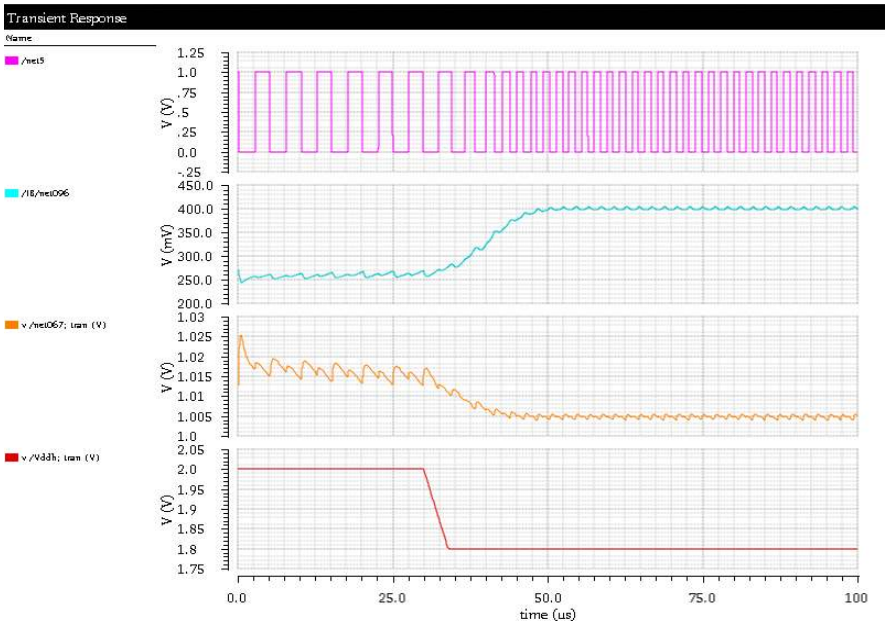

Figure 4.17: Test for the line regulation of the DC-DC converter with a gain of 2/3. generated clock(purple), Vcontrol(cyan blue), input voltage(orange), output voltage(yellow)

Table 4.3: Power dissipation of the DC-DC converter (with the CR= 2/3)

Vref	Vin	IL	Pin(2V)	Pcontrol	Pout	Eff
1V	2V	10uA	14.18uW	122nW	10.56uW	74.47%
1V	2V	20uA	27.64uW	163.9nW	20.48uW	74.1%
1V	1.8V	10uA	12.71uW	170nW	10.36uW	81.51%
1V	1.8V	20uA	24.25uW	338nW	19.98u	82.39%

Chapter 5

Layout Design and Post-Layout Simulation

In the simulations presented in the previous chapters, many physical parameters have been neglected, e.g. the parasitic resistance and capacitances of the interconnections. Once we take into account these quantities, the performance of the circuit may decrease and become unsatisfactory. In this chapter, we investigate the most critical blocks, namely the OTA, the SC-array and the VCO.

5.1 Layout of the OTA

The phase margin of the OTA can vary and consequently it can make the system unstable. To check that, the layout of the amplifier has been designed, and the parasitics have been extracted. We note that the Bode plot is approximately the same respect to the pre-layout simulations (Figure 5.2) In fact, the cutoff frequency is changed from 13.08KHz to 12.76KHz, while the phase margin from 71.45 to 71.02 (Figure 5.2). Therefore, the stability was not compromised at all. As can be seen from the layout (Figures 5.1), the area of the OTA is not a problem in the calculation of the total area since it is much smaller than that of SC-arrays.

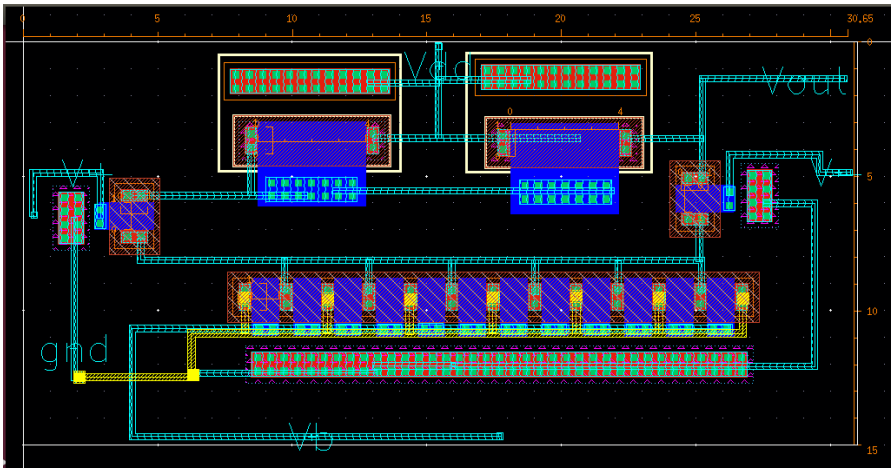

Figure5.1: Layout of the OTA (30µmX15µm)

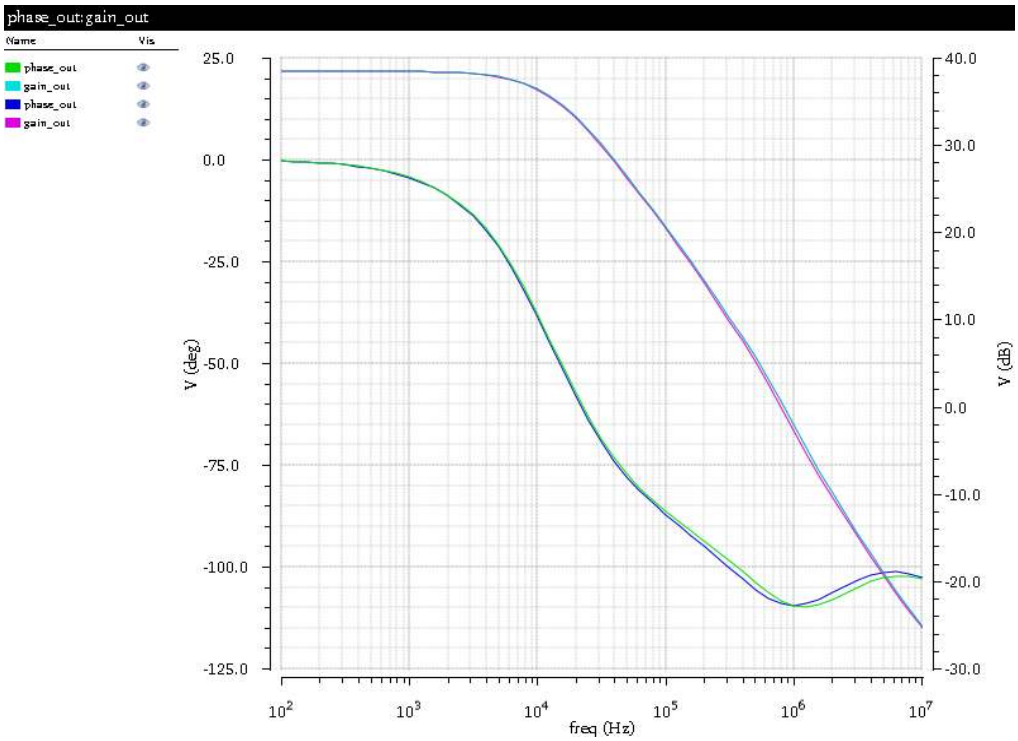

Figure5.2: Comparison layout vs schematic of the bode plot

5.2 Layout of the SC-Array

In the SC arrays the resistance of the wires and the series resistance of the flying capacitors is included in the model. They have been added to the resistances of the switches in the calculation of R_{FSL}, as explained in [3].
The resistance of the wire must be negligible compared to the on-resistance of the switches (in particular to the lowest among them). The latter resistance depends on the bias point of the MOS, which varies over time. For example, in the divide-by-two circuit with one flying capacitor the on-resistances in the best case (when they are lowest in the time) are listed in table 5.1.

Table5.1: Operating point of the switches

Mosfet	|VGS|	|VDS|	RON
M0	967.8mV	967.8mV	788Ohm
M1	974mV	1V	788Ohm
M2	2V	1V	383.2Ohm
M3	2V	969.3mV	198.7Ohm

Therefore, the total resistance of the two wires that connect the capacitor to switches (as shown in the figure 5.4 they are the longest) must be much smaller than 198.7Ohm.

In order to calculate the resistance of the two lines we may use the table5.2, which shows the sheet resistance of metal for each level of used technology.
The longest line is designed in metal4 (sheet resistance of 0.03 $\Omega/\square$) and is approximately 500um long, therefore, if it has a thickness of 4um:

$$\frac{L}{W} = 125 \Rightarrow R = 0.03 \cdot 125 = 3.71\Omega \tag{5.1}$$

In the sizing of the wire, the electromigration was not considered, since the current flowing in the wires is very small (in the scale of 100μA). The switching losses represent another problem. Due to the addition of the parasitic capacitances of the wires, that are comparable to the gate capacitance of the switches, the driven capacitance increases.

Table5.2: Sheet resistances in the 180nm technology

Layer	Sheet resistance ($\Omega/\square$)
Diffusion(silicided)	3-10
Diffusion (not silicided)	50-200
Poly silicided	3-10
Poly not silicided	50-400
M1	0.08
M2	0.05
M3	0.05
M4	0.03
M5	0.02
M6	0.02

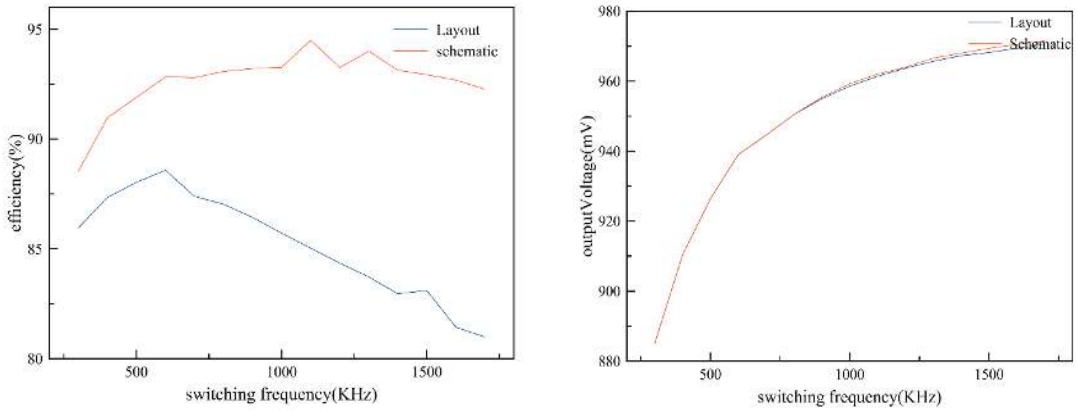

Figure5.3: Layout vs Schematic (output voltage and efficiency)

As you can see from Figure 5.3, the parasitic resistance of the wires does not affect the behavior of the circuit. In particular, since it affects R_{FSL}, and consequentially also affect the output voltage at high frequency, that fall of about 1.5mV (at a frequency of 1.7MHz). Since the parasitic capacitance on the gate of the switches, the switching losses increase considerably, leading to a degradation of the efficiency, that will be higher at high

frequency (worse than 10 percent than the pre-layout simulation). Thus, the optimum frequency will be much lower than the previous one, while the maximum efficiency is 88.5%.

The MOS Transistors are multifingered (Fig. 5.5) and we chose the finger's number as a result of a trade-off between resistance and parasitic capacitance of the gate. As the number of fingers increases, the W of each finger and the parasitic resistance of the gate decrease,while there would be a higher number of parasitic capacitances in parallel.

The total area of the switched capacitor is almost totally occupied by the capacitor (Fig. 5.4). In fact, the area of the circuit is equal to 68000 μm^2, while the capacitor occupies an area of 60000 μm^2.

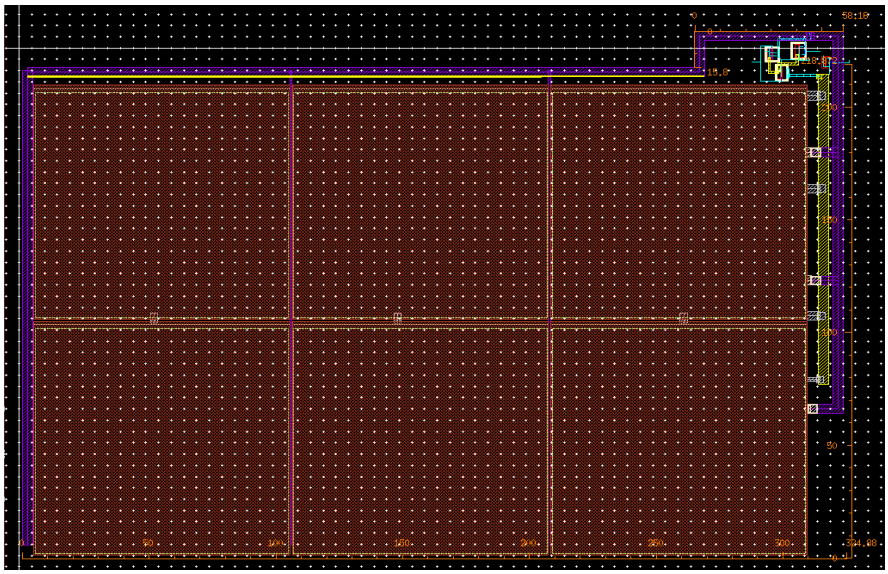

Figure5.4: Layout of the divide-by-two circuit

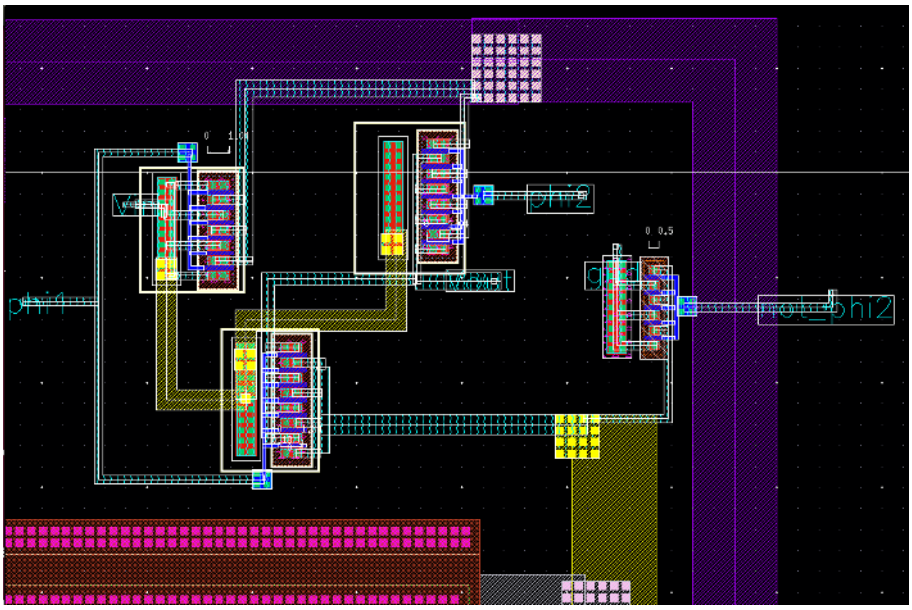

Figure5.5: Layout switches (50µmX15µm)

5.3 Layout of the VCO

The main problem in the realization of the oscillator is the variation of the oscillation frequency due to the parasitic capacitance of interconnections, which are added to the load capacitance of each stage, designed to achieve a desired frequency. Besides, the load capacitance, that has been chosen, is very low (3fF), comparable to the parasitic capacitances.

Therefore, the VCO has been modified increasing those capacities (it was brought to 26fF), so as to make the VCO insensitive to the addition of the parasitic capacitances. However, as shown in figure 5.6, they influence, although less strongly than before, the range(5.6).

To regain the same frequency range, however, we needed to increase the current drained from each branch, but, in this way, also the power consumption grows, or to modify the number of stages from five to three.

Furthermore, since the SC array, taking into account the parasitic parameters, has a much lower efficiency at high frequency, the range must be decreased. The VCO is able to generate a clock with the frequency 1,37KHz when the output of OTA saturates at 1V (see figure 5.6). You can note from the figure 5.6 that the linearity of the function Vcontrol-f_{sw} is enhanced by the enlargement of the MOSFET M1 of the VCO.

From the Layout (Fig. 5.7) we note that the area occupied by the VCO is equal to 1900µm^2, and that the load capacitor of the last stage is designed smaller than the others because it is summed with a parasitic capacitance larger than the other stages.

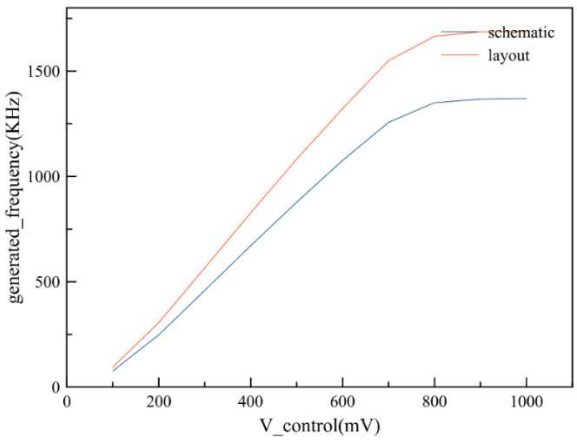

Figure5.6: comparison between the ranges of the VCO before and after the layout

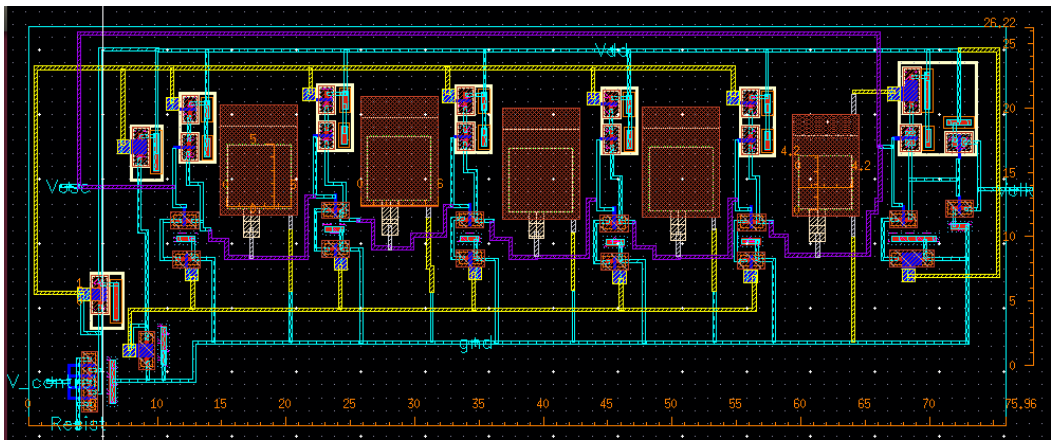

Figure5.7: Layout of the VCO (75µmX25µm)

5.4 Short summary

As can be seen from Figure 5.3, the efficiency of the converter (with CR = 1/2 and a flying capacitor) decreased by five percent due to increase of switching losses while losses of the control circuit are roughly the same. The peak efficiency is reached when the load current drains 9μA, the reference voltage is 900mV and the input voltage 2V. In those conditions the frequency of the driving clock is about 700KHz, the efficiency is 86.7%(Fig. 5.8), while the control losses are equal to 308nW. Those losses could be decreased using a VCO with three stages instead of five. The maximum output current is 40μA when the input is 2V and 24 μA when the input voltage is 1.9V, after those values the converter cannot still provide the desired output voltage (900mV). That efficiency could be improved by decreasing the gate capacitances of the switches (and approach, in this manner, the ideal value of 91.3%).

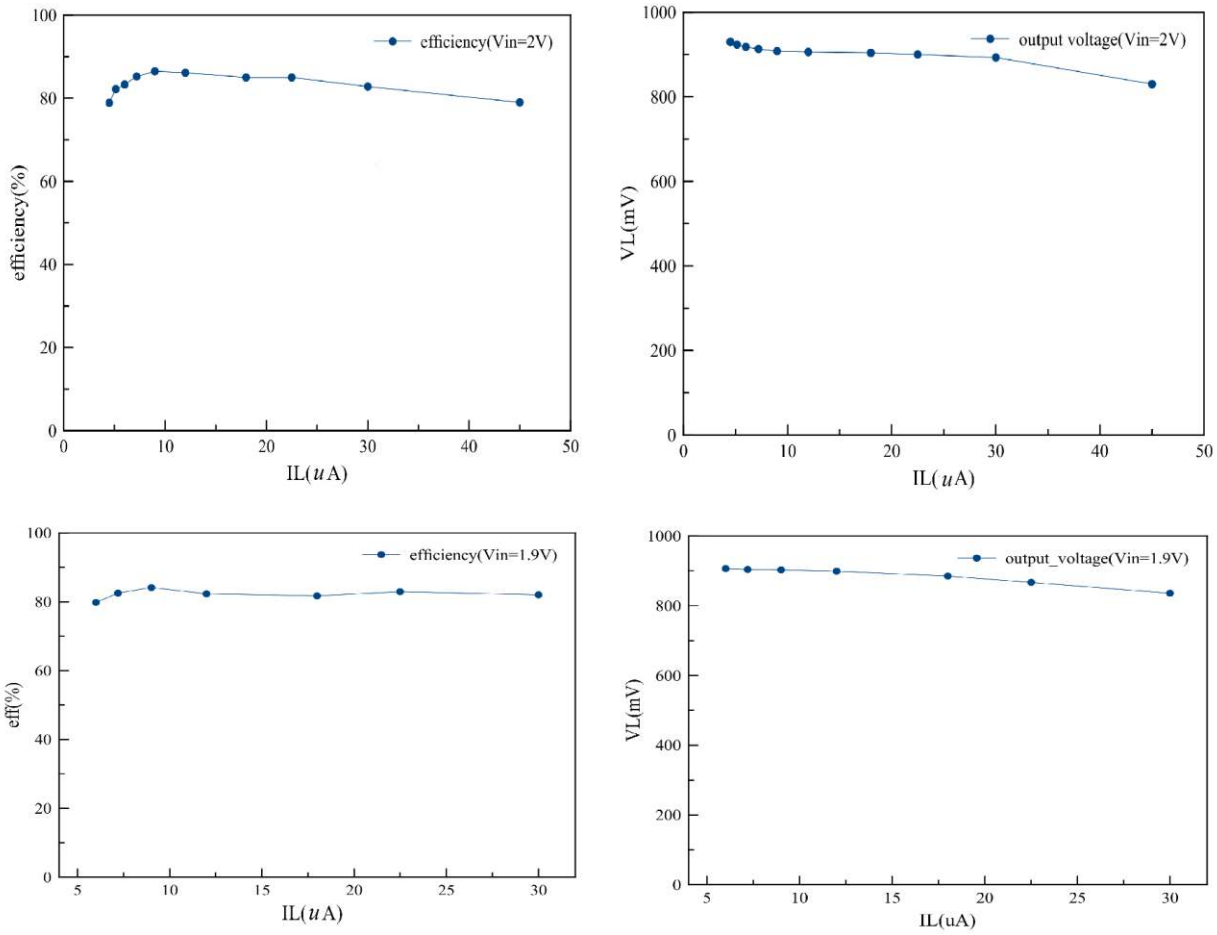

Figure 5.8: Post-layout behavior of the converter by varying the output current when the input voltage is 2Volts and 1.9Volts

Table5.4: Comparison with other works

	This Master Thesis	[20], 2013	[21], 2010	[22], 2007	[19], 2010	[23], 2013
Technology	**180nm**	40nm	130nm	180nm	350nm	180nm
Gain	**1/2**	1/4, 1/3, 1/2, 2/3	1/2	1, 1/3, 1/2, 2/3, 3/4	2/3	20 type
N°Power switches	**4**	10	5	13	7	-
Flying capacitors	**1 x 60pF**	2 x 371pF	2 x 200pF	2.4nF	2 x 336nF	-
Max switching frequency	**1.7MHz**	20MHz	20MHz	15MHz	7MHz	1.7MHz
Output regulation method	**PFM**	Hysteretic	Hysteretic +body bias control	Hysteretic	PFM	Hysteretic
Input voltage	**1.9÷2V**	1.1V	1÷1.2V	1.2V	2.5V	3.4 ÷ 4.3V
Output voltage	**900mV**	0.18÷0.6V	0.4V	0.3÷1.1V	0.9÷1.2V	0.9 ÷ 1.5V
Max output current	**40µA**	1mA	310µA	300µA	400µA	50 µA
Peak efficiency	**91.24% (Vin= 2V, Io = 9µA) 87% (post-layout)**	88.84% (V0= 0.53V, Io = 1mA)	74% (Vo = 0.4V, Io = 250µA)	85% (Vo= 1.1V, Io= 10µA)	66.7% (Vo = 1.4V)	72%(Vout = 0.9V) 69%(Vout = 1.2V) 65%(Vout = 1.5V)
Active area	**0.07mm^2**	0.074mm^2	0.13mm^2	2.56mm^2	7.8mm^2	1.69mm^2

Chapter 6

Conclusions and Future Works

This Master Thesis is a part of the challenging project in the field of implatable systems. The project goal is to avoid the use of the battery, which could add many problems, such as the complicated trade-off between small size and long lifetime. An energy harvester, which collect the energy present in the human body, replace the battery supplying the implantable system. A PMU is needed in order to extract as much energy as possible for the biosensor. Its main features should be a very low power consumption, due to the small amount of harvested energy, and a very small size, typical feature of the implantable system. In particular, the goal of this work is to deliver the right voltage needed to supply the digital circuits of the biosensor by using the energy stored in a supercapacitor by the energy harvester.

Since the harvested energy and energy consumed by the biosensor are not constant the voltage across that capacitor ranges between 1.8V and 2V. For this input and output conditions the SC DC-DC converter is the most suitable candidate to achieve the goals. Therefore, five different topologies have been investigated and the most efficient one has been determined. The designed topology can provide an output voltage of 900mV and achieve an 87% peak post-layout efficiency, including the control losses.

A lower efficiency is obtained by the SC- arrays with a conversion ratio of 2/3 and two flying capacitors, analyzed in the section 3.3.1. Effectively, the pre-layout peak efficiency is the 82%. On the other hand, since the operating frequency is lower, then the control losses are less. Moreover, it can obtain precisely 1V output, also when the input voltage is drops.

Also an ULP PFM control has been implemented in order to regulate the supply voltage of the biosensor. To decrease the power consumption as much as possible, a part of the control circuitry has been designed to work in weak inversion.

The main advantages of this design are the high efficiency and the very small overall area, which makes it suitable for implantable system applications. Indeed, only Ref. [20] has an area comparable to that of the presented master thesis, but, it uses another technology. In general, all the works presented in the Table 5.4 need much larger capacitors. Moreover, they often use a hysteretic control in order to achieve a wider range without deteriorating the efficiency. Therefore, to extend the range of our regulator, we could design the same hysteretic control, combining the advantages of the 2^{nd} and 3^{rd} topology, described in the section 3.5. However, in our application, a wider range is not really needed.
Moreover, the post layout efficiency could be enhanced following the same steps shown for the pre-layout efficiency enhancement (section 2.5), and re-finding the right trade-off among all the losses. Effectively, the width of the transistors were chosen without taking into account the parasitic parameters, extracted after the layout design. Another reason of the reduction of the efficiency from the pre-layout simulations to post layout simulations is the rise of the losses in the PFM control circuitry. By reducing the losses in the PFM control circuitry, the overall performance can be improved.

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