Ultra low-power low-noise amplifier designs for 2.4 GHz ISM band applications

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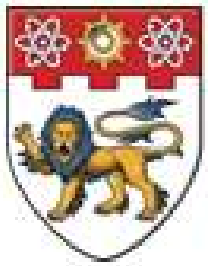

NANYANG TECHNOLOGICAL UNIVERSITY

Ultra low-power low-noise amplifier designs

for

2.4 GHz ISM band applications

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A thesis submitted to the
Nanyang Technological University
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STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

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ABSTRACT

The wireless communication industry is currently experiencing tremendous growth. In responding to the demand for a low-cost but high performance wireless front-end, many intensive researches on CMOS radio-frequency (RF) front-end circuits have been carried out. The ultimate goal is to minimize the trade-off between high performance and low-cost, low power consumption design.

Low noise amplifier (LNA) is typically the first stage of a receiver. Its performance greatly affects the overall receiver performance. In this thesis, four LNAs are proposed. They are designed for the IEEE 802.15.4 standard in the 2.4 GHz ISM band. The first three LNAs are optimized for low NF and low power. An application of this type of LNA is to be used as the amplification stage before the active mixer in the receiver chain . Active mixer provides active gain while consuming some dc power. Therefore the LNA's gain requirement can be relaxed. But its power consumption needs to be low to compensate for the power consumption from the active mixer. With a relaxed gain, the LNA should have good NF to avoid degrading the overall receiver NF. The fourth LNA is optimized for high gain. This optimization is useful in the receiver system where passive mixer is used for frequency conversion. Passive mixer consumes no dc power while having some conversion loss. Therefore, high LNA gain is required in this type of system.

There are four important contributions in this research. Firstly, and LNA (LNA1) that combining the merits of the inductive source degeneration common-source LNA (L-CSLNA) and the common-gate LNA (CGLNA) is introduced. The proposed LNA1 is a fully differential g_m-boosting CGLNA with series inductor input matching network that

improves the NF. The circuit's input matching, NF and gain have been derived to verify the design methodology. The LNA was designed and fabricated using 0.18 µm CMOS technology. It consumes only 0.98 mA from 1.0 V power supply and achieves a measured gain of 15 dB and NF of 5 dB. The series inductor input matching CGLNA is attractive for low-power fully integrated applications in CMOS technologies.

Even though the high NF problem of the CGLNA has been addressed in the proposed LNA1, we wish to further reduce the NF to achieve better trade-off between NF and power consumption. LNA2 was designed with a simple but effective noise-reducing technique. An inductor was added in parallel to the input transistor to reduce the noise from both the cascode and the input transistor. The LNA's input matching, NF and gain have been derived to verify the design methodology. The LNA achieves a measured gain of 14.8 dB, NF of 4.5 dB and *IIP3* of -5.7dBm respectively. It consumes only 0.95 mW from a 1.0 V supply voltage.

The third LNA (LNA3) was designed to consume less power and provide lower NF than that of LNA1 and LNA2. The power consumption can be reduce by operating the circuit at lower supply voltage but this shouldn't degrade the circuit's performance. LNA3 was designed for very low supply voltage such as 0.6 V. To deal with the small voltage headroom, the single-stage non-cascode structure is employed. The poor reverse isolation problem in this structure is improved by using the capacitive cross-coupling (CCC) across the two sides of a differential input stage. The CCC technique has been utilized in many LNA designs. However, in all of the reported works using CCC, the CCC technique was mainly used to improve the NF, not the reverse isolation. The poor reverse isolation problem in single-stage non-cascode structure has never been analyzed. This work shows

a novel analysis on the feedback cancellation mechanism to improve the reverse isolation. Other analysis on input matching, gain and NF of LNA3 was also performed to show the feasibility of employing CCC technique for low-voltage LNA as well as the advantages of LNA3 over the conventional common-source (CS) and common-gate (CG) LNA. This LNA is designed using 0.18 µm CMOS technology. At 2.4 GHz, high reverse isolation of -38 dB and good input matching of -24 dB was obtained. The LNA produces a total gain of 14 dB while drawing only 0.83 mA from a 0.6 V supply voltage. The NF is only 3.55 dB. The total power consumption is only 0.5 mW.

The fourth LNA (LNA4) was designed to achieve very high gain. It utilizes the π-match and capacitive feedback input network. The capacitive feedback helps to eliminate the need of using inductor at the source terminal of the input transistor for input matching condition. Moreover, higher gain and an additional degree of design freedom are achieved with the use of the π-match network. The detailed input matching, NF and gain have been derived to verify the design methodology. The LNA is designed using 0.13µm RF CMOS technology. It achieves a gain of 21.7 dB with an S_{11} of -12 dB while consuming only 0.6 mW. The NF is 4.9 dB and the *IIP3* is -12 dBm.

The performance of the four LNAs meets the specification requirements of the desired standard. In brief, the thesis investigates the CMOS RFIC designs, especially for LNA designs. It provides different approaches which can help to achieve a compact, low power and fully-integrated LNA.

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During the long journey towards this doctoral degree, it would never be possible to come up with this dissertation and all the work that went into it, without the generous assistance and support of many great people.

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Chapter 1: Introduction

1.1 Motivation

The IEEE 802.15.4 standard was specially designed to cater for the fundamental lower network layers of wireless personal area network (WPAN) which focuses on low-cost, low-speed ubiquitous communication between devices. The emphasis is on very low cost communication of nearby devices with low power consumption and little to no underlying infrastructure. The concept of IEEE 802.15.4 standard is to provide communications over distances up to about 10 meters and with maximum transfer data rates of 250 kbps. Low power consumption has been the centre of attention for many technologies. In the context of mobile wireless applications, lower power consumption can lead to longer battery life or in another word longer time over which a mobile device can be used without having to recharge. The IEEE 802.15.4 frequency bands align with the license free radio bands that are available around the globe. Of the bands available, the 2.4 GHz band is the most widely used in view of the fact that it is available globally and this brings many economies of scale.

It is known that the LNA is the first active amplification block in the receiving path as shown in Figure 1.1.

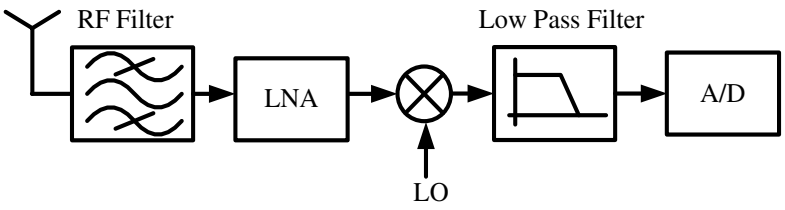

Figure 1.1: RF receiver

In fact, the performance of the RF receiver is significantly influenced by the LNA [1]. Being the first block of the receiver, the LNA plays a crucial role in amplifying the received signal while adding little noise to it. In addition, the input of the LNA needs to be matched to the output of the filter following the antenna to prevent the incoming signal from reflecting back and forth between the LNA and the antenna. While the LNA is a relatively simple design compared to other RF components in a cellular receiver chain, the performance tradeoffs challenge the LNA design engineer. LNA design typically involves making choices between directly competing performance parameters such as: noise, gain, linearity and power consumption. In the IEEE 802.15.4 standard, the NF and linearity requirement can be relaxed in order to achieve other important parameters such as gain and power consumption.

1.2 Objective and Major contributions

The objectives of our research are to develop a thorough understanding of low-power LNA design and to introduce new low-power LNA design for the IEEE 802.15.4 standard. In this thesis, four LNAs are proposed for the 2.4 GHz ISM band of IEEE 802.15.4 standard. The first three LNAs were optimized for low NF and low power consumption while the fourth LNA was optimized for high gain.

The first design (LNA1) is a fully differential g_m-boosting CGLNA with series inductor input matching network that retains the advantages of both the CSLNA and CGLNA topology. It consumes only 0.9 mA from 1.0 V power supply and achieves a measured gain of 15 dB and NF of 5 dB.

In the second design (LNA2), we introduced a noise cancellation technique that reduces the NF of the CGLNA to achieve better trade-off between NF and power

consumption. The LNA achieves a measured gain of 14.8 dB, NF of 4.5 dB and *IIP3* of -5.7 dBm respectively. It consumes only 0.95 mW from 1.0 V supply voltage.

The third LNA (LNA3) was designed with low supply voltage to reduce the total power consumption. LNA3 was designed to operate at 0.6 V supply voltage. It uses a single-stage non-cascode structure with CCC across the two sides of a differential input stage. The CCC technique had been employed in many other LNAs. However, it was mainly used to improve the LNA's NF and none of the LNAs using CCC had demonstrated low voltage operation properly. In this work, the CCC technique is not only used to lower the LNA's NF, but also to improve the reverse isolation of the single-stage non-cascode structure. A novel analysis on the feedback cancellation mechanism of the CCC technique was carried out. At 2.4 GHz, it has an input matching better than -24 dB and a reverse isolation better than -38 dB; produces 14 dB gain and 3.55 dB NF while drawing only 0.83 mA current from a 0.6 V supply voltage.

The fourth LNA (LNA4) was designed to achieve very high gain. The π-match and capacitive feedback input network were utilized. The capacitive feedback network helps to save on chip area by using only one inductor for the input matching. The π-match network introduces an additional degree of design freedom and allows the LNA to achieve higher gain than the conventional L-CSLNA. It achieves a gain of 21.7 dB with a S_{11} of -12 dB while consuming only 0.6 mW. The NF is 4.9 dB.

For all designs, the circuit's input matching, noise factor and gain have been derived to verify the design methodology. Compared to recent related works, our LNAs consume the least power but still achieve a very good performance in other parameters.

1.3 Thesis organization

The thesis is organized into seven chapters. Chapter 1 provides an introduction, motivation, objectives and an outline of the thesis. In Chapter 2, the RFIC design backgrounds including RFIC design parameters, receiver architectures, design trade-offs and conventional LNA topologies are described. The current ultra-low power LNA designs and the important requirements in the IEEE.802.15.4 standard are also discussed in this chapter. From chapter 3 to chapter 6, four ultra-low power LNAs are presented together with the measurement results. Chapter 7 draws the conclusion and suggests future works.

Chapter 2: Literature review on LNA design

As the first active block in the receiver chain, the performance of an LNA dictates the overall performance of receivers [2]. In this chapter, a review on two main receiver architectures is presented, and then key performance parameters for RF communication circuit design are discussed. Following that are an introduction to LNAs and trade-offs in LNA design. Next, the input matching architectures in LNA designs will be classified and examined. Finally, the LNA load tuning techniques will be discussed.

2.1 Receiver architectures

Complexity, cost, power dissipation and the number of external components have been the primary criteria in selecting receiver architectures. Two architectures will be discussed which are: heterodyne and homodyne receiver.

2.1.1 Heterodyne Receiver

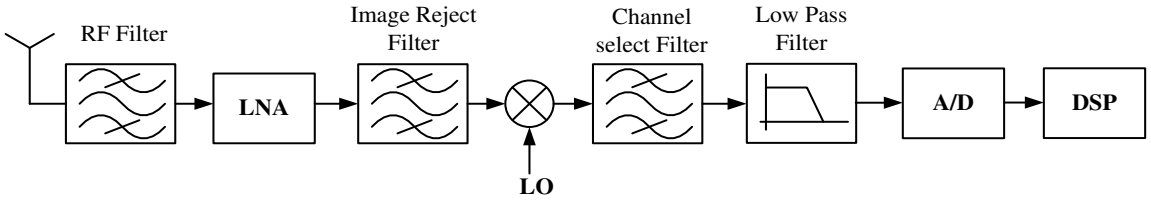

Figure 2.1: Heterodyne receiver architecture

The heterodyne receiver is probably the most popular receiver architecture. Due to its reliable performance, it has been widely implemented in many radio applications. As seen in Figure 2.1, the incoming signal is first filtered by an RF filter to lower unwanted out-of-band signals. After being amplified by an LNA, the signal is then filtered by the image-reject (IR) filter to further reduce the power level of undesired signals. Next, the RF signal is down-converted to the intermediate frequency (IF). This step is done by a

mixer. There are two types of mixer: active and passive. The active mixer consumes dc power while providing active gain. The passive one does not consumes power but having some conversion loss. To counterbalance for the lack of gain in the passive mixer, more gain is needed in the LNA stage. After passing through a narrow-band IF filter, the signal is converted to baseband signal for further processing in subsequent stages. Intermediate frequency (IF) is a critical parameter in heterodyne receiver design. The choosing of IF frequency involves a fundamental tradeoff between image rejection and channel selection or sensitivity and selectivity. More specifically, a higher IF eases image rejection because the image frequency is further away from the desired frequency. The quality factor of a filter is determined by f_{center}/BW_{filter}. Therefore a lower IF leads to a larger rejection of the interference of adjacent channels. Shown in Figure 2.2 are two cases corresponding to high and low values of IF so as to illustrate the trade-offs.

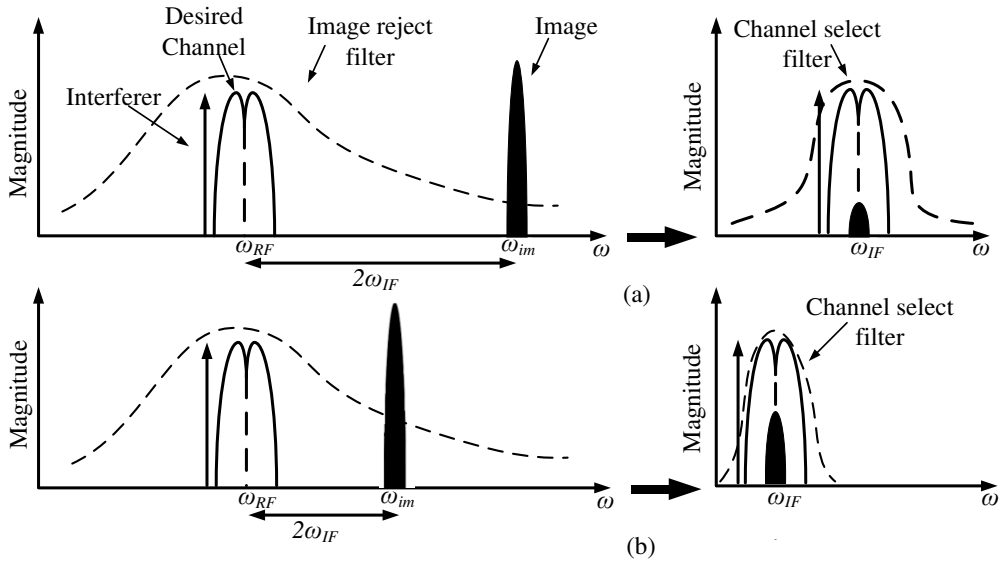

Figure 2.2: Rejection of image versus suppression of interferers for (a) high IF and (b) low IF

A high IF leads to substantial rejection of the image whereas a low IF allows great suppression of nearby interferers. The choice of IF therefore depends on trade-offs among

three parameters: the amount of image noise, the spacing between the desired band and the image, and the loss of the image reject filter. To minimize the image, one can either increase the IF or tolerate greater loss in the filter while increasing its quality factor.

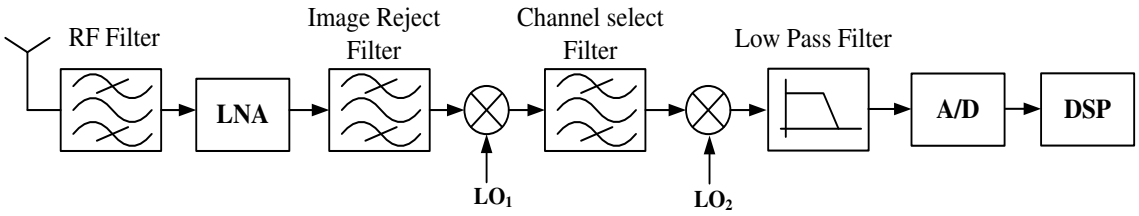

Figure 2.3: Dual-IF receiver

The multiple down-conversion helps to relax the Q requirement of the channel select filter therefore ease the trade-off between selectivity and sensitivity [3]. Shown in Figure 2.3 is the dual-IF receiver which employs two stages of down conversion. A superior performance with respect to selectivity, sensitivity and signal-to-noise ratio (SNR) makes the heterodyne receiver very attractive. However, the implementation of a heterodyne architecture involves many high-Q filters. The full integration of heterodyne receiver is very difficult. In order to avoid the needs of external IR and IF filters, direct conversion (zero-IF) and low-IF architectures have increasingly gained popularity in recent designs of wireless communications systems [4-18].

2.1.2 Homodyne Receiver (Direct conversion receiver)

A homodyne receiver is also called a zero-IF or direct conversion receiver. For double-sideband amplitude modulated signals, down conversion can be done with simple mixers. For frequency and phase modulated signals, down conversion must be performed with quadrature mixers so as to avoid loss of information due to positive and the negative part of the spectra overlap after down-conversion. The block diagram of homodyne or direct conversion receiver architecture is illustrated in Figure 2.4.

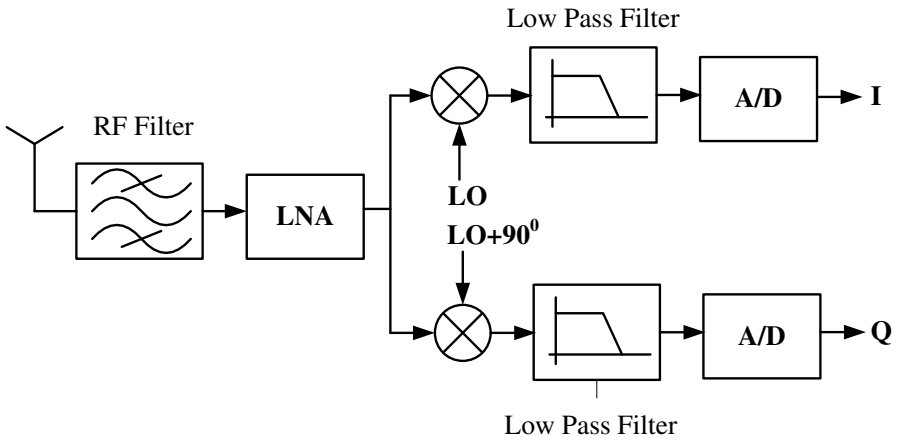

Figure 2.4: Homodyne receiver architecture

A homodyne receiver structure is very similar to the low-IF receiver. The main difference is that it down-converts RF signal frequencies directly to base band frequencies. The simplicity of the homodyne architecture offers two important advantages over a heterodyne counterpart. Firstly, the problem of image is circumvented because ω_{IF} is equal to zero. As a result, no IR filter is required, and the LNA need not drive a 50 Ω impedance of an off-chip IR filter, which reduces the overall power consumption. Secondly, the IF filter and subsequent down-conversion stages are replaced with low-pass filters and base band amplifiers that are amenable to monolithic integration [19].

However, despite its simplicity, the homodyne receiver does have some other performance issues that impede its widespread adoption [19]. Its main disadvantage is the DC offset problem. In the homodyne topology, the IF frequency is at base band, any DC offset can easily overwhelm the desired signal and saturate the following stages. The isolation between the LO port and the input of the mixer and the LNA is not perfect. There is a finite amount of feed-through exists from the LO port to the LNA input and mixer input. This leakage signal is then mixed with the LO signal, thus generating a dc

component. This phenomenon is called "self-mixing". A similar effect occurs if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself [19]**.** Another serious problem of homodyne receiver is the I/Q mismatch. Due to the quadrature mixing requirement, either the RF signal of the LO output has to be shifted by 90^0. Since shifting the RF signal generally causes severe noise-power-gain trade-offs, it is more plausible to use the topology in Figure 2.4. I/Q amplitude and phase mismatch can cause degraded SNR performance.

2.2 Design parameters

2.2.1 Sensitivity

RF receiver sensitivity quantifies the ability to respond to a weak signal. It is defined as the minimum detectable signal (MDS) power level with the requirement of the specified SNR for an analog receiver and bit-error-rate (BER) for a digital receiver [19].

IEEE 802.15.4 Requirement: Sensitivity

The sensitivity requirement of an IEEE 802.15.4 standard compliant receiver is -85 dBm [20].

2.2.2 Noise figure

Noise factor (*F*) is a measurement of the noise performance of a circuit. It is frequently expressed in decibels and commonly referred to as noise figure (*NF*):

$$NF = 10log_{10}F \tag{2.1}$$

where F is defined as:

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.2}$$

or:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{sig}/P_{RS}}{SNR_{out}} \tag{2.3}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output and P_{sig} denotes the input signal power and P_{RS} represents the source resistance noise power, both per unit bandwidth. It follows that:

$$P_{sig} = P_{RS}.F.SNR_{out} \tag{2.4}$$

Since the overall signal power is distributed across the channel bandwidth, B, the two side of equation (2.4), must be integrated over the bandwidth to obtain the total mean square power. Thus, for a flat channel:

$$P_{sig,tot} = P_{RS}.F.SNR_{out}.B \tag{2.5}$$

Equation (2.5) predicts the sensitivity as the minimum input signal that yields a given value for the output SNR. Changing the notation slightly and expressing the quantities in dB or dBm, we have:

$$P_{sig,\min\ |dB} = P_{RS|dB/Hz} + NF + SNR_{\text{out,min}\ |dB} + 10logB \tag{2.6}$$

where $P_{sig,\min}$ is the minimum input level that achieves $SNR_{\text{out,min}}$. We obtain P_{RS} as the noise power that R_s delivers to the receiver:

$$P_{RS} = \frac{4kTR_s}{4}\frac{1}{R_{in}} = kT = -174\ dBm/Hz \tag{2.7}$$

with conjugate matching at the input and at room temperature. Equation (2.6) is thus simplified to:

$$NF = P_{sig,\min\ |dB} - (-174\ dBm/Hz) - 10logB - SNR_{\text{out,min}\ |dB} \tag{2.8}$$

For a cascade system of *N* stages, the overall noise factor can be obtained in terms of the noise factor and gain at each stage. The total noise factor [19] can be expressed by the Friis equation:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1}A_{p2}} + \cdots + \frac{F_N - 1}{A_{p1}A_{p2}\ldots A_{p(N-1)}} \tag{2.9}$$

where F_m and A_{pm} are the noise factor and the available power gain of the mth stage. According to this equation, the noise contributed by each stage decreases as the gain of the preceding stage increases. Thus, the first few stages in a cascade are the most critical stages. In practice, the LNA is the first active block in the receiving chain. Therefore, its NF directly adds to that of the system. An LNA should provide enough gain to overcome the noise contribution of the subsequent stages and add as little noise as possible.

IEEE 802.15.4 Requirement: Noise Figure

Using the aforementioned 2 MHz bandwidth and $SNR_{\text{out,min}\ |dB}$ of 0.5 dB [20, 21], the required NF is -85 - (-174) - 10log(2M) – 0.5 = 25.5 dB. Therefore the required NF assuming a 5 dB loss preceding the LNA is 20.5 dB.

2.2.3 Harmonic distortion and Intermodulation

The linearity of a system determines the maximum allowable signal level to its input. All real-life systems exhibit some degree of nonlinearity. Signal distortion is a direct consequence of the nonlinear behavior of the devices in the circuits. The most common measures of non-linearity are the 1-dB compression point (P_{1dB}) and the third-order intercept point (*IP3*) [19].

2.2.3.1 The 1-dB compression point

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. When the input signal is $x(t) = Acos\omega t$ then the output through the system will be:

$$y(t) = \alpha_1 Acos\omega t + \alpha_2 A^2 cos^2 \omega t + \alpha_3 A^3 cos^3 \omega t + \cdots \tag{2.10}$$

$$\approx \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{\alpha_3 A^3}{4}\right) cos\omega t + \frac{\alpha_2 A^2}{2} cos2\omega t$$

$$+ \frac{\alpha_3 A^3}{4} cos3\omega t$$

where $\alpha_1, \alpha_2, \alpha_3$ and so on are the corresponding equation's coefficients and A is the amplitude of the input signal $x(t)$. In equation (2.10), the term with the input frequency is called the "fundamental" and the terms with higher-order frequencies are the "harmonics". For most circuits of interest, α_3 is less than zero [19]. Therefore, the gain $(\alpha_1 A + \alpha_3 A^3/4)$ is a decreasing function of A (amplitude). As the input power increases, the circuit components become saturated and the fundamental output fails to respond linearly to the input.

Figure 2.5 shows that the gain compression due to the nonlinearities in the system causes the power gain to deviate from its idealized curve. The point at which the power gain is down 1 dB from the ideal curve is referred to as the 1-dB compression point. The input power where *P1dB* occurs is known as *IP1dB*. A system must operate several decibels below this level to avoid the nonlinear region. The 1-dB compression point can be calculated as [19]:

$$IP_{1dB} = 20log_{10}\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.11}$$

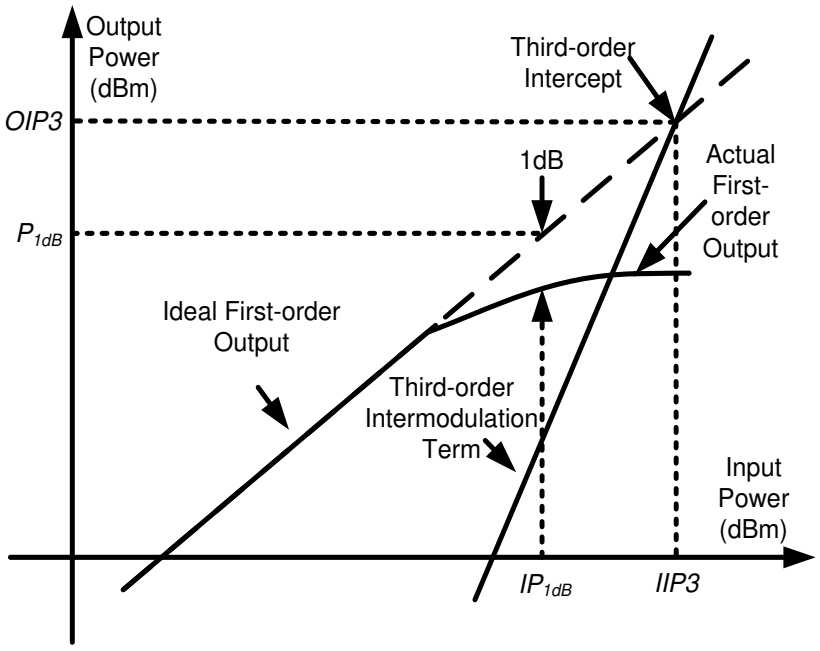

Figure 2.5: Illustrations of P_{1dB} and IP_3 (logarithmic scale)

2.2.3.2 The 3rd Order Intercept Point

While harmonic distortion is often used to describe nonlinearities of analog circuits, certain cases in RF system require other measures of non-linearity behavior. Commonly used is the "third order intercept point measured by a "two-tone" test [19].

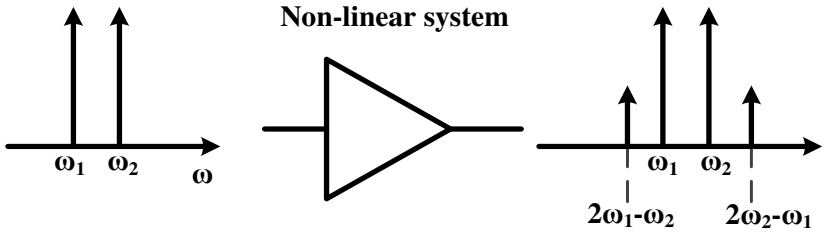

Figure 2.6: Intermodulation in a nonlinear system

When two signals with different frequencies are applied to a non-linear system (Figure 2.6), the output exhibits some components that are not harmonics of the input frequencies. Called intermodulation (IM), this phenomenon arises from "mixing" (multiplication) of the two signals. Assume that the input signal is $(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t$, then the output through the system will be:

$$y(t) = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \alpha_2(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 \quad (2.12)$$
$$+ \alpha_3(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3$$

Expanding the right side and discarding dc terms and harmonics, we obtain the following intermodulation products:

$$\omega = \omega_1 \pm \omega_2 : \alpha_1 A_1 A_2 \cos(\omega_1 + \omega_2)\, t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)\, t \quad (2.13)$$

$$= 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2)t \quad (2.14)$$

$$= 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4} cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^2 A_1}{4} cos(2\omega_2 - \omega_1)t \tag{2.15}$$

and these fundamental components:

$$\omega = \omega_1, \omega_2 : \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1^2 A_2\right) cos\omega_1 t \tag{2.16}$$

$$+ \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2^2 A_1\right) cos\omega_2 t$$

As illustrated in Figure 2.6, if the difference between ω_1 and ω_2 is small, the third-order IM products at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ appear in the vicinity of ω_1 and ω_2, thus revealing nonlinearities.

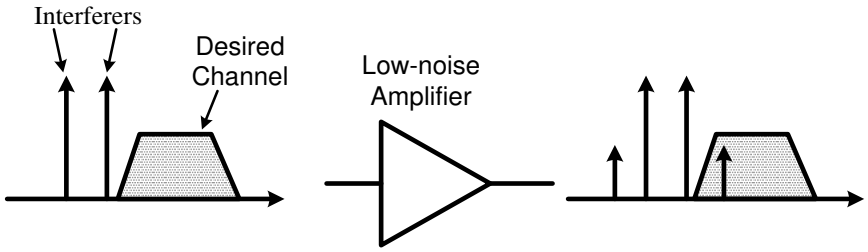

Figure 2.7: Corruption of a signal due to intermodulation between two interferers

Intermodulation is a troublesome effect in RF system. As shown in Figure 2.7, if a weak signal accompanied by two strong interferers experiences third-order non-linearity, then one of the IM products falls in the band of interest, corrupting the desired component. The "third intercept point" (*IP3*) has been defined to characterize the corruption of signals due to third-order intermodulation of two nearby interferers. It is measured by a two-tone test where $A_1 = A_2 = A$. The input signal level, where the power of the third-order IM product equals to that of the fundamental is defined as "two-tone

input-referred third-order intercept point" (*IIP3*). And the corresponding output level is called the "output third-order intercept point" (*OIP3*). $IIP3$ [19] can be calculated as:

$$IIP3 = 20log_{10}\sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.17}$$

IIP3[19] can be given by

$$IIP3 > \frac{3P_{int} - P_{sig} + SNR_{min} + margins}{2} \tag{2.18}$$

where P_{int} is the power of two interferers ($\pm$10 MHz apart and $\pm$20 MHz apart from the signal, respectively in the IEEE 802.15.4 standard), and P_{sig} is the power of the desired signal. For a cascade of N-stage network, the *IIP3* of the system, $IIP3_{tot}$, can be expressed as [3]:

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{A_1}{IIP3_2} + \frac{A_1A_2}{IIP3_3} + \cdots + \frac{A_1A_2 \ldots A_{N-1}}{IIP3_N} \tag{2.19}$$

where $IIP3_i$ and A_i (i=1,2,…N) are the $IIP3$ and the available power gain of the ith stage network respectively. Equation (2.19) suggests that, for the IIP_3 calculation, the last stage contributes the most to the distortion of the system. It is unlike the NF calculation, where the first stage is the most critical. Thus it is important to end the system with a high linearity block [22].

IEEE 802.15.4 Requirement: IIP3 and IP1dB

With an interfering power of −52 dBm, a minimum signal power of −82 dBm (3 dB above minimum sensitivity level), and an $SNR_{out,min}$ of 0.5 dB, the calculated *IIP3* based on equation (2.18) is −32.5 dBm, assuming a 10 dB margin. The input 1-dB gain

compression point (*IP1dB*) needs to be above −42.5 dBm considering *IIP3* is about 10 dB higher than IP_{1dB} [23].

2.2.4 Dynamic Range

Dynamic range (DR) is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit can provide a reasonable signal quality. This definition is quantified in different applications differently. "Spurious-free dynamic range" (*SFDR*) and blocking dynamic range (*BDR*) are two commonly used definitions of the dynamic range [24]. *SFDR* is a measure of the receiver's immunity to distortion generated by spurious signals.

The upper bound of *SFDR* is defined as the maximum input level $P_{in,\max}$ in a two-tone test, at which the third-order IM products do not exceed the noise floor. The lower bound is set by MDS. *SFDR* [25] can be expressed as:

$$SFDR = P_{in,max} - P_{in,min} = \frac{2}{3}(IIP3 - F) - SNR_{min} \tag{2.20}$$

where *F* is the receiver's NF plus the noise floor power P_n in decibel scale. P_n is calculated as $P_{RS|dB/Hz} + 10logB$ which is (-174) + 10log(2M) = −111 dBm. *BDR* is a measure of the resilience of the receiver to a large out-of-band blocking signal which, by driving the receiver into compression, desensitizes it to a small desired signal [24]. The upper bound of *BDR* is the 1-dB compression point, and the lower bound is also MDS. When expressed in *dBm*, *BDR* is given by:

$$BDR = IP_{1dB} - P_{in,min} \tag{2.21}$$

The graphic representations of *SFDR* and *BDR* are shown in Figure 2.8.

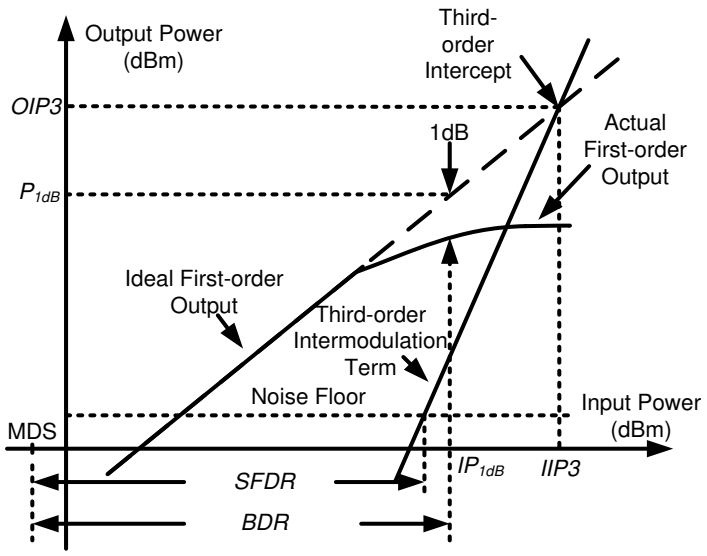

Figure 2.8: Dynamic ranges for a receiver

IEEE 802.15.4 Requirement: SFDR

From (2.20), the calculated *SFDR* is about 38 dB with an *IIP3* of −32.5 dBm, a P_n of −111 dBm, an NF of 20.5 dB, and an SNR_{min} of 0.5 dB.

2.2.5 S-Parameters

There are many different ways to characterize the behavior of a two port net work. At low frequency, Y, Z, H, T and ABCD parameters are commonly used. They use open and short circuit conditions to characterize a linear electrical network. However, these terminations are quite difficult to realize at high signal frequencies. In radio frequency range, scattering parameters (S-Parameters) is normally employed. It uses matched load termination and the measurements are based on incident and reflected waves.

Figure 2.9 illustrates a two-port network, where a_1 and a_2 are incident waves; b_1 and b_2 are reflected waves. Their relation is expressed as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = [S] \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.22}$$

The matrix $[S]$ is called scattering matrix, where S_{11} is the input reflection coefficient, S_{12} is the reverse transmission coefficient, S_{21} is the forward transmission coefficient, and S_{22} is the output reflection coefficient. They can be measured according to Figure 2.10 and equations (2.23a) – (2.23d):

$$S_{11} = \frac{b_1}{a_1}|_{a_2=0} = \text{input reflection coefficient with matched output port} \tag{2.23a}$$

$$S_{12} = \frac{b_1}{a_2}|_{a_1=0} = \text{reverse transmission coefficient with matched input port} \tag{2.23b}$$

$$S_{21} = \frac{b_2}{a_1}|_{a_2=0} = \text{forward transmission coefficient with matched output port} \tag{2.23c}$$

$$S_{22} = \frac{b_2}{a_2}|_{a_1=0} = \text{output reflection coefficient with matched input port} \tag{2.23d}$$

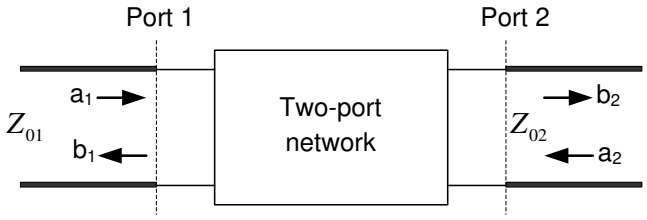

Figure 2.9: A two-port network

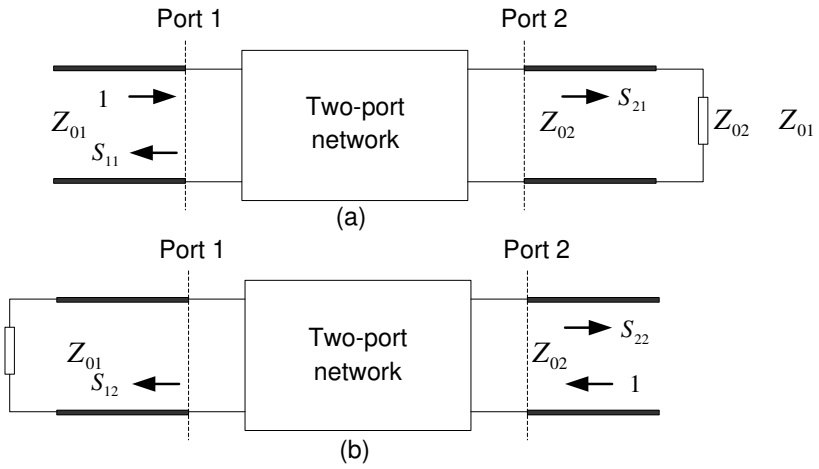

Figure 2.10: Measurement of S-parameters using (a) matched output port, (b) matched input port

From the view point of amplifier design, S_{11} and S_{22} denote how well the input and output impedances are matched to the reference impedance respectively. S_{21} measures the amplification gain of the amplifier. S_{12} represents the isolation between output and input ports. S-parameters can be converted to Y-parameters or other network representations. Detailed formula can be found in most microwave textbooks, such as [26].

2.3 Introduction to LNA

The front-end of a typical transceiver consists of a receiving path and a transmitting path. For the transmitting path, the only existent signal is the wanted signal. This simplifies the design of the transmitting path, as issues such as noise, interference rejection and selectivity can be relaxed. In contrast, for the receiving path, the wanted RF signal is weak and surrounded by noise and interferers. Thus, the design of the receiver involves many issues and trade-offs. LNA is the first active element in the receiving chain. Its NF and gain play a significant role in the overall performance of the receiver

[27]. Before exploring the design details of a low-power LNA, it is helpful to have the knowledge of the LNA design first.

In practice, the incoming RF signals are considerably small (generally around -100 dBm), which leads to a small SNR. Any additional noise will further degrade the overall SNR and therefore the receiver performance. Because LNA is the first gain stage along the receiver chain, its NF has to be low enough to keep the overall system's NF low. In addition, the gain of the LNA needs to be high enough to reduce the noise contribution from the subsequent mixer and other stages, but not too high to degrade the overall system's linearity. The linearity requirement of the LNA by itself is, in general, not very critical, except for systems such as Code-Division Multiple Access (CDMA), in which both receiver and transmitter are on at the same time. In the conventional super heterodyne receiver, because the RF filter and the image-reject filter, which are typically required to be matched to 50 Ω, are placed in front of and after the LNA, input/output impedance matching is part of LNA's specifications. The super heterodyne architecture requires at least three discrete filters. Although this architecture provides very high performance, it is very costly due to the discrete components, the packages and the additional assembly process. Hence, new radio architectures which can replace expensive discrete components with low-cost integrated circuits should be proposed. The ultimate goal is to implement a single-chip radio system. Single-chip architectures usually include homodyne/direct IF, image-reject (including Weaver architecture [28] and Hartley architecture [29]), and so on. The qualities of the above architectures allow high integration LNA design. Firstly, due to the removal of the image-reject filter, the output of the LNA no longer needs to be matched exactly to 50 Ω. Therefore, the output

impedance can be optimized for a better performance and the power consumption can be reduced due to the elimination of the additional 50 Ω output driver stage that is normally required. Secondly, aiming for full-system integration, the LNA is required to provide input matching with minimum discrete components. A fully-integrated LNA is the best option. Finally, power consumption is a concern, especially for portable devices.

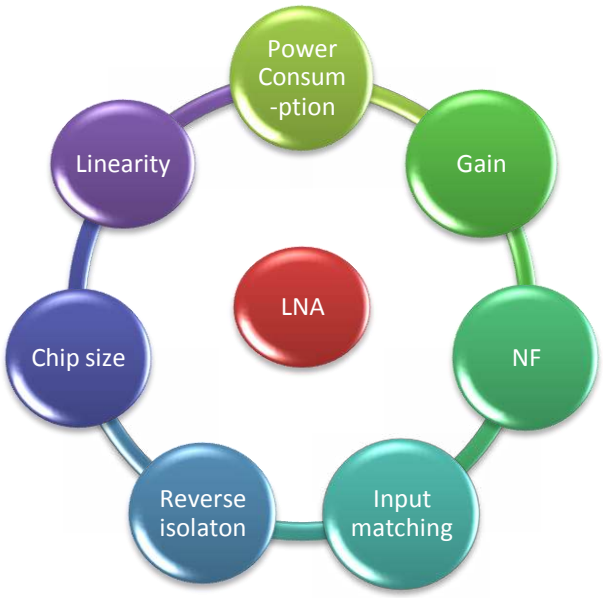

Figure 2.11: Important features in LNA design

In summary, the important features in the design of an LNA in nowadays receiver architecture are: NF, gain, input impedance matching, power consumption, reverse isolation, chip size and linearity (Figure 2.11) [30-42].

2.3.1 Performance trade-offs in LNA design

Different application has different requirement for LNA performance. Therefore, it is important to understand the trade-offs involved in LNA design. The three important trade-offs are gain vs. power efficiency, linearity vs. drain-source dc current and LNA's gain vs. receiver's dynamic range.

2.3.1.1 Gain vs Power efficiency

As we all know, an amplifier's gain is proportional to the transconductance, g_m, of its input transistor. High g_m is desirable for high gain. Using the standard saturation region dc current equations for long channel devices, we can approximate:

$$I_{DS} = \frac{1}{2} K \frac{W}{L} (V_{GS} - V_t)^2 \tag{2.24}$$

$$g_m = \sqrt{K \frac{W}{L} I_{DS}} \tag{2.25}$$

$$\frac{g_m}{I_{DS}} = \frac{2}{(V_{GS} - V_t)} \tag{2.26}$$

where K is a technology dependant constant, W and L are the width and length of the transistor, I_{DS} is the drain-source dc current, V_{GS} is the gate-source voltage and V_t is the threshold voltage. From equation (2.24) and (2.26), we notice that I_{DS} is directly proportional to $(V_{GS} - V_t)^2$, while g_m/I_{DS} is inversely proportional to $(V_{GS} - V_t)$. Figure 2.12 shows the I_{DS} and g_m/I_{DS} ratio vs. V_{GS}.

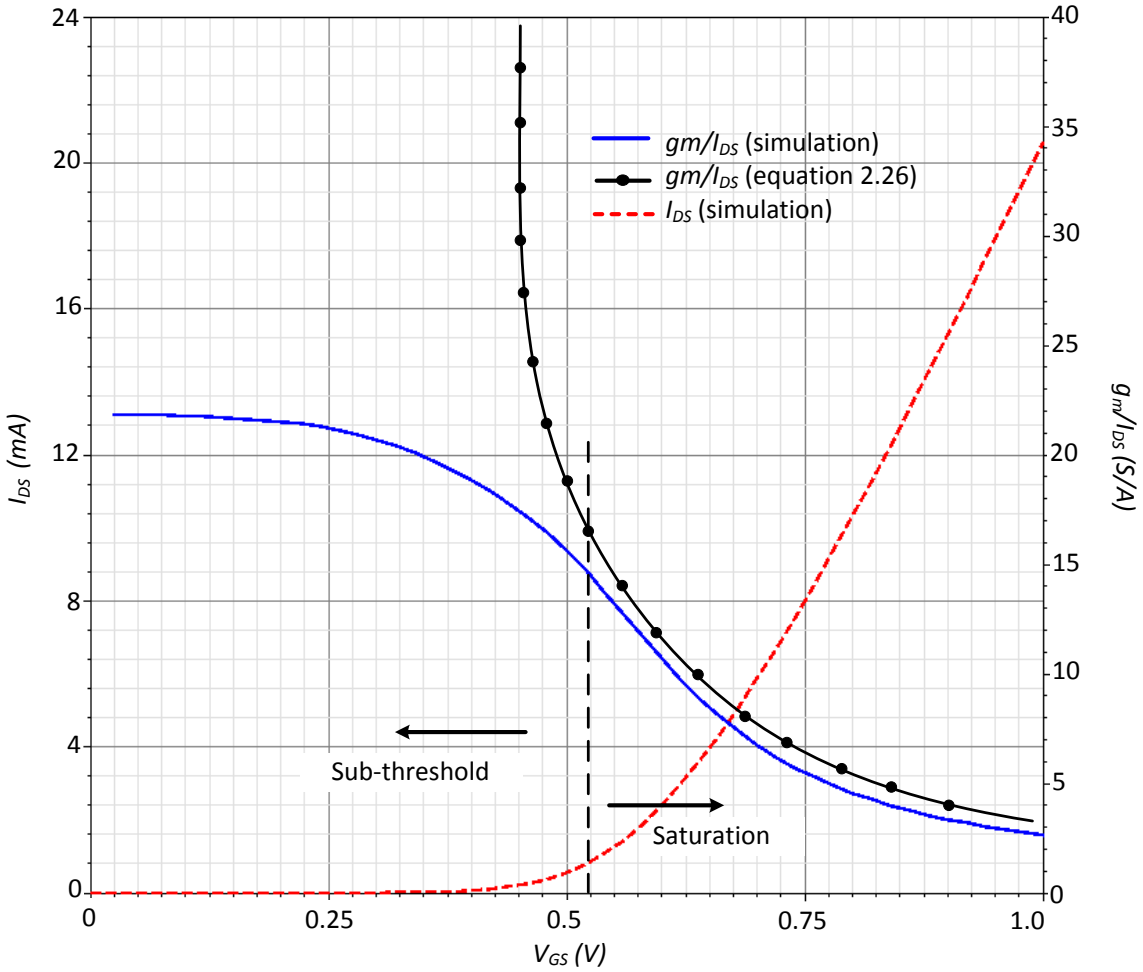

Figure 2.12: Variation of I_{DS} and g_m/I_{DS} with V_{GS} in CSM 0.18 µm RF CMOS technology (W=120 µm)

As seen in Figure 2.12, the g_m/I_{DS} calculated based on equation (2.26) is fairly close to the simulation one for $V_{GS} > 0.55$ V. The ratio g_m/I_{DS} doesn't approach infinity for $V_{GS} \to V_t$ which is 0.45 V in our simulation. This is because equation (2.26) is only applicable for the transistor in saturation region. In sub-threshold region, the MOSFET behavior is similar to a BJT, therefore g_m/I_{DS} is nearly constant. The expression of g_m/I_{DS} in sub-threshold region is :

$$\frac{g_m}{I_{DS}} = \frac{1}{nV_t} \tag{2.27}$$

where *n* is the sub-threshold slope, which for the CSM 0.18 µm RF CMOS technology is roughly equal to 1.0-1.5. The analysis and simulation results clearly demonstrate the trade-off between gain and power efficiency. High gain but low power efficiency is achieved at high V_{GS} while high power efficiency but low gain is achieved at low V_{GS}.

2.3.1.2 Linearity vs Current

Assume the main nonlinearity of a MOS transistor arises from transconductance nonlinearity [19]. The *IIP3*[19] of an LNA can be calculated as:

$$IIP3 = 20log_{10}\sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|} \tag{2.28}$$

where g_1 and g_3 are the 1st and 3rd order coefficient of M_1 obtained by taking the derivative of the drain-source dc current I_{DS} with respect to the gate-to-source voltage V_{GS} at the dc bias point:

$$g_1 = \frac{\partial I_{DS}}{\partial V_{GS}}, g_3 = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial^3 V_{GS}^3} \tag{2.29}$$

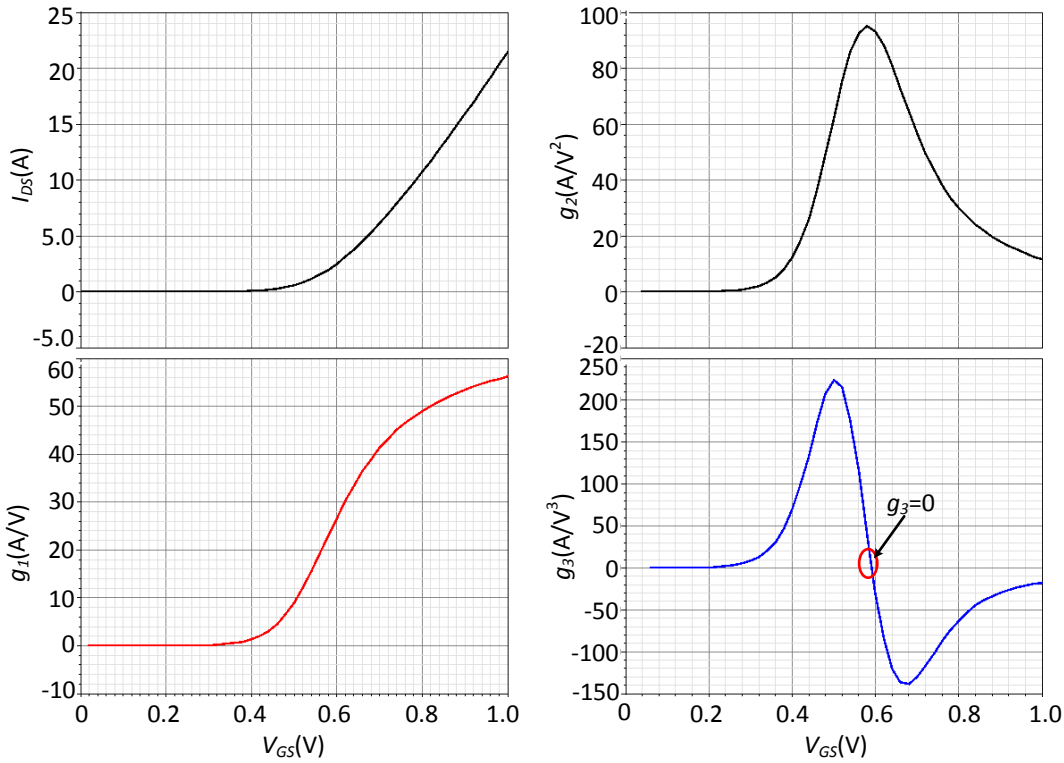

Figure 2.13: NMOS transconductance characteristics (GF 0.18 um CMOS process, W/L=120/0.18, V_{DS}=1 V)

We fixed M_1's drain source voltage V_{DS} and swept the gate source voltage V_{GS}. The first three derivatives of the drain source dc current I_{DS} with respect to V_{GS} are plotted in Figure 2.13. For high *IIP3*, it is desired to biased the transistor near the "sweet spot" where $g_3 = 0$. In our simulation, the optimum biasing point is $V_{GS} = 0.585$ V. Shown in Figure 2.14 is the $|g_1/g_3|$ value which is proportional to the *IIP3* value. As $g_3 \to 0$, $|g_1/g_3| \to \infty$ which results in a very high linearity. However, this requires a very accurate biasing which is a difficult task since biasing voltage is prone to process variations and circuit parasitic components. Outside the high linear region, we observe that the linearity improves as V_{GS} or I_{DS} increases. In this case, the task of a designer is to choose V_{GS} such that sufficient *IIP3* is achieved while using as little power as possible to accomplish this.

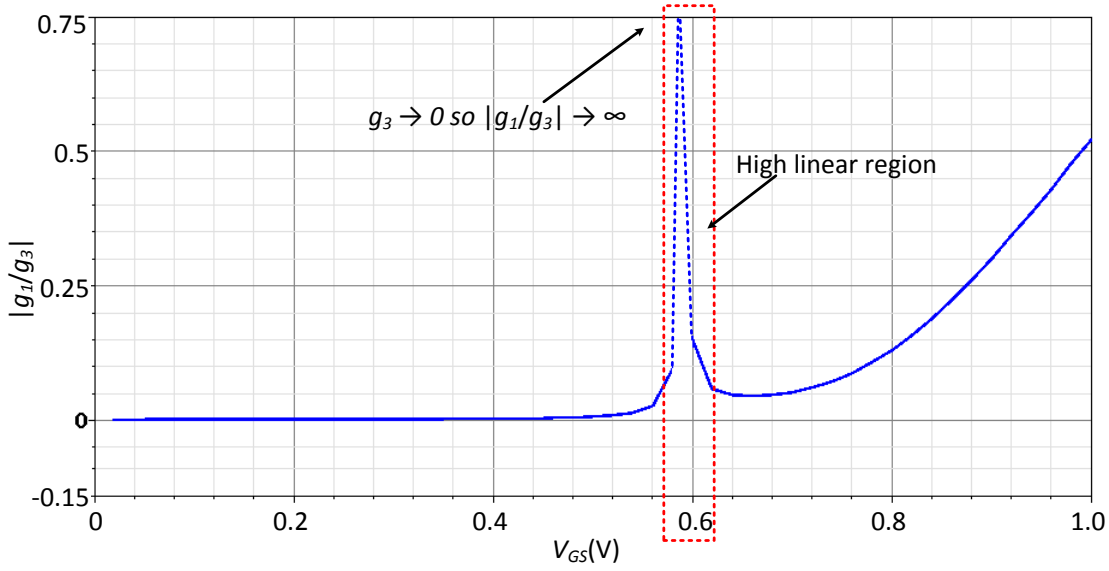

Figure 2.14: $|g_1/g_3|$ vs. V_{GS} (GF 0.18 um CMOS process, W/L=120/0.18, V_{DS}=1 V)

2.3.1.3 LNA's Gain vs Receiver's dynamic range

The trade-off between LNA's gain and receiver's dynamic range can be explained using these two equations:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1}A_{p2}} + \cdots + \frac{F_N - 1}{A_{p1}A_{p2} \ldots A_{p(N-1)}} \tag{2.30}$$

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1G_2}{IIP3_3} + \cdots + \frac{G_1G_2 \ldots G_{N-1}}{IIP3_N} \tag{2.31}$$

As shown in equation (2.30), high LNA gain is required so that the noises added by elements in the receiver lineup following the LNA are minimized. However, equation (2.31) shows that the receiver's linearity decreases as LNA's gain increases. Using equation (2.30) and (2.31), the overall NF and *IIP3* of a receiver for the IEEE 802.15.4 standard were plotted with respect to the LNA's gain in Figure 2.15 and 2.16. The performances of all the blocks right after the LNA are referred from [43].

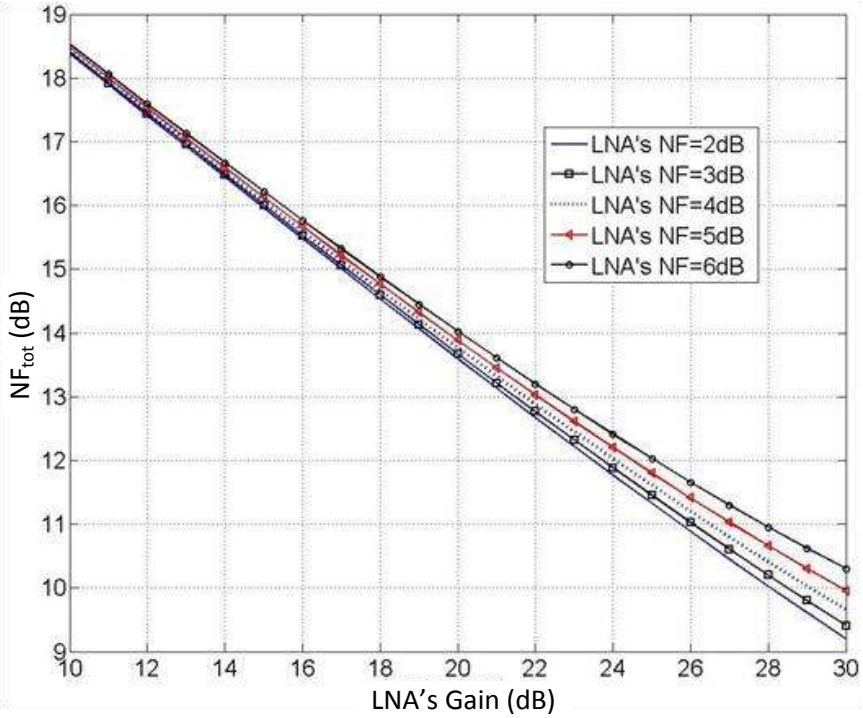

Figure 2.15: Receiver's NF vs LNA's gain (IEEE 802.15.4 standard)

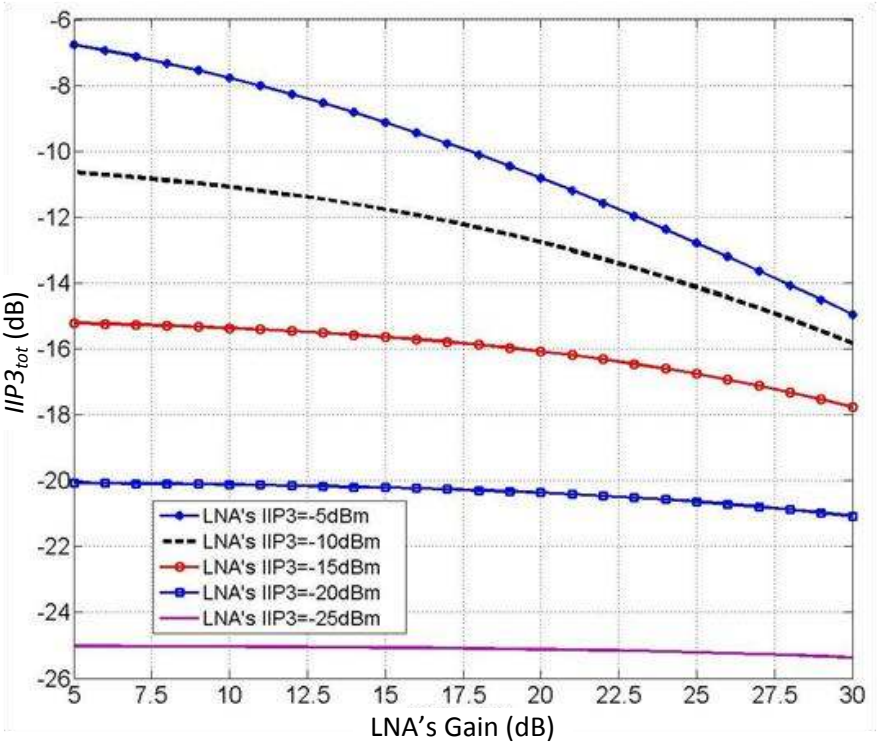

Figure 2.16: Receiver's *IIP3* vs LNA's gain (IEEE 802.15.4 standard)

As expected, the receiver's NF is improved while the *IIP3* is worsened as the LNA's gain increases. The receiver's *IIP3* becomes almost independent of LNA's gain when the LNA's *IIP3* is small (-25 dBm). This can be explained by equation (2.31). When the LNA's *IIP3*, $IIP3_1$, is very small, $1/IIP3_1$ becomes very large and dominates the right side of equation (2.26). The receiver's *IIP3* can be estimated by the LNA's *IIP3*.

In the IEEE 802.15.4 standard, the linearity requirement is not very stringent (-32.5 dBm) , therefore the trade-off between LNA's gain and receiver's dynamic range can be relaxed in our design.

2.3.2 Input Architecture

Recall from the previous section, it is known that input impedance matching to 50 Ω is one of the common goals in LNA design. Input matching architectures in LNAs can be classified into four types: CS with resistive termination, CG, CS with shunt feedback and CS with inductive source degeneration. Each of these architectures can be implemented in single-ended or differential form.

2.3.2.1 Common-Source Stage with Resistive Termination LNA

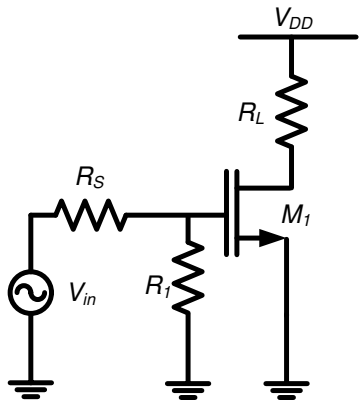

Figure 2.17: Common-source with resistive termination

This technique uses resistive termination in the input port to provide 50 Ω input impedance. As shown in Figure 2.17, a 50 Ω resistor, R_1, is placed in parallel with the input, to realize input matching for the LNA. However, this termination resistor generates noise. The noise factor [27] of the circuit can be calculated as:

$$F = \frac{\overline{v_{n,out}^2}}{\overline{v_{n,o,Rs}^2}} = \frac{\overline{v_{n,o,Rs}^2} + \overline{v_{n,o,R1}^2} + \overline{v_{n,o,M1}^2}}{\overline{v_{n,o,Rs}^2}} \tag{2.32}$$

$$= \frac{4kT(R_s//R_1)g_m^2R_L^2\Delta f + \overline{i_{n,d}^2}R_L^2}{\frac{1}{4}g_m^2R_L^2}\frac{1}{4kTR_s\Delta f}$$

where $\overline{v_{n,out}^2}$ represents the total output noise; $\overline{v_{n,o,Rs}^2}$, $\overline{v_{n,o,R1}^2}$ and $\overline{v_{n,o,M1}^2}$ are the output noise due to R_s, R_1 and M_1, respectively, k is the Boltzmann's constant and T is the absolute temperature. Transistor M_1 has various noise sources. For simplicity's sake, only the channel thermal noise $\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f$ is taken into account where γ is the coefficient of the channel thermal noise and g_{d0} is the transconductance at zero V_{DS}, since in most conditions, channel thermal noise is the dominant noise source. Equation (2.32) [27] can be further simplified to:

$$F = \frac{4(R_s//R_1)}{R_s} + \frac{4\gamma}{\alpha g_m R_s} = 2 + 4\frac{\gamma}{\alpha}\frac{1}{g_m R_s} \tag{2.33}$$

where g_m is the transconductance of the input device, and α is is the ratio of g_m to the zero V_{DS} channel conductance. The NF $(10log_{10}F)$ of this structure is very high. The NF degradation is due to two reasons. Firstly, the added resistor R_1 contributes as much noise as the source resistor R_s does. It results in a factor of 2 in the first term of equation (2.33). Secondly, the input is attenuated, leading to a factor of 4 in the second term of equation

(2.33) [44]. The poor NF makes this architecture unattractive for applications where a low noise as well as a good input matching is desired.

2.3.2.2 Common-Gate LNA

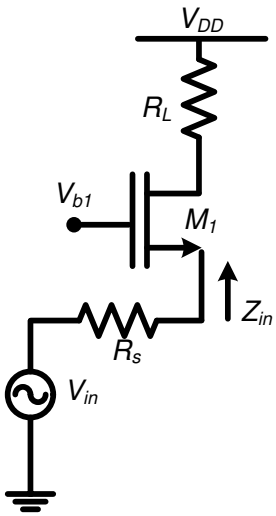

Figure 2.18: CGLNA

Figure 2.18 shows the simplified CGLNA. The CGLNA is well known for wideband applications [45-53]. The input impedance and voltage gain of a CGLNA are:

$$Z_{in} = \frac{1}{g_m} \tag{2.34}$$

$$A = g_m R_L \tag{2.35}$$

To realize the input matching, its g_m value is fixed at $1/R_S$. As a result, only the load impedance R_L remains as a design variable. Moreover, due to the input matching constraint, the transconductance of the input transistor cannot be arbitrarily high, thus imposing a lower bound on the noise factor. Through derivation, total noise factor [26] of CGLNA can be simplified as:

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_s} \tag{2.36}$$

When the input is matched, noise factor simply becomes $1 + \gamma/\alpha$. This noise factor is quite reasonable and acceptable. However, it is important to note that other noise sources such as gate induced noise and substrate noise can degrade the performance substantially. Furthermore, the load as well as the biasing circuits can generate additional noise. If we consider the effect of finite transistor drain-source resistor, r_{ds}, the total noise factor of this LNA is:

$$F = 1 + \frac{\gamma}{\alpha}\frac{g_m}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_L)/r_{ds}}\right)^2 + \frac{R_L}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}}{R_s + R_L + (1 + g_m R_s) r_{ds}}\right)^2 \tag{2.37}$$

as derived in Appendix A. In the noise analysis, the effect of gate noise is omitted since its contribution to the total noise factor is negligible compared to other noise sources. This assumption is verified through our simulations, where the gate noise accounts for less than 3% of total output noise in all of the cases. If $r_{ds} \to \infty$, $F_{CGLNA} = 1 + (\gamma/\alpha)[1/(g_m R_s)]$, which is consistent with the textbook result. The channel thermal noise of transistor M_1 and the thermal noise of the output load are accounted in the second and third term of equation (2.37) respectively. This equation is derived for CGLNA with resistive load. If inductive load is used, (2.37) becomes:

$$F = 1 + \frac{\gamma}{\alpha}\frac{g_m}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_p}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)/r_{ds}}\right)^2 + \frac{r_L}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_P}{1 + g_m r_{ds}}}{R_s + R_p + (1 + g_m R_s) r_{ds}}\right)^2 \quad (2.38)$$

where r_L is inductor loss and R_p is the equivalent output impedance at the desired frequency. The value of r_L ranges from $0 - 15\ \Omega$ for all the inductors we used in this thesis. Let's represent the second and third term in (2.38) by k_1 and k_2. When r_{ds} is increased from $0 \to \infty$, k_1 increases from $0 \to (\gamma/\alpha)/(g_m R_s)$ while k_2 decreases from $r_L/R_s \to 0$. Equation (2.38) shows that the value of r_{ds} has a great impact on the total noise factor of the CGLNA. We will base on this characteristic to design a noise cancellation scheme for the CGLNA which will be presented in Chapter 4. When r_{ds} is large, k_2 is much smaller than unity and k_1. The effect of k_2 on the overall noise factor can be neglected. Equation (2.38) can be simplified to:

$$F = 1 + \frac{\gamma}{\alpha}\frac{g_m}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_p}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)/r_{ds}}\right)^2 \quad (2.39)$$

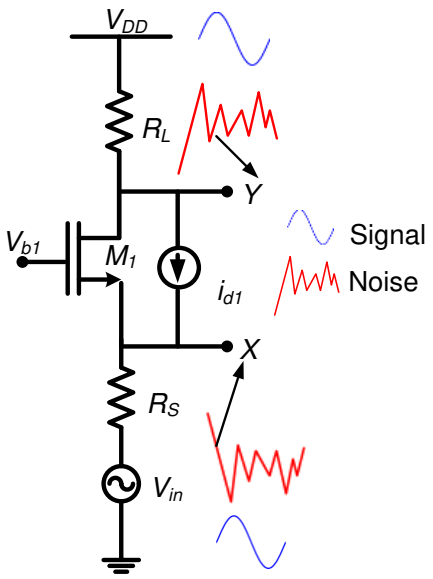

Figure 2.19: Noise and signal voltage at the source and drain terminal of CGLNA

Next, we will discuss some noise cancellation techniques for CGLNA in literature. The technique in [54-56] is based on the signal and noise characteristic at the drain and source terminals of the input transistor As demonstrated in Figure 2.19, the channel thermal noise of transistor M_1, which is modeled as a current source i_{d1}, flows into node *X* and out of node *Y*. This creates two correlated but out-of phase noise voltages at node X and Y. On the other hand, the signal voltages at these two nodes are totally in phase. The LNA in [54] is a single-ended design as shown in Figure 2.20(a). The principle of noise cancellation in this LNA can be briefly explained as follows. The input signal undergoes feed-forward voltage amplification whereas the channel thermal noise of transistor M_1 undergoes subtraction at the output node due to two correlated but out-of-phase noise voltages at the drain and source terminal of transistor M_1. A residual factor [54]:

$$\delta = \frac{R_s}{R_1}\frac{g_{m3}}{g_{m2}} - 1 \tag{2.40}$$

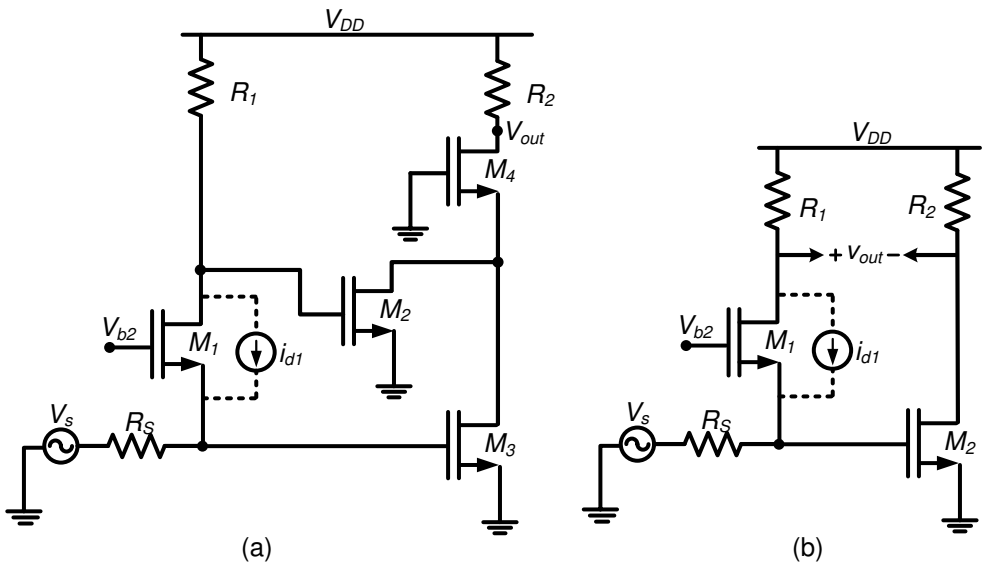

Figure 2.20: (a) Single and (b) Differential CGLNA with noise cancellation

defines the degree of cancellation of M_1's channel thermal noise. $\delta = -1$ represents disabling M_3 and no cancellation while $\delta = 0$ represents full cancellation of M_1 noise. δ can be any value greater than -1. A minimum NF below 2 dB for broadband CGLNA was predicted by maximally utilizing the available voltage headroom and power supply in a given technology. The same noise cancellation principle can be implemented in a single-input differential-output structure to eliminate the need of off-chip balun as shown in Figure 2.20(b) [55-56]. The residual factor [55] defining the degree of cancellation of M_1 channel thermal noise in this case is:

$$\delta = \frac{R_s}{R_1}\frac{1}{g_{m2}R_2} - 1 \tag{2.41}$$

To achieve a well-balanced output, the gain of two branches must be equal in magnitude and opposite in sign. Though simple in principle, this noise cancellation technique has several limitations. Firstly, the cancellation and output balance are sensitive to process variations (e.g., transistor and resistor matching). Secondly, the full cancellation condition requires resistive output loading to maintain a precise ratio of

R_1/R_s. This will limit the maximum achievable gain and minimum required supply voltage. And lastly, this technique uses an additional CS stage to cancel to noise of the CG transistor. However, this CS stage still adds noise and consumes extra power to the whole LNA. This technique may not be suitable for ultra-low power LNA. Reported in [54-56], the LNAs consume 36 mW, 17.4 mW and 12.6 mW respectively.

The designs in [57] and [58] employed the capacitive cross coupling technique to boost the transconductance value without drawing additional current. By doing so, the NF of the CGLNA is reduced significantly. A complete noise analysis of this technique will be discussed in chapter 5.

2.3.2.3 Common- Source Stage with Shunt Feedback LNA

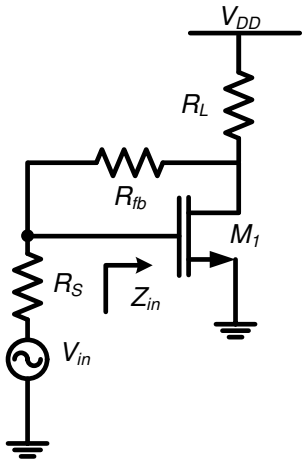

Figure 2.21: Common-source input stage with shunt feedback

Figure 2.21 illustrates another topology, which uses the resistive shunt feedback to set the 50 Ω input impedance of the LNA. The input impedance [27] can be expressed as:

$$Z_{in} \approx R_{fb}/(1 + |A_v|) \tag{2.42}$$

where R_{fb} is the feedback resistor and A_v is the corresponding voltage gain which equals to $\left[1 - g_m\left(R_L // R_{fb}\right)\right]$. The noise factor [27] for this configuration can be expressed as follows:

$$F = 1 + \left(\frac{G_s + G_{fb}}{g_m - G_{fb}}\right)^2 R_s(G_L + \gamma g_{d0}) + \left(\frac{G_s + g_m}{g_m - G_{fb}}\right)^2 R_s G_{fb} \tag{2.43}$$

where g_{d0} is the zero V_{DS} channel conductance, G_s, G_{fb} and G_L is the conductance of the resistors R_s, R_{fb} and R_L, respectively. This topology is commonly used for wideband applications. Compared to the conventional CGLNA, it normally can achieve lower NF. However, it still has several disadvantages. Firstly, the input impedance Z_{in} depends on R_{fb} and A_v. Therefore it is sensitive to process variation. Secondly, the feedback signal may contain substantial noise, thus raising the NF to an unacceptable level. Lastly, the total phase shift around the loop may create instability for certain source and load impedances. The analysis in [59] indicates that the drain noise is the largest contributor. The work in [60] used noise canceling technique to reduce the channel thermal noise of a wideband LNA of this structure. The noise cancellation principle is the same as in [54-56]. Therefore it has the same disadvantages. The LNA in [60] consumes 35 mW from 2.5 V supply voltage which is quite high for our targeted application.

2.3.2.4 Common-Source Stage with Source Inductive Degeneration LNA

Figure 2.22 shows the fourth architecture which employs source inductive degeneration to generate a real term in the input impedance. The input impedance [3] is:

$$Z_{in} \approx j\left(\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\right) + \frac{g_m L_s}{C_{gs}} \tag{2.44}$$

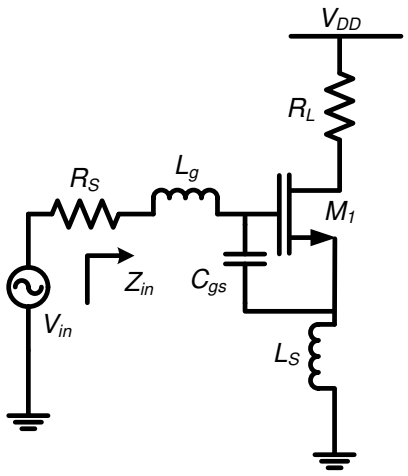

Figure 2.22: Common-source input stage with source inductive degeneration

The input impedance has a resistive term $g_m L_s/C_{gs}$, which is directly proportional to the inductance value. Whatever value this resistive term is, it does not generate thermal noise like an ordinary resistor does, because a pure reactance is noiseless [61]. Therefore, this structure can be exploited to provide the specified input impedance without degrading the noise performance of the amplifier. To get the 50 Ω input impedance, let the real part $g_m L_s/C_{gs}$, of equation (2.44) equal to 50 Ω and the imaginary part $\left[\omega L_g + \omega L_s - 1/\left(\omega C_{gs}\right)\right]$ be zero at the frequency of interest. The resonance frequency is therefore:

$$\omega_0 = \frac{1}{\sqrt{\left(L_g + L_s\right)C_{gs}}} \tag{2.45}$$

A detailed noise analysis and optimization of the LNA with this architecture are presented in [11] and will not be repeated here. The noise factor can be simplified as:

$$F = 1 + 2.4\frac{\gamma}{\alpha}\frac{\omega_0}{\omega_T} \tag{2.46}$$

where $\omega_T = g_m/C_{gs}$ is the unity current gain frequency. Based on the analysis in [44], the CS topology with source inductive degeneration provides a low NF, comparable gain and low power consumption. Currently, this topology is widely used in the design of CMOS narrow-band LNAs [62-73]. However, in system-on-chip (SOC) design, inductor L_g normally has low quality factor, i.e., has large parasitic resistance which significantly affects the input matching and the NF of the LNA. The input impedance which takes into account the effect of parasitic resistance, r_L, of inductor L_g is:

$$Z'_{in} \approx j\left(\omega_0 L_g + \omega_0 L_s - \frac{1}{\omega_0 C_{gs}}\right) + \frac{g_m L_s}{C_{gs}} + r_L \tag{2.47}$$

Substituting $C_{gs} = 1/\left[\omega_0^2\left(L_g + L_s\right)\right]$ into (2.47) at matching condition $Z'_{in} = R_s$, we have derived the relation of L_g and L_s as followed:

$$L_s = \sqrt{\frac{L_g^2}{4} + \frac{R_s - r_L}{g_m \omega_0^2}} - \frac{L_g}{2} \tag{2.48}$$

The unity current gain frequency is derived as:

$$\omega_T = \frac{g_m}{C_{gs}} = g_m \omega_0^2\left(L_g + L_s\right) = g_m\left(\sqrt{\frac{L_g^2}{4} + \frac{R_s - r_L}{g_m \omega^2}} + \frac{L_g}{2}\right) \tag{2.49}$$

The noise factor including the effect of r_L is:

$$F' = 1 + 2.4\frac{\gamma}{\alpha}\frac{\omega_0}{\omega_T} + \frac{r_L}{R_s} \tag{2.50}$$

From equation (2.49), it is shown that ω_T increases as L_g increases. Therefore, an increasing in L_g results in a reduction of the second term but an increasing of the third term in the noise factor equation (2.50). To achieve the minimum NF, the L_g must be

carefully chosen to balance the trade-off between the second and third term. Figure 2.23 shows the L-CSLNA's NF at different L_g value. The minimum NF occurs near $L_g = 7\ nH$ in our simulation.

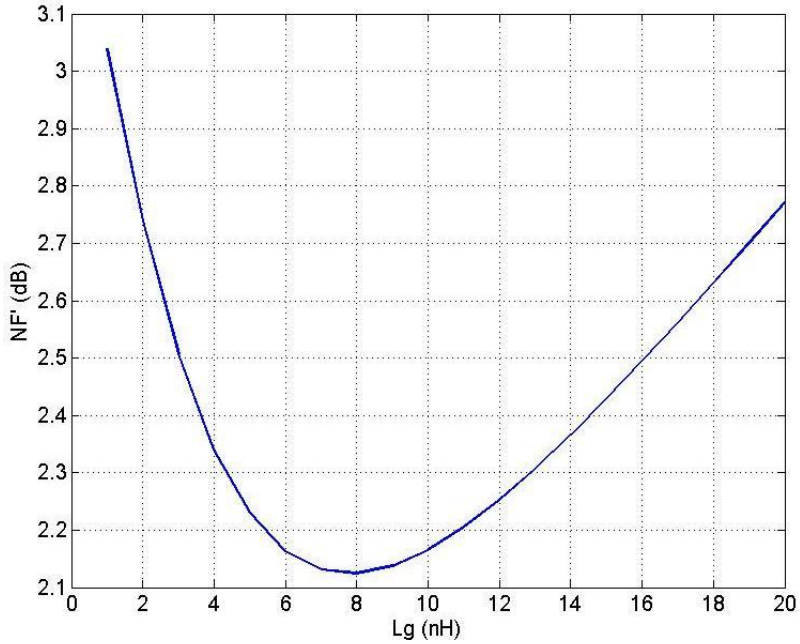

Figure 2.23: NF of L-CSLNA vs L_g ($g_m = 40\ mS, \omega = 2\pi * 2.4\ GHz, R_s = 50\ \Omega$)

2.3.3 Tuning techniques of LNA's Load

Besides the input matching network, the tuning techniques applied to the load at the device output will also affect the performance of the LNA. A good design of the tuning load helps to reject out-of-band signals and noise as well as to achieve a high gain. Three types of tuning loads commonly used are: resistive load, passive LC load and active inductor and passive capacitor load.

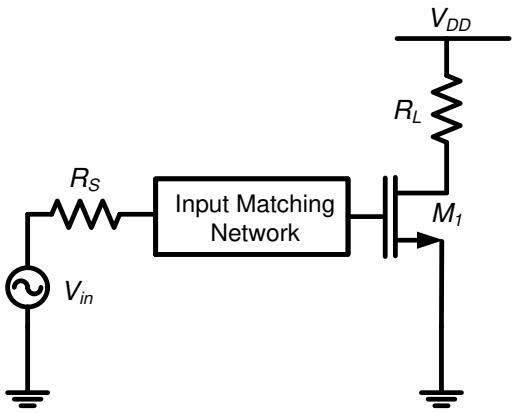

Figure 2.24: LNA with resistive load

2.3.3.1 Ordinary Resistor as Load

As shown in Figure 2.24, an ordinary resistor R_L is used as the LNA output load. Sometimes, resistor R_L is replaced by a MOS transistor. This method produces wideband output impedance and can be easily implemented. However, it is not suitable for low noise applications, because the resistor generates thermal noise. Moreover, the use of resistive load will reduce the voltage headroom across the transistor significantly. This will result in poor linearity performance if low supply voltage is required.

2.3.3.2 Passive LC as Tuning Load

Figure 2.25 shows another type of load. It is the most prevalent type used in LNA design [74-77]. It is used extensively in communication circuits to provide selective amplification of wanted signals and to filter out unwanted signals to some extent. The RLC network has an admittance of:

$$Y = j\left(\omega C_L - \frac{1}{\omega L_L}\right) + 1/R_p \tag{2.51}$$

where C_L equals to the total parasitic capacitances at the drain terminal of M_1 plus the capacitance of next stage, R_p is the equivalent parallel resistance of L_L. When the

inductor L_L and capacitor C_L are designed to resonate at a selected frequency, the impedance is purely real and at its maximum. The higher the quality factor of L_L is, the larger R_p is, and the higher the voltage gain is. This type of tuning load is very suitable for narrow-band applications. It allows LNAs to achieve substantial gain at relatively high frequencies with low power consumption.

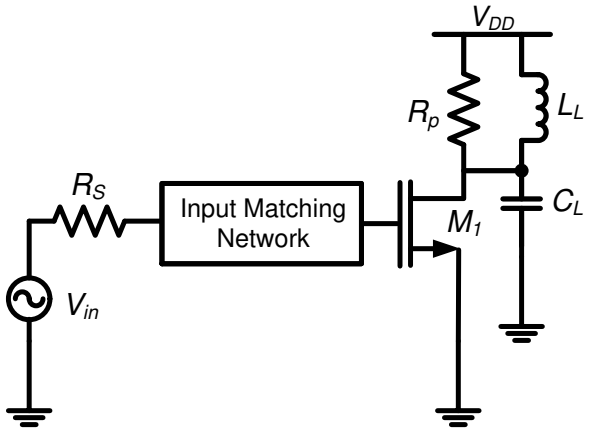

Figure 2.25: LNA with passive LC tuning stage

In practice, the silicon-based on-chip spiral inductor does not have a large quality factor Q. Hence, R_p is not very high. R_p is normally less than 1 kΩ for most of the cases. There are several ways to increase R_p. One way is to use high-Q off-chip inductors by sacrificing the market demands for highly-integrated products. Another way is through process modification to obtain a higher inductor Q. For example, a higher Q can be achieved by removing the inductor's underlying silicon substrate or by using a thick top metal. These might introduce additional processing steps and increase the cost. The third way is to use the Q-enhanced technique [78-80], as illustrated in Figure 2.26.

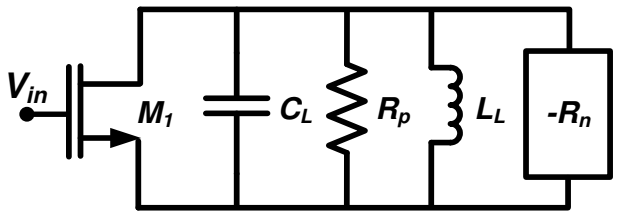

Figure 2.26: The Q-enhancement technique

The basic principle of the Q-enhancement technique is to add a negative conductance to the LC resonator so that the resistive loss of the inductor can be compensated. Without the negative resistance $-R_n$, Q can be expressed as $Q = \left(\sqrt{C_L/L_L}\right) R_p$ [26]. The above equation indicates that Q is drastically reduced because of the ohmic loss in the inductor. To reduce the effect of R_p on the Q, a negative resistance $-R_n$ is employed to compensate the loss in the inductor. Thus the Q of the tuned circuit increases to $Q = \left(\sqrt{C_L/L}\right)R_p R_n/\left(R_n - R_p\right)$. With this method, the achieved Q can be 20 or even higher. R_p can't be larger than R_n; otherwise, the circuit will oscillate [26].

2.3.3.3 Active Inductor and Capacitor as Tuning Load

Due to the limitation of spiral inductors, for example, large chip area or parasitic capacitance and resistance loss, active inductors that can be implemented with a reasonable physical size offer a good alternative for its passive equivalent [81-85]. Traditional active inductors are typically implemented by using high gain operational amplifiers with negative feedback, and are unsuitable for operating frequencies up to gigahertz. Another type of active inductor is implemented by exploiting the parasitic capacitance of the transistors to generate the required poles and zeros [81-85]. Figure 2.27 illustrates a simplified schematic diagram of an active inductor [86].

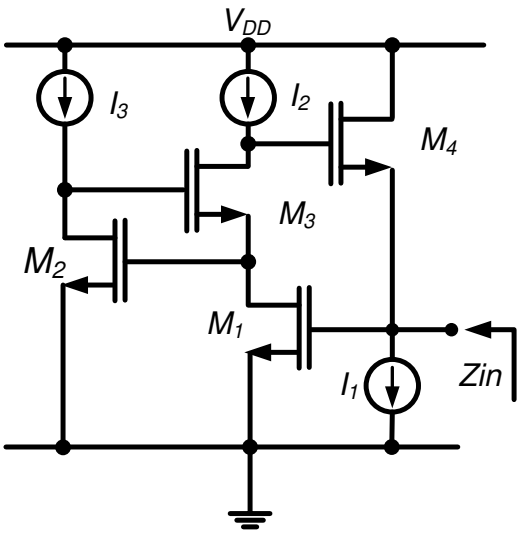

Figure 2.27: Simplified schematic diagram of an active inductor

By varying I_1 and I_2, the required value of the inductor can be obtained. There are two limitations for this circuit. Firstly, it has poor linearity [86]. Secondly, the active inductor has poor noise performance. In general, active inductors are always noisier than passive inductors due to the active devices.

2.3.4 Ultra-low power LNA design

The conventional L-CSLNA is widely used in narrow band applications due to its high gain and low noise advantages. However, when the NF requirement is not very stringent, other topologies can be explored in order to minimize the power consumption. In [87], the cascode-CS topology is used together with an inter-stage inductor to enhance the gain of the input stage. A low power of 0.8 mW and a NF of 4.1 dB are reported. This LNA efficiently trades the NF with the power consumption. However, four on-chip inductors are needed in this design which results in a large chip area. The work in [57] introduces a g_m-boosting scheme that helps to improve the noise performance of the CG topology making this topology attractive for narrow band applications. This LNA

achieves a low NF of 3 dB while consuming 6.48 mW of dc power. Such a low NF is not necessary in our application; therefore this technique can be explored in order to effectively trade the NF for low power consumption.

2.3.5 IEEE 802.15.4 Specifications

The IEEE 802.15.4 standard covers three frequency bands, i.e., 868 MHz, 915 MHz, and 2.4 GHz. The popular 2.4 GHz industrial, scientific, and medical (ISM) band was chosen for this work because it is an unlicensed band and is accepted worldwide. Furthermore, 2.4 GHz is a high enough frequency (compared to 868 MHz, and 915 MHz band) to permit integration of high quality on-chip inductors with reasonable size [88]. Receiver's specifications [43] that are important to the LNA design is shown in Table 2.1. The IEEE 802.15.4 standard has a system bandwidth spanning 83.5 MHz. This 83.5 MHz bandwidth is divided into 16 channels each with a bandwidth of 2 MHz, and spaced by 5 MHz.

Table 2.1: IEEE 802.15.4 Receiver requirements

Receiver's Specification	Requirement
Bandwidth	83.5 MHz
NF	< 19 dB
IIP3	> -20 dBm

We aim to optimize our LNA design in two directions; one is for low NF and low power and the other one is for high gain. We need to formulate two sets of LNA specification requirement for our designs. The work in [43] and [89] introduced two different receiver system for the 2.4 GHz ISM band. One used active mixer and the other used passive mixer to realize the front-end. Based on the performances of all the blocks right after the LNA in [43] and [89], we formulate the required specifications for our LNAs. For the system using active mixer at its front-end, we set the LNA's targeted gain to be 15 dB. If passive mixer is used, higher LNA's gain is required. Our targeted gain for this case is 21 dB. The other LNA's specifications are derived in Table 2.2 respectively. S_{11} and S_{12} represent the input matching and reverse isolation of an LNA.

Table 2.2: IEEE 802.15.4 LNA requirements for system using active mixer

LNA's Specification	LNA's Requirement (low NF)	LNA's Requirement (high gain)
Bandwidth	83.5 MHz	
Gain	15 dB	21 dB
NF	< 16.19 dB	<18.9 dB
IIP3	> -19.77 dBm	>-20 dBm
S_{11}	< -10 dB	< -10 dB
S_{12}	< -30 dB	< -30 dB

Chapter 3: LNA1-Series input resonance common-gate LNA

3.1 The proposed series input resonance CGLNA (LNA1)

LNA1 combined the series RLC input matching network of the L-CSLNA with the CGLNA topology. The RLC input network adds an additional degree of freedom to the input matching design and improves the NF of the CGLNA. These advantages will be presented below.

3.1.1 Input matching

Figure 3.1 and 3.2 show the schematic of LNA1 and its equivalent small signal circuit for input matching analysis.

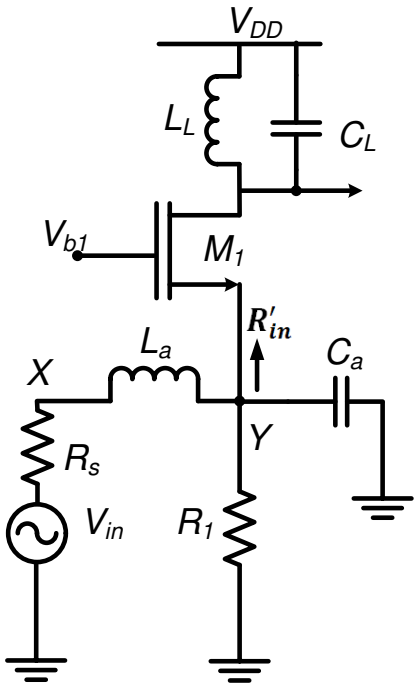

Figure 3.1: The proposed CGLNA with series input matching

To reduce the chip area, resistor R_1 is used to connect M_1's source terminal to ground instead of an inductor. C_a is the total capacitance at node Y. Resistor r_{La} is the parasitic resistance of the gate inductor L_a. R'_{in} is the impedance looking into the transistor source terminal from node Y. If an infinite transistor output resistance, r_{ds}, is assumed, it is easy to show that $R'_{in} = 1/g_m$. However, in practice, especially in short-channel MOSFET case, where r_{ds} is not very large, the effect of the finite transistor output resistance, r_{ds}, has to be taken into account. In CG topology, r_{ds} forms a positive feedback and the input resistance R'_{in} becomes:

$$R'_{in} = \left(r_{ds} + R_p\right)/(1 + g_m r_{ds}). \tag{3.1}$$

where R_p is the equivalent output impedance.

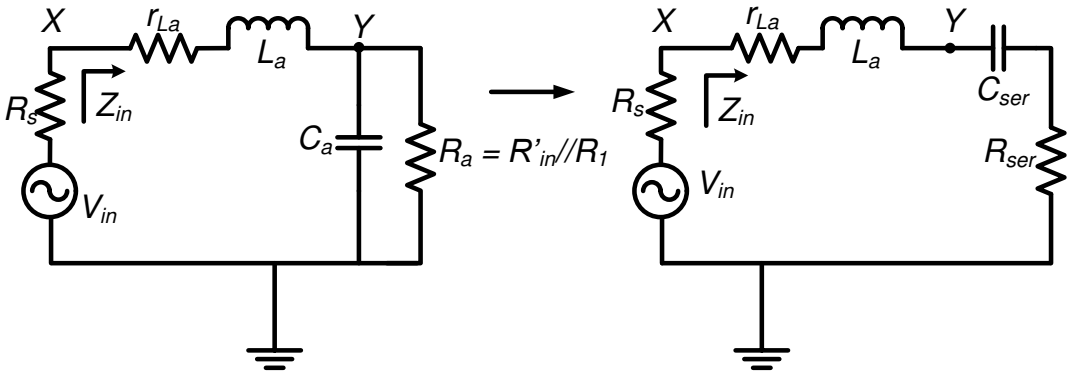

Figure 3.2: Equivalent input matching network of the CGLNA with series input matching network

The parallel input network is converted into a series input network as seen in Figure 3.2. The input impedance is:

$$Z_{in} = j\omega_0 \left[L_a - \frac{C_a}{(1/R_a)^2 + \omega_0^2 C_a^2}\right] + \frac{1/R_a}{(1/R_a)^2 + \omega_0^2 C_a^2} + r_{La} \tag{3.2}$$

In (3.2), R_a equals to $R'_{in}//R_1$. The resonance frequency is found to be:

$$\omega_0 = \sqrt{\frac{1}{L_a C_a} - \frac{(1/R_a)^2}{C_a^2}} \tag{3.3}$$

Based on the small signal circuit in Figure 3.2, the input impedance of LNA1 at resonance frequency ω_0 can be simplified as:

$$R_{in} = \frac{1}{1/R_a + \omega_0^2 C_a^2 R_a} + r_{La} = R_{ser} + r_{La} \tag{3.4}$$

As discussed in section 2.3.2.2, in the conventional CGLNA, if the g_m value is smaller than $1/R_s$, the input impedance is not matched to the source impedance. In our LNA, capacitance C_a adds an additional degree of freedom to the input matching design. The impedance can be matched to the source by designing the value of C_a so that R_{in} equals to the source impedance, R_s, at the resonance frequency. The proposed input matching network makes it possible to implement the CG topology for cases where g_m is smaller than $1/R_s$. From (3.3) and (3.4), the capacitor C_a and inductor L_a at resonance frequency can be expressed as follow:

$$C_a = \sqrt{\frac{1/[R_a(R_{in} - r_{La})] - (1/R_a)^2}{\omega_0^2}} \tag{3.5}$$

and

$$L_a = \frac{C_a}{(1/R_a)^2 + \omega_0^2 C_a^2}. \tag{3.6}$$

The quality factor of the series network is:

$$Q_L = (\omega_0 L_a)/(R_{ser} + r_{La}). \tag{3.7}$$

The components in the series network are L_a, C_{ser} and R_{in} where, C_{ser} is $C_a(1 + 1/Q_L^2)$. According to Figure 3.2, at resonance, the series matching topology boosts the voltage at the source of M_1 by:

$$\begin{aligned}\frac{V_Y}{V_X} &= \frac{R_{ser} + 1/(j\omega_0 C_{ser})}{R_{ser} + r_{La} + 1/(j\omega_0 C_{ser}) + sL_a} = \frac{R_{ser}}{R_{ser} + r_{La}} + \frac{1/(j\omega_0 C_{ser})}{R_{ser} + r_{La}} \\ &= \frac{R_{ser}}{R_{ser} + r_{La}} - \frac{\omega_0 L_a}{R_{ser} + r_{La}} = [R_{ser}/(R_{ser} + r_{La}) - jQ_L]\end{aligned} \tag{3.8a}$$

Thus the effective transconductance and the overall voltage gain is enhanced by a gain G_{ser}, where G_{ser} is defined as:

$$G_{ser} = \sqrt{[R_{ser}/(R_{ser} + r_{La})]^2 + Q_L^2} \tag{3.8b}$$

3.1.2 Noise analysis

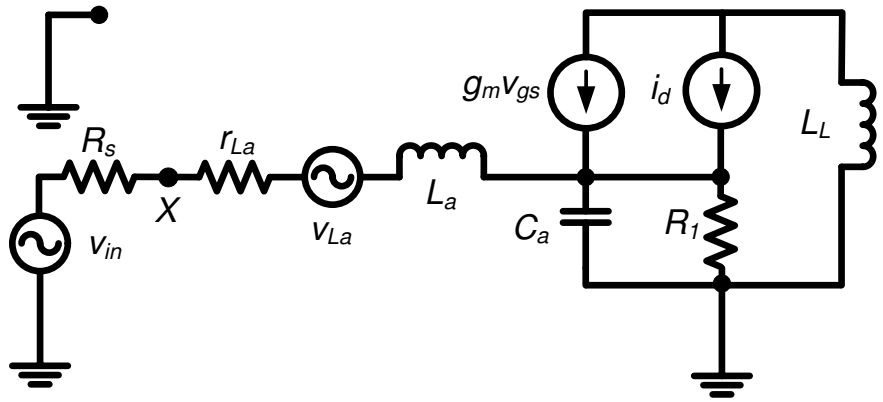

Figure 3.3: Noise analysis small signal model of LNA1

The small signal model shown in Figure 3.3 is used to derive the NF of this LNA. In the noise analysis, the effect of gate noise is omitted since its contribution to the total NF is negligible compared to other noise sources. The noise factor of the conventional CGLNA including the effect of R_1 and C_a is:

$$F_{CGLNA} = 1 + \beta_1 . \frac{\gamma}{\alpha}\frac{g_m}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_P}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)\frac{1}{r_{ds}}}\right)^2 + \beta_1 . \frac{r_{LL}}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_P}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)\frac{1}{r_{ds}}}\right)^2 + \frac{R_s}{R_1} \tag{3.9}$$

where

$$\beta_1 = (1 + R_s/R_1)^2 + (\omega_0 C_a R_s)^2 \tag{3.10}$$

If $R_1 = \infty$ and $C_a = 0$, then $\beta_1 = 1$ which is consistent with the results derived in Appendix A. M_1's channel noise, R_1's thermal noise and L_L's parasitic resistance, r_{LL},'s thermal noise account for the second, third and fourth term in (3.9) respectively. The total noise factor of the proposed LNA is derived as follow:

$$F_{L-CGLNA} = 1 + \beta_2 \frac{\gamma}{\alpha}\frac{g_m}{R_s}\left(\frac{R_s + \frac{1}{1/r_{ds}+g_m} + \frac{R_p}{1+g_m r_{ds}}}{1 + g_m R_s + (R_s + R_p)\frac{1}{r_{ds}}}\right)^2$$

$$+ \beta_2 . \frac{r_{LL}}{R_s} . \left(\frac{R_s + \frac{1}{1/r_{ds}+g_m} + \frac{R_P}{1+g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)\frac{1}{r_{ds}}}\right)^2 \qquad (3.11)$$

$$+ \left[\frac{R_s}{R_1}\left(1 + \frac{r_{La}}{R_s}\right)^2 + \frac{(\omega_0 L_a)^2}{R_1 R_s}\right] + \frac{r_{La}}{R_s}$$

where

$$\beta_2 = [1 + (R_s + r_{La})/R_1 - \omega_0^2 L_a C_a]^2 + (\omega_0 C_a R_s + \omega_0 L_a/R_1 + \omega_0 C_a r_{La})^2 \qquad (3.12)$$

The fifth terms in (3.11) is due to the thermal noise of r_{La}. The use of series input inductor L_a introduces extra noise to the circuit due to the inductor parasitic resistance r_{La}. However, the negative component which is $(-\omega_0^2 L_a C_a)$ in the expression of β_2 helps to lower the noise contribution of M_1's channel thermal noise and r_{La}'s thermal noise when compared to the conventional CGLNA. A conventional CGLNA was designed to compare its NF with LNA1. The circuits were simulated with different values of g_m such as 6 mS, 8 mS and 10 mS. The NF simulation results are shown in Figure 3.4. Our CGLNA with series input matching achieves much lower NF than the conventional CGLNA. By adding the series inductor L_a, the noise contribution from the channel thermal noise is reduced resulting in a lower NF of LNA1. The simulation results agree well with the analysis. There is a great improvement of NF. When g_m is at its lowest value which is 6 mS in our simulation, the NF improvement is up to 1.2 dB.

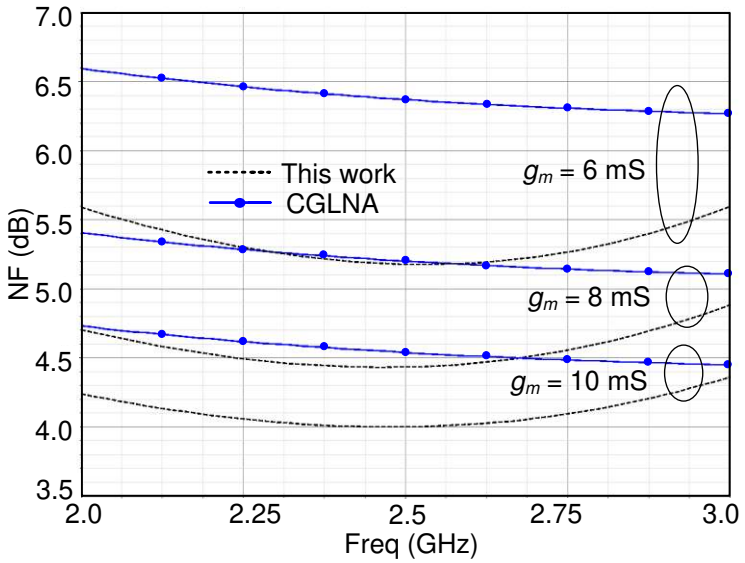

Figure 3.4: Simulated NF versus different g_m values in the 0.18µm RF CMOS technology

3.1.3 Circuit implementation

To demonstrate the idea, an LNA was designed and fabricated in a standard 0.18 µm RF CMOS technology. To further improve the gain performance of the circuit, two big capacitors C_c were placed across the two sides of a differential input stage to effectively boost the transistor's transconductance value without requiring extra dc current. The use of C_c introduced an inverting amplification, A, at the source and the gate terminal of the input device. The inverting amplification value is approximately given by the capacitor voltage division ratio: $C_c/(C_c + C_{gs})$ where C_{gs} is the parasitic gate-source capacitance of the input transistor. When C_c is designed to be much larger than C_{gs}, the transconductance is effectively boosted to $(1 + A)g_m \approx 2g_m$. This increases the voltage gain by two times, making the total improvement in voltage gain becomes $2\sqrt{[R_{ser}/(R_{ser} + r_{La})]^2 + Q_L^2}$, and the total noise factor is reduced to:

$$F_{L-CGLNA}{}' = 1 + \frac{\beta_2}{2}\frac{\gamma}{\alpha}\frac{g_m}{R_s}\left(\frac{R_s + \frac{1}{1/r_{ds}+g_m} + \frac{R_p}{1+g_m r_{ds}}}{1 + g_m R_s + (R_s + R_p)\frac{1}{r_{ds}}}\right)^2$$

$$+ \frac{\beta_2}{2}.\frac{r_{LL}}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds}+g_m} + \frac{R_P}{1+g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)\frac{1}{r_{ds}}}\right)^2 \qquad (3.13)$$

$$+ \left[\frac{R_s}{R_1}\left(1 + \frac{r_{La}}{R_s}\right)^2 + \frac{(\omega_0 L_a)^2}{R_1 R_s}\right] + \frac{r_{La}}{R_s}$$

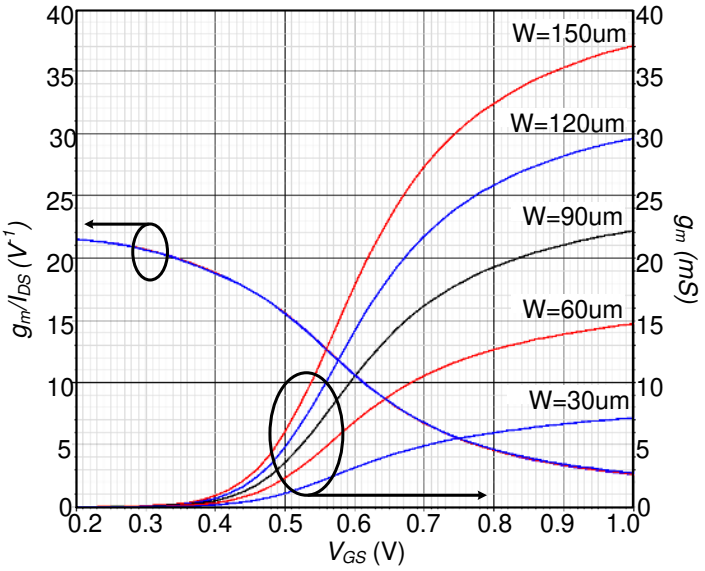

Figure 3.5: Variation of g_m and g_m/I_{DS} with V_{GS} and transistor size in the 0.18 µm RF CMOS technology

The g_m value of the input transistor is chosen based on the gain requirement. After deciding the g_m value of the input transistor, the value of C_a and L_a can be determined based on equation (3.5) and (3.6). C_a can be realized by using the parasitic capacitances of the input transistor. Extra capacitor may be added if required. In most of LNA designs, the S_{11} minimum requirement is -10 dB. This means that R_{in} can range from 30 Ω to

70 Ω. Let's say we choose $g_m = 10\,mS$, based on equation (3.5), the value of C_a is calculated to be from 0.31 pF to 1.02 pF. As long as the value of C_a is in this range, the LNA can achieve a S_{11} better than -10 dB.

Figure 3.5 shows the variation of g_m and g_m/I_{DS} with V_{GS} and transistor size in the 0.18 µm RF CMOS technology. As the transistor size increases, the g_m curve moves upward. The g_m/I_{DS} curves are almost the same for different transistor sizing. For the same g_m value, an LNA with larger transistor size has larger g_m/I_{DS} value or better gain efficiency as seen in Figure 3.5. However, this advantage comes with a NF tradeoff.

Based on equation (3.9), NF is reduced as r_{ds} decreases. For the same g_m value, an LNA with a smaller transistor size has smaller r_{ds}, therefore has better NF. Figure 3.6(a) and 3.6(b) show the NFs of the CGLNA and the proposed LNA versus different transistor sizes. The g_m value is kept constant at 10 mS for all cases. The simulation results agree well with the analysis. The NF increases as the transistor size increases. Based on the figure of merit in [91], a ratio of $(g_m/I_{DS})/(F-1)$ can be used to decide the optimum transistor size and biasing point. Figure 3.7 plots this ratio vs. transistor size at 2.4 GHz. In our simulation, the highest value occurs when the transistor width is 150 µm.

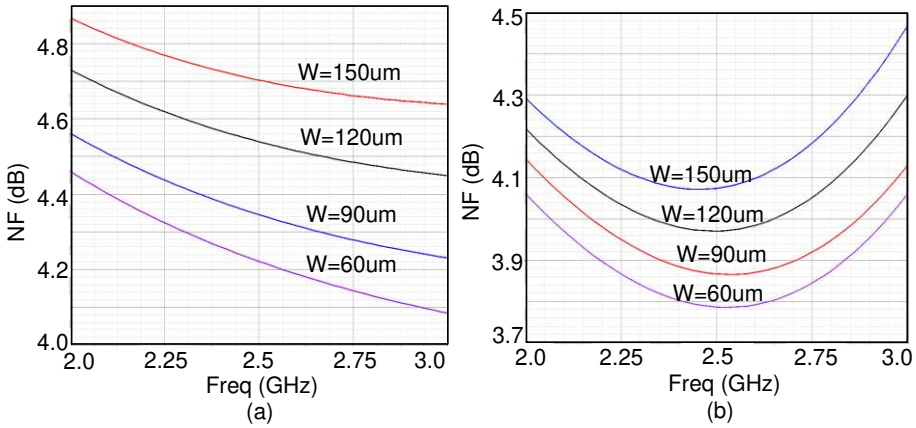

Figure 3.6: Simulated NF versus different transistor sizes at g_m =10 mS in the 0.18 µm RF CMOS technology (a) CGLNA (b) LNA1

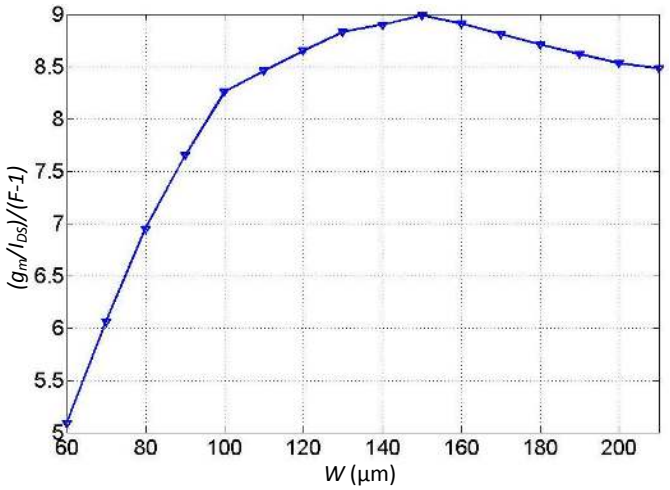

Figure 3.7: $(g_m/I_{DS})/(F-1)$ of LNA1 vs transistor size at 2.4 GHz and g_m =10 mS in the 0.18 µm RF CMOS technology

The schematic and chip micrograph of LNA1 is shown in Figure 3.8. The LNA was designed using standard V_{th} transistors, metal-insulator-metal (MIM) capacitors, and standard spiral inductors. Transistor M_{1b} and M_{2b} were added to improve the reverse isolation and reduce the Miller capacitance between the gate and drain of the input devices, M_{1a} and M_{2a}. The transistors were biased at 0.5 mA with a 1.0 V supply. Capacitor C_a is realized by the parasitic capacitances from transistor M_{1a} and M_{2a}. Capacitors C_c are designed to be large so that they are short circuit at the resonance frequency. The second stage of the LNA is a source follower buffer. It has 50 Ω output impedance to match with the 50 Ω load of the measuring equipment. The load of the first stage was tuned to 2.4 GHz using L_L and the input capacitance of the second stage. The total chip size including pads and bypass capacitors is 0.98x1.20 mm^2. The design parameters are summarized in Table 3.1.

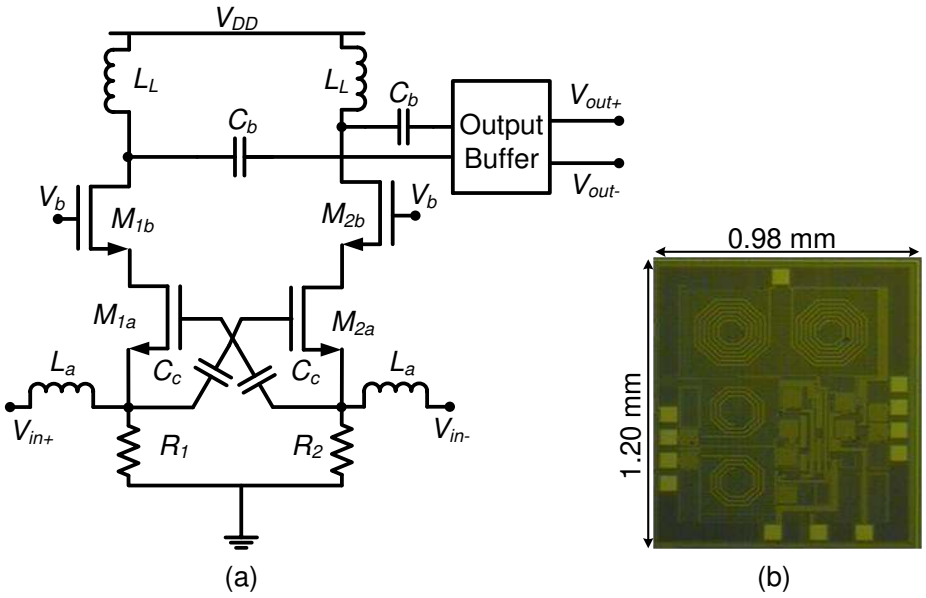

Figure 3.8: (a) Schematic and (b) Chip micrograph of LNA1

Table 3.1: Design parameters of LNA1

Design parameters	$M_{1\,a}, M_{1b}, M_{2\,a}, M_{2b}$	C_b, C_c	L_a	L_L	R_1, R_2
Value	150 µm/0.18 µm	10 pF	2.6 nH	7.8 nH	500 Ω

3.2 Measurement results and discussion

The measurement setup is shown in Figure 3.9. The LNAs are measured using the HP8510 Network analyzer which has a built-in NF personality. The measurement is based on RF-probing. The basic test setup includes a wafer probe station, the HP8510 network analyzer system and a bias supply. The network analyzer consists of a sweep synthesizer (so that measurements will be repeatable), a test set which includes two ports, a control panel, an information display, and two RF cables to hook up the design-under-test (DUT). Each port of the test set includes dual directional couplers and a complex ratio measuring device.

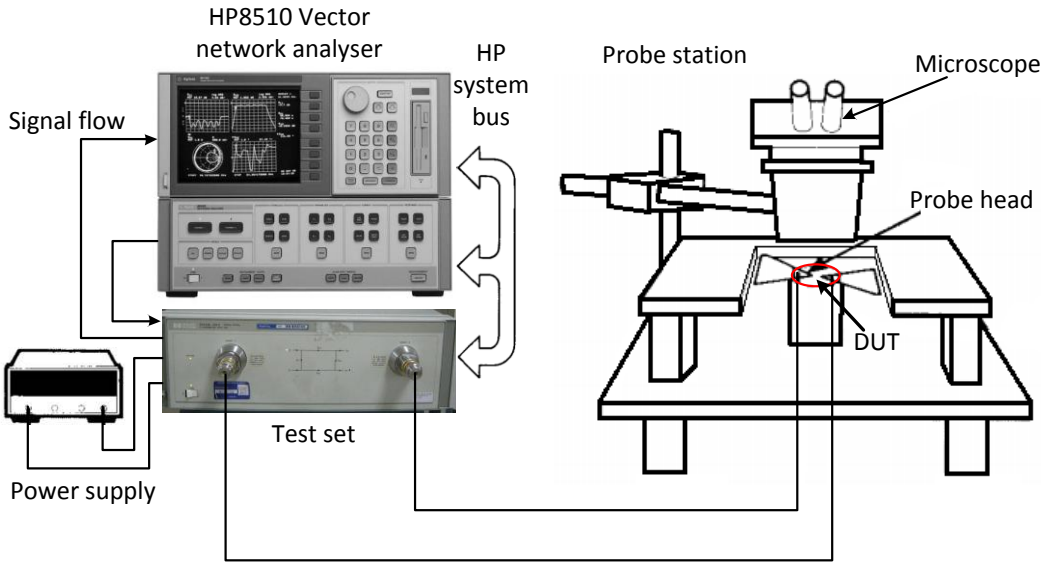

Figure 3.9: Measurement set-up

A test signal is generated by the signal generator (from the network analyzer). The test set takes the signal generator output and routes it to the DUT and it routes the signal to be measured back to the receiver of the network analyzer. The receiver makes the measurements. A network analyzer will have one or more receivers connected to its test ports. This set-up was used for the measurement of all four LNAs. Figure 3.10 shows the measured S_{11} and S_{21} of LNA1. The LNA has better than -10 dB input matching over the desired band. At 2.4 GHz, the voltage gain is 15 dB. Figure 3.11 shows the measured and simulated NF of the LNA. The measured NF exceeded the simulated NF by 1 dB. This difference can be attributed to the poor noise modeling and process variation. At 2.4 GHz, the measured NF is 5 dB.

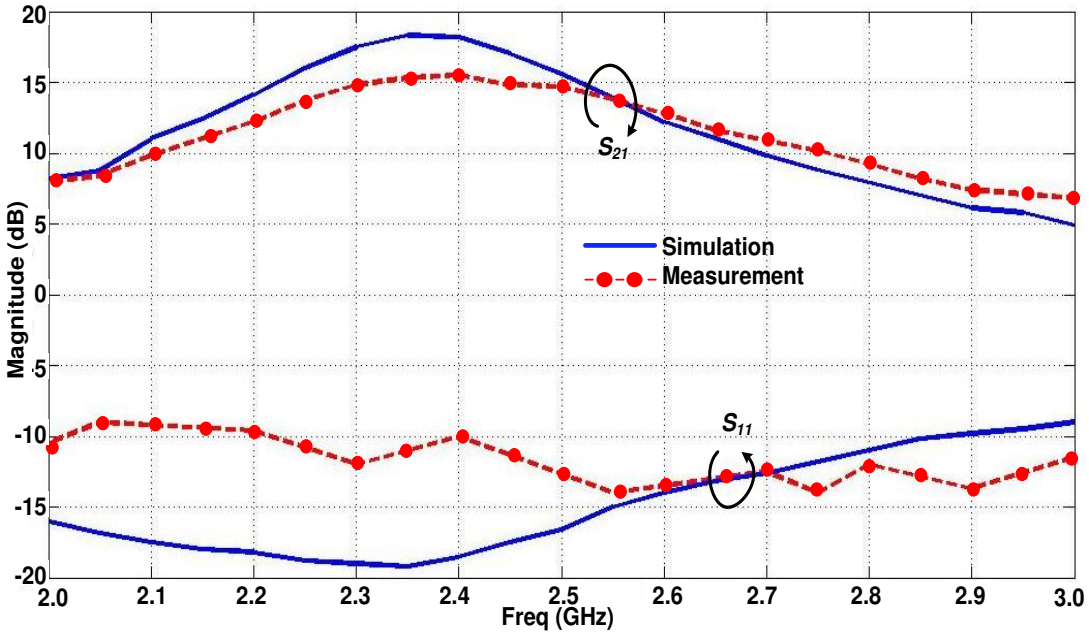

Figure 3.10: Measured and simulated S_{11} and S_{21} of LNA1

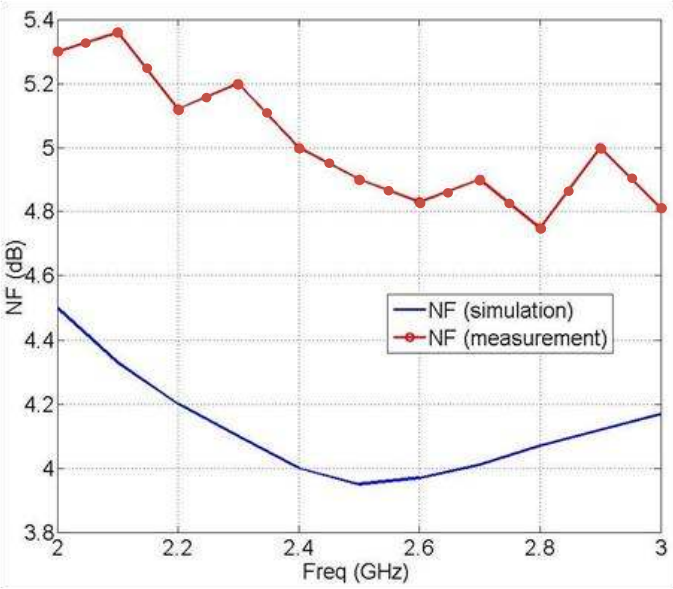

Figure 3.11: Measured and simulated NF of LNA1

Figure 3.12 shows the S_{12} and stability factor K and Δ. For an LNA to be stable, K and Δ must be larger and smaller than unity respectively. LNA1 has high reverse isolation and is stable at the frequency of interest as seen on Figure 3.12. (S_{12} = -63 dBm, K>1 and Δ<1

at 2.4 GHz). The LNA core only consumes 0.98 mW power from 1.0 V supply voltage, making it suitable for low-power applications. The measured *IIP3* of the LNA core is -19 dBm. The use of resistor at the source of transistor M_{1a} and M_{2a} together with the low supply voltage at 1.0 V has limited the linearity performance of this LNA. LNA1's performance is summarized in Table 3.2.

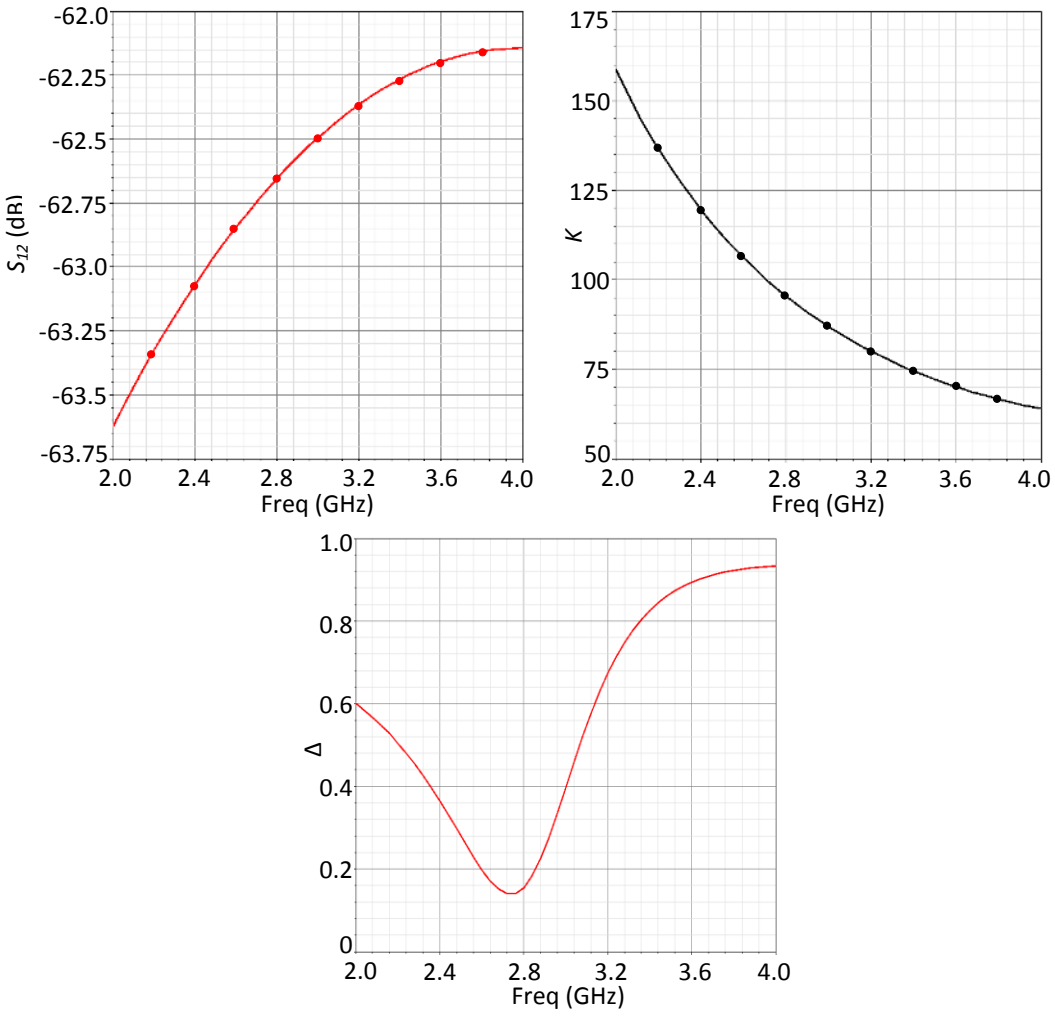

Figure 3.12: S_{12} , K and Δ of LNA1

Table 3.2: LNA1's measurement results

LNA's Specification	Requirement	Measurement results
Gain	15 dB	15 dB
NF	< 16.19 dB	5 dB
IIP3	> -19.77 dBm	-15 dBm
S_{11}	< -10 dB	-11 dB
S_{12}	< -30 dB	-63 dB

The comparisons of this LNA with recently published 2.4 GHz LNAs and state-of-the-art ultra-low power LNAs are summarized in Table 3.3. Two figure of merits (FOM) [91] are used to compare the performance of the LNAs. The *FOM1* is a function of the operating frequency, gain, noise factor, and power consumption. It is given by:

$$FOM1 = 10log_{10}\left(\frac{Freq_{(GHz)}.Gain_{(mag)}}{(F-1)_{mag}.P_{DC(mw)}}\right) \tag{3.14}$$

FOM2 includes *IIP3* and is given by:

$$FOM2 = 10log_{10}\left(\frac{Freq_{(GHz)}.Gain_{(mag)}}{(F-1)_{mag}.P_{DC(mw)}}.IIP3_{mw}\right) \tag{3.15}$$

The LNAs in [30, 43, 92, 93] have better NF but consume much more power than ours. Moreover, such low NF is not necessary for our application. The works in [21] and **[77]** have better FOM than ours. Both designs bias the transistors in sub-threshold region for high power efficiency. [21] has good FOM due to its high gain of 21.4 dB which is achieved by using large resistive load. Therefore, it can't operate at low supply voltage such as 1.0 V. **[77]** achieves the best FOM due to its low supply voltage (0.6 V).

However, it has low gain of 9.1 dB. This is due to the small inductive load of 2 nH. Our *FOM2* is low due to the low *IIP3*. In order to improve the *FOM2*, in the next designs we will increase the linearity. To improve the *FOM1*, we will reduce the NF, increase gain or reduce the power consumption.

Table 3.3: LNA1's performance comparisons

	[77]	**[95]**	**[21]**	**[30]**	**[92]**	**[93]**	**[43]**	**LNA1**
Tech (nm)	130	130	180	130	130	130	90	180
Freq (GHz)	3.0	5.1	2.4					
Pdc (mW)	0.4	1.03	1.13	6.5	17	3.2	3	0.98
Gain (dB)	9.1	10.3	21.4	13	10	16.5	15	15
NF (dB)	4.7	5.3	5.2	3.6	3.7	2.66	3	5.0
S_{11} (dB)	-17	-17.7	-19	-14	-25	-11.8	-30	-11
***IIP3* (dBm)**	-11	n/a	-11	n/a	-6.7	-4.93	-7	-19
V_{DD} (V)	0.6	0.4	1.8	1.2	1.2	1.2	0.6	1
***FOM1* (dB)**	10.4	8.32	10.33	1.07	-4.7	7.73	6.55	8.04
***FOM2* (dB)**	-0.6	n/a	-0.67	n/a	-11.49	2.8	-0.4	-10.96

3.3 Conclusion

In this chapter, an ultra-low power sub-mA series input resonance with g_m-boosting technique differential CGLNA was presented. The design methodology was explained, the proposed LNA was fabricated and its performance was compared with other works. Unlike the conventional CGLNA, the g_m value of this LNA is not fixed by the input matching condition which makes optimizing for low power possible. The LNA consumes only 0.98 mA from 1.0 V supply voltage and attains a measured NF of 5.0 dB and gain of 15 dB at 2.4 GHz. The LNA shows excellent trade-off between NF and power consumption. The measured power consumption is among the lowest in current literature. The proposed technique makes the CG topology attractive for low-power fully integrated designs.

Chapter 4: LNA2- A noise reducing technique for common-gate LNA using shunt inductor

The parallel RLC input matching network of the CGLNA limits its noise and gain performance. At resonance, the CGLNA's input impedance is $1/g_m$. Matching the input impedance of the CGLNA to the source impedance restricts the choices of power consumption and device size. In LNA1 design, we proposed a technique to overcome this limitation. Although its performance has met the requirement for the 2.4 GHz ISM band of the IEEE 802.15.4 standard, we wished to improve the NF and linearity to achieve better FOMs. In this chapter, a new CGLNA design with noise reducing technique using shunt inductor will be proposed.

4.1 Noise analysis

In LNA1 design, the source terminal of the input device is connected to ground through a large resistor. Although resistor size is much smaller than that of inductor, its noise contribution to the overall NF is quite significant. In LNA2, we decided to connect the source terminal of the input device to ground through an on-chip inductor to achieve a better NF.

4.1.1 Conventional non-cascode CGLNA

The conventional non-cascode CGLNA is shown in Figure 4.1. Inductor L_s resonates with the total capacitor at the source of M_1 at the frequency of interest. The total NF of this LNA including the effect of finite drain-source resistor, r_{ds1}, of transistor M_1 is:

$$F_{CGLNA\_1} = 1 + \frac{\gamma}{\alpha}\frac{g_{m1}}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds1} + g_{m1}} + \frac{R_L}{1 + g_{m1}r_{ds1}}}{1 + g_m R_s + (R_s + R_L)/r_{ds}}\right)^2 + \frac{R_L}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds1} + g_{m1}} + \frac{R_L}{1 + g_{m1}r_{ds1}}}{R_s + R_L + (1 + g_{m1}R_s)r_{ds1}}\right)^2 \quad (4.1)$$

as derived in Appendix A.

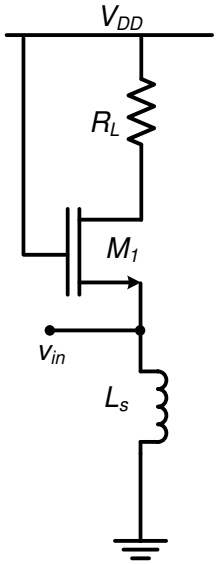

Figure 4.1: Non-cascode CGLNA

4.1.2 Conventional cascode CGLNA

A cascode CGLNA as seen in Figure 4.2(a) can be considered as a two-stage CG-CG amplifier. C_b is the by-pass capacitor. C_X includes all parasitic capacitances of node X, as well as junction capacitors and the gate–source and drain-source capacitance of M_2 and M_1. Due to the existence of the parasitic capacitance C_X, the influence of the cascode transistor to the overall NF increases. The load of stage 1 is the total impedance looking upward from node X which is:

$$Z_{L1} = \frac{1}{\frac{1 + g_{m2}r_{ds2}}{r_{ds2} + R_p} + sC_x} \tag{4.2}$$

where R_p is the equivalent parallel impedance of inductor L_L. The channel thermal noise of M_2 and the effect of r_{ds2} on the overall NF will be considered in stage 2. According to the voltage gain derived in Appendix A, the gain of stage 1 is therefore equals to:

$$A_1 = \frac{1/r_{ds1} + g_{m1}}{1/r_{ds1} + 1/Z_{L1}} = \frac{1/r_{ds1} + g_{m1}}{1/r_{ds1} + \frac{1 + g_{m2}r_{ds2}}{r_{ds2} + R_p} + sC_x} \tag{4.3}$$

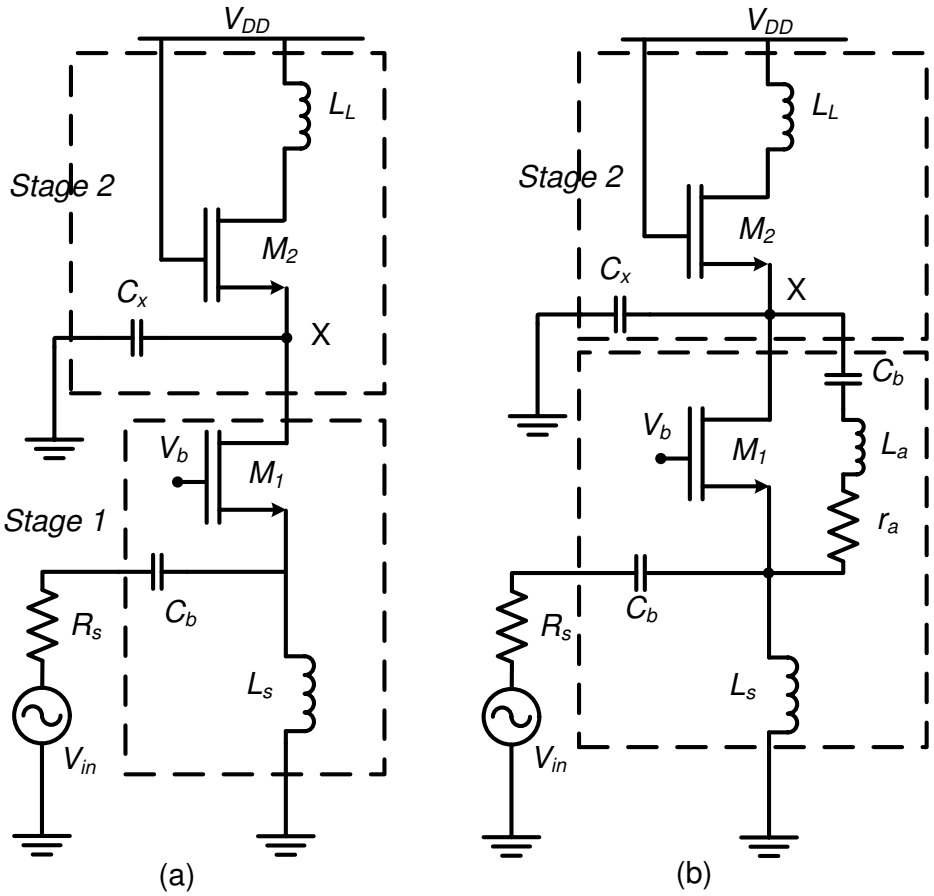

Figure 4.2: (a) Conventional cascode LNA (b) The proposed CGLNA with noise reduction technique

The total noise factor of the cascode CGLNA is:

$$F_{CGLNA\_2} = F_1 + (F_2 - 1)/A_1 \tag{4.4}$$

where F_1 and F_2 are the noise factor of stage 1 and 2. They can be calculated as:

$$F_1 = 1 + \frac{\gamma}{\alpha}\frac{g_{m1}}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds1} + g_{m1}} + \frac{Z_{L1}}{1 + g_{m1}r_{ds1}}}{1 + g_{m1}R_s + (R_s + Z_{L1})/r_{ds}}\right)^2 \tag{4.5}$$

$$\begin{aligned} F_2 = 1 + \frac{\gamma}{\alpha}\frac{g_{m2}}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds2} + g_{m2}} + \frac{R_p}{1 + g_{m2}r_{ds2}}}{1 + g_{m2}R_s + (R_s + R_P)/r_{ds}}\right)^2 \\ + \frac{r_L}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds2} + g_{m2}} + \frac{R_P}{1 + g_{m2}r_{ds2}}}{R_s + R_p + (1 + g_{m2}R_s)r_{ds2}}\right)^2 \end{aligned} \tag{4.6}$$

In (4.6), r_L is the parasitic resistance of inductor L_L. To minimize the effect of the cascode stage, one should increase the gain of stage 1. This can be done by designing the LNA such that $g_{m1} > g_{m2}$. From equation (4.4), we note that despite the improvement in reverse isolation, the use of cascode stage could introduces significant amount of noise to the overall LNA especially when A_1 is small.

4.1.3 The proposed LNA with noise reduction

In order to reduce the F_{CGLNA_2}, F_1 should be decreased and A_1 should be increased. In equation (4.5), if $r_{ds1} \to 0$, then $F_1 = 1$. In equation (4.3), if a negative imaginary component is added to the denominator of A_1 to cancel sC_x, A_1 can be increased. In the proposed LNA (LNA2), inductor L_a is added in parallel with transistor M_1. Resistor r_a is

the parasitic resistance of inductor L_a. Similar to the cascode CGLNA, the total noise factor of LNA2 is:

$$F_{CGLNA\_shunt} = F_1^{'} + \left(F_2^{'} - 1\right)/A_1^{'} \tag{4.7}$$

where $F_1^{'}$ and $F_2^{'}$ are the noise factor of stage 1 and 2 in the proposed LNA respectively and $F_2^{'}$ can be calculated using equation (4.6). In LNA2, the equivalent drain source resistance of M_1 is $r'_{ds1} = r_{ds1}//(sL_a + r_a)$. If $L_a \to 0$ then $F_1^{'} \to 1$. This means that the smaller L_a is, the lower $F_1^{'}$ becomes. The gain, $A_1^{'}$, and noise factor, F_1', of stage 1 are defined as:

$$A_1^{'} = \frac{1/r_{ds1} + 1/(sL_a + r_a) + g_{m1}}{1/r_{ds1} + 1/(sL_a + r_a) + \dfrac{1 + g_{m2}r_{ds2}}{r_{ds2} + R_p} + sC_x}$$

$$= \sqrt{\frac{\left[g_{m1} + \dfrac{1}{r_{ds1}} + \dfrac{1}{\omega_0 L_a Q_L\left(1 + \dfrac{1}{Q_L^2}\right)}\right]^2 + \left[\dfrac{1}{\omega_0 L_a\left(1 + \dfrac{1}{Q_L^2}\right)}\right]^2}{\left[\dfrac{1 + g_{m2}r_{ds2}}{r_{ds2} + R_p} + \dfrac{1}{r_{ds1}} + \dfrac{1}{\omega_0 L_a Q_L\left(1 + \dfrac{1}{Q_L^2}\right)}\right]^2 + \left[\omega_0 C_X - \dfrac{1}{\omega_0 L_a\left(1 + \dfrac{1}{Q_L^2}\right)}\right]^2}} \tag{4.8}$$

$$F_1' = 1 + \frac{\gamma}{\alpha}\frac{g_{m1}}{R_s}.\left(\frac{R_s + \dfrac{1}{1/\,r'_{ds1} + g_{m1}} + \dfrac{Z_{L1}}{1 + g_{m1}\,r'_{ds1}}}{1 + g_{m1}R_s + (R_s + Z_{L1})/\,r'_{ds1}}\right)^2 \tag{4.9}$$

They are derived using the equivalent small signal circuit in Figure 4.3 below. In equation (4.8) and (4.9), Q_L is the quality factor of L_a and ω_0 is the operating frequency. When L_a increases from zero nH to a value, L_{a_cancel}, of which the added negative

imaginary component in the denominator of $A_1^{'}$ approaches sC_x, $A_1^{'}$ increases and the noise contribution from stage 2 ($F_2^{'}$) reduces. L_{a_cancel} can be calculated as:

$$L_{a\_cancel} = 1/\left[\omega_0^2 C_x\left(1 + 1/Q_L^2\right)\right] \tag{4.10}$$

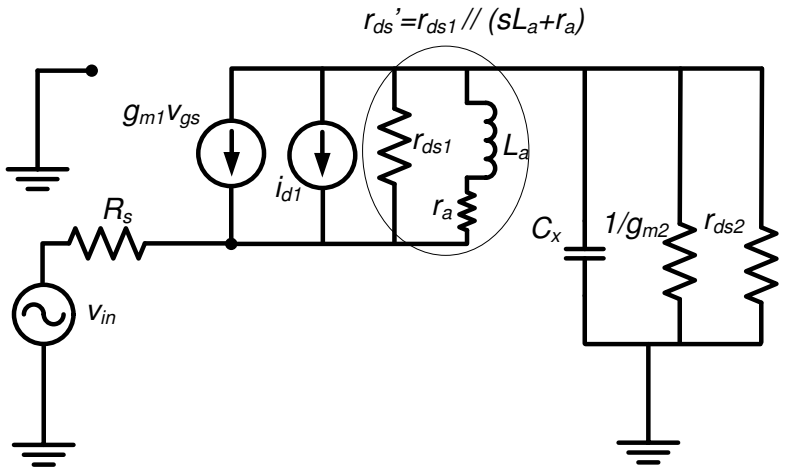

Figure 4.3: Small signal model used for noise analysis in the proposed LNA2

On another hand, when L_a approaches zero, r'_{ds1} also approaches zero which makes the denominator of the second term in equation (4.9) become infinity. As a result, $F_1' \to 1$. Therefore, there is an optimal value of L_a which results in a minimum F_{CGLNA_shunt} which is determined by $\left(F_1^{'} + \left(F_2^{'} - 1\right)/A_1^{'}\right)$. To verify the theory, we simulated the NF performance of LNA2 with various L_a values. The L_a value is swept from 0.5 nH to 15 nH. Figure 4.4 shows the noise contribution of three main noise sources in the proposed LNA which is the input source thermal noise and the channel thermal noise of M_1 and M_2. In our simulation, when L_a increases, r'_{ds1} also increases which make the noise contribution of M_1 increases. The noise contribution from M_2 decreases because the added inductor helps to lower the effect of capacitor C_x on the gain of stage 1 therefore reduces the noise from stage 2. The optimal value of L_a is found when the input source

thermal noise contribution percentage is the highest which results in the lowest NF. In our simulation, the optimal L_a value is 3 nH. Figure 4.5 shows the NF of our LNA and of the conventional cascode CGLNA. The power consumption of the two circuits is the same. As expected, the NF of the conventional cascode CGLNA is 2.3 dB worst than ours at 2.4 GHz. The measured NF exceeded the simulated NF by 1 dB due to poor noise modeling and process variation. However, the LNA2's measured NF is still better than the CGLNA's NF by 1.4 dB.

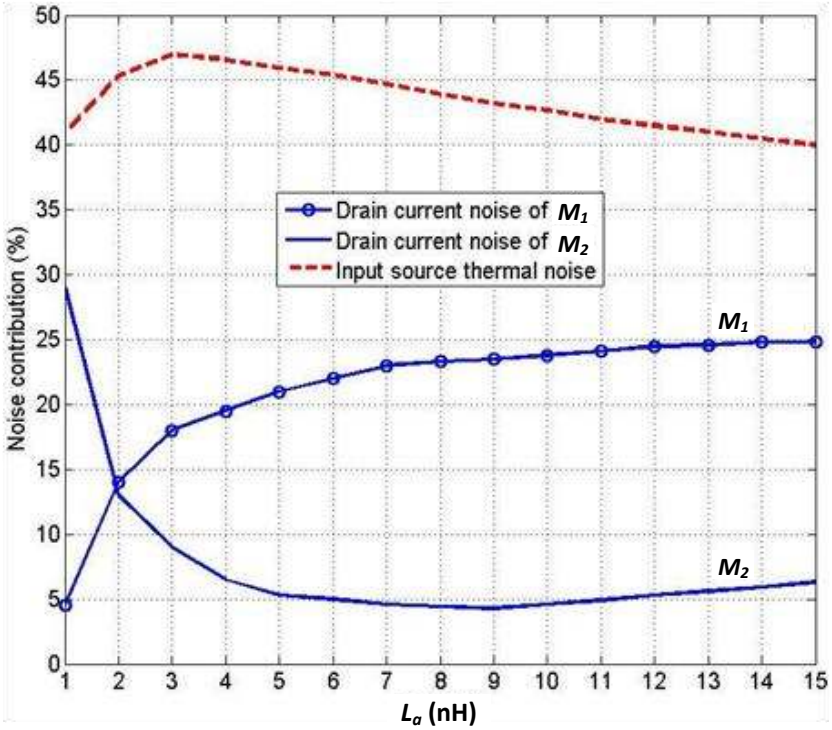

Figure 4.4: Noise contribution of different noise source in the LNAs

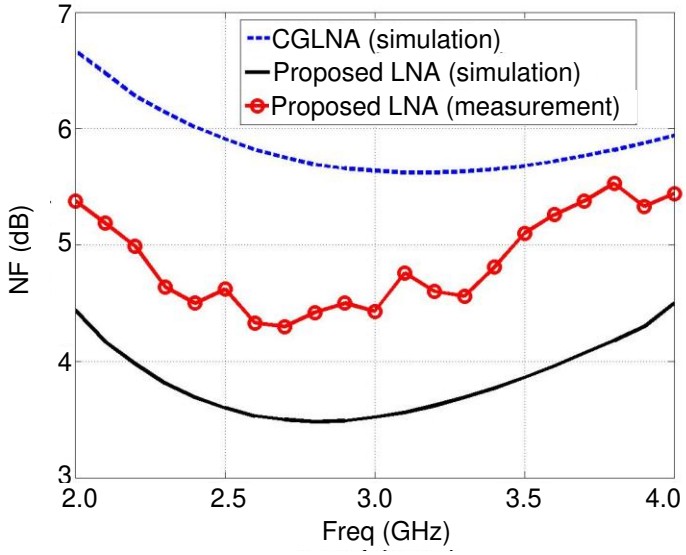

Figure 4.5: NF of LNA2 and conventional cascode CGLNA

4.2 Circuit implementation

To demonstrate the idea, LNA2 was designed in a standard 0.18 µm RF CMOS technology. The schematic of LNA2 is shown in Figure 4.6(a).

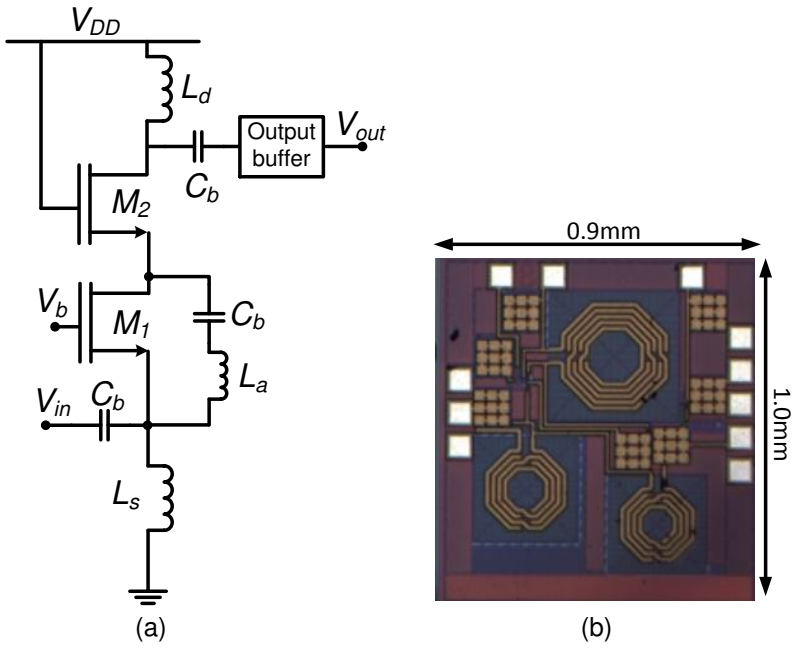

Figure 4.6: (a) Schematic and (b) Microphotograph of LNA2

On-chip inductor L_d acts as output impedance. Capacitors C_b are bypass capacitors. On-chip inductors L_s are used to tune out the total capacitances at the source nodes including pad capacitances. The second stage of the LNA acts as an output buffer. It has 50 Ω output impedance to match with the 50 Ω load of the measuring equipment. The loading effect of the buffer is determined to be about the same as the mixer loading effect on the LNA stage. The chip micrograph is shown in Figure 4.6(b). The total die area including the output buffer and ads is 0.9x1.0 mm^2. The design parameters are summarized in Table 4.1.

Table 4.1: Design parameters of LNA2

Design Parameter	M_1	M_2	L_S	L_d	L_a	C_b
Value	150 µm /0.18 µm	100 µm /0.18 µm	3.4 nH	10 nH	3 nH	10 pF

4.3 Circuit performance and discussion

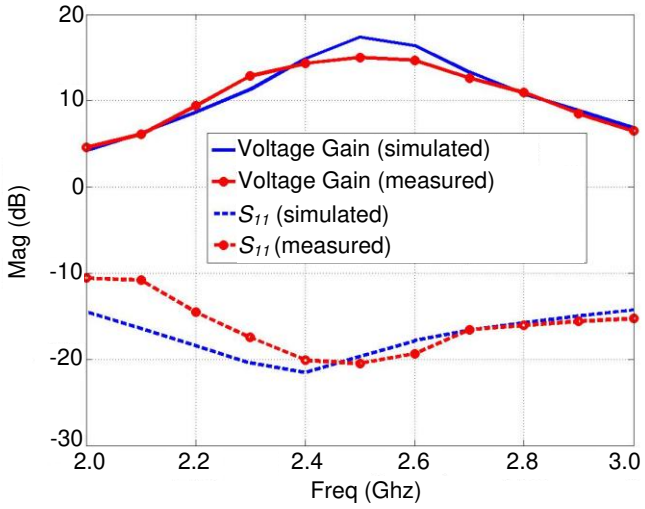

Figure 4.7: S_{11} and voltage gain of LNA2

The LNA gain and S_{11} are plotted in Figure 4.7. The LNA's peak voltage gain is 14.8 dB. This gain is slightly below the targeted gain 15 dB. Gain can be improved by

slightly increasing the power consumption. The parasitic resistance of the wire connection from L_d to V_{DD} reduces the quality factor of L_d which results in a lower gain and wider bandwidth as showed in Figure 4.8. The LNA achieves a NF of 4.5 dB at 2.4 GHz. The measured NF exceeded the simulated NF by 1 dB. This difference is attributed to the poor noise modeling and process variation and the value of inductor L_a is no longer at its optimum point which results in a poorer NF. However, the measured NF of our LNA is still much better than that of the conventional CGLNA which is 5.9 dB at 2.4 GHz as shown in Figure 4.5.

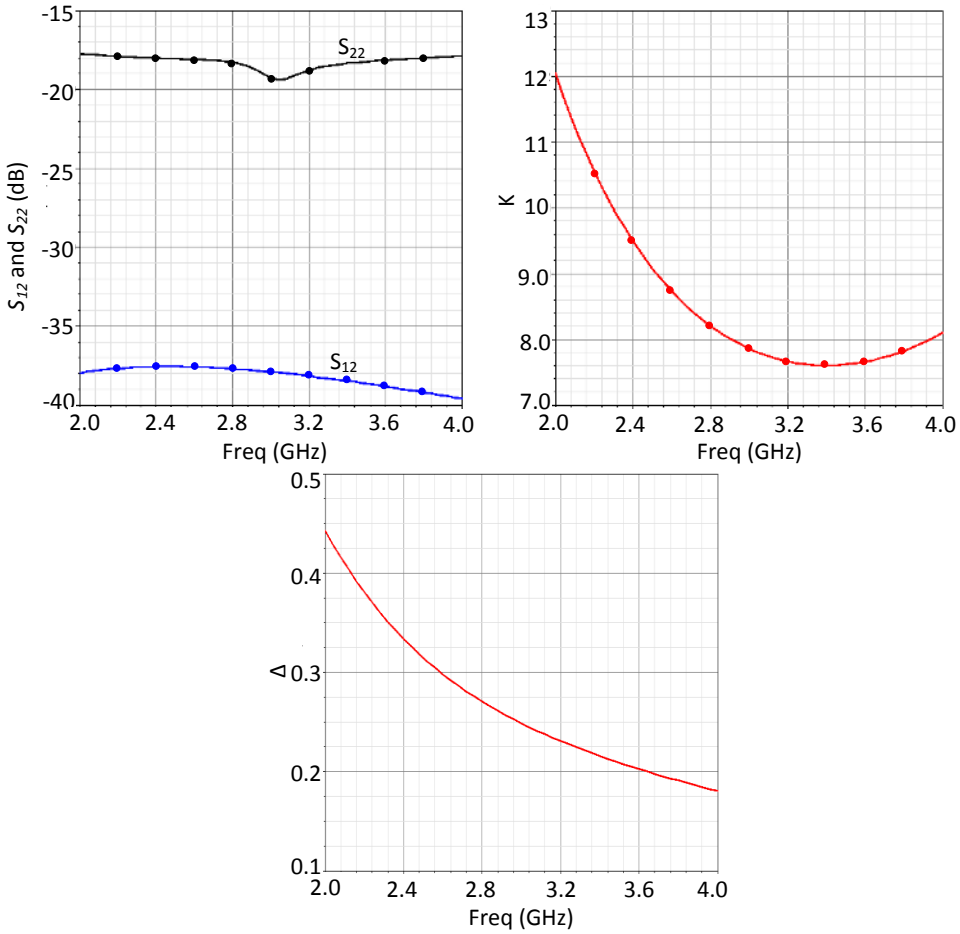

Figure 4.8: S_{11}, S_{22} , K and Δ of factor of LNA2

The LNA has good input and output matching at the frequency of interest. It has high reverse isolation and is stable at the frequency of interest as seen on Figure 4.8.

(S_{12} = -37 dB , K>1 and Δ<1at 2.4 GHz). The core LNA draws 0.95 mA from a 1.0 V supply voltage. Total power consumption is 0.95 mW. The *IIP3* is -5.7 dBm. The overall performance is summarized in Table 4.2. The comparisons of this LNA with published literatures are shown in Table 4.3.

Table 4.2 : LNA2's measurement results

LNA's Specification	Requirement	Measurement results
Gain	15 dB	14.8 dB
NF	< 16.19 dB	4.5 dB
IIP3	> -19.77 dBm	-5.7 dBm
S_{11}	< -10 dB	-20 dB
S_{12}	< -30 dB	-37 dB

Our LNA is compared with LNAs operating at 2.4 GHz and other state-of-the-art ultra-low power LNAs. The power consumption of the presented LNA is among the lowest. Compared to the LNAs operating at 2.4 GHz, our LNA consumes the least power while providing high gain and acceptable NF and *IIP3* value. Compared to LNA1, the *IIP3* and NF have been improved. The power consumption of [21, 77, and 95] is quite comparable to that of LNA2. However, their linearity is lower. The low linearity issue is due to low voltage headroom. The LNA in [21] uses large resistive load to achieve high gain which reduces the total voltage across the drain-source terminals of the transistors. The LNAs in [77, 95] operates at low supply voltages of 0.4-0.6 V which explains the low linearity. Based on the FOMs calculated in Table 4.3, the proposed LNA2 has the best *FOM2* and very high *FOM1*.

Table 4.3: LNA2's performance comparisons

	[77]	[95]	[21]	[30]	[92]	[93]	[43]	LNA1	LNA2
Tech (nm)	130	130	180	130	130	130	90	180	180
Freq (GHz)	3.0	5.1	2.4						
Pdc (mW)	0.4	1.03	1.13	6.5	17	3.2	3	0.98	0.95
Gain (dB)	9.1	10.3	21.4	13	10	16.5	15	15	14.8
NF (dB)	4.7	5.3	5.2	3.6	3.7	2.66	3	5.2	4.5
S_{11} (dB)	-17	-18	-19	-14	-25	-11.8	-30	-11	-20
***IIP3* (dBm)**	-11	n/a	-11	n/a	-6.7	-4.93	-7	-19	-5.7
V_{DD} (V)	0.6	0.4	1.8	1.2	1.2	1.2	0.6	1	1
***FOM1* (dB)**	10.4	8.32	10.33	1.07	-4.7	7.73	6.55	8.04	8.83
***FOM2* (dB)**	-0.6	n/a	-0.67	n/a	-11.49	2.8	-0.4	-11.24	3.13

4.4 Conclusion

A noise reducing technique for the cascode CGLNA was introduced in this chapter. An inductor was added parallel with the input transistor to reduce the noise from both the cascode and the input transistor. An LNA based on this technique was designed for the IEEE 802.15.4 standard. The LNA achieves a gain of 14.8 dB, NF of 4.5 dB and *IIP3* of -5.7 dBm. It consumes only 0.95 mW from 1.0 V supply voltage. The measured power consumption is among the lowest in current literature. The proposed technique makes the CG topology attractive for low-power fully integrated designs.

Chapter 5: LNA3- Ultra-low power CMOS LNA with capacitive cross-coupling technique

With the rapid growth of wireless communications, there is an increasing demand for portable wireless devices. These portable devices require low power dissipation to maximize battery lifetime. In current literature, there are two common techniques to reduce power consumption which are: reusing the drain current and operating the circuit at low supply voltage. Some low power applications, such as wireless medical telemetry, require the portable devices to operate at a low supply voltage with a small battery. Moreover, following scaling law, the power supply voltage of CMOS has been reduced progressively down to approximately 1.0 V at the 0.13 µm technology node and likely to be 0.75 V in the 45 nm technology [96]. The third LNA (LNA3) presented in this thesis is designed for very low supply voltage such as 0.6 V. It is a differential single-stage non-cascode LNA. The poor reverse isolation problem in this structure is improved by employing the capacitive cross-coupling (CCC) across the two sides of a differential input stage.

5.1 Circuit description

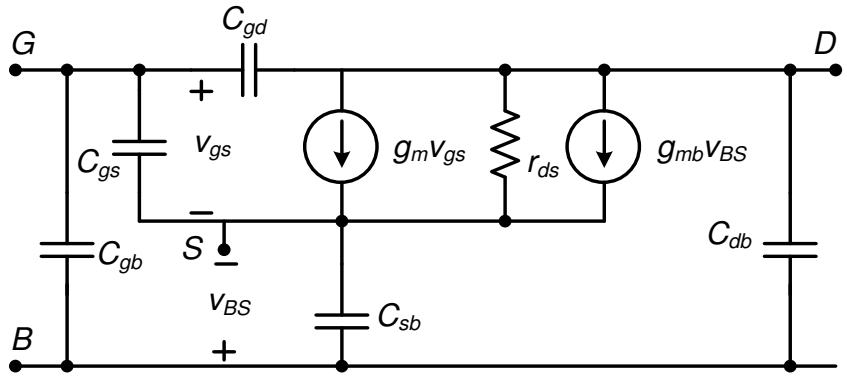

Figure 5.1: MOS small signal model

In order to operate at low supply voltage without degrading the linearity and dynamic range, the number of stacked transistors must be reduced. Using folded structure could help to lower the required voltage headroom, but would draw more dc current. Therefore, to lower the supply voltage and to reduce the power dissipation simultaneously, a circuit without folded structure is preferred. Figure 5.1 shows the CMOS transistor small signal model with its parasitic capacitances C_{gd}, C_{gs} , C_{db}, C_{gb} and C_{sb}. A single-stage non-cascode LNA has very poor reverse isolation due to the leakage from output to input through the parasitic capacitors as shown in Figure 5.2.

In the CSLNA, there are two leakage paths as shown in Figure 5.2(a). The first path is directly from the output to the input through capacitor C_{gd}. The second path is from the drain to the source terminal of transistor M_1, then from the source terminal to the input through capacitor C_{gs}. In the CGLNA, the leakage path is from the drain to the source terminal as shown in Figure 5.2(b). Since the leakage is normally dominated by the C_{gd} path, the CSLNA usually has worse reverse isolation than the CGLNA.

A low-IF or zero-IF architecture is widely implemented in most of the receiver system nowadays due to its high integration by eliminating the need for off-chip image-reject filtering after the LNA. The LNA is followed directly by a mixer. The reverse-isolation of the LNA is important as it determines the amount of LO signal that leaks from the mixer to antenna. Moreover, the LNA' stability improves as the reverse-isolation of the circuit increases. A reverse-isolation of -30 dB for an LNA is generally enough for most cases [19]. With a standard LO power of zero dBm and an average LO-RF isolation from the mixer of -40 dB [73], the LO power at the input of the LNA is therefore (-30) + (-40) = -70 dBm.

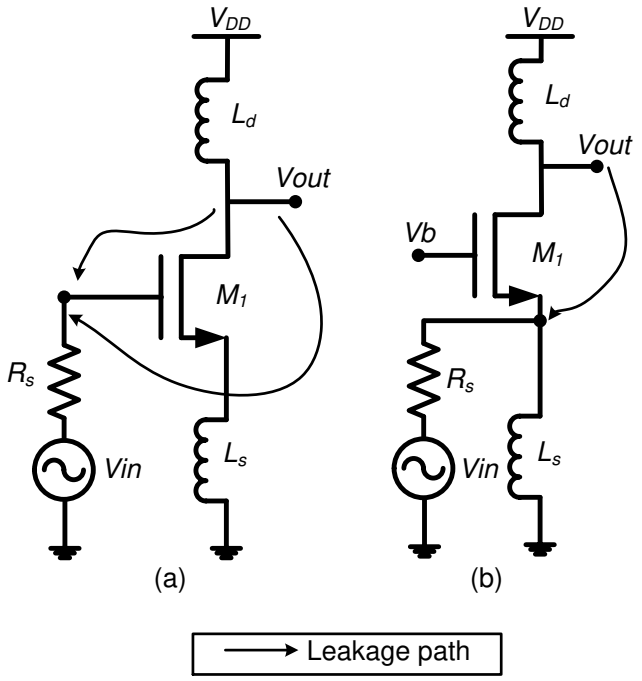

Figure 5.2: Output – input leakage path in (a) CSLNA (b) CGLNA

Figure 5.3 shows the simplified schematic of LNA3. It has a single-stage non-cascode structure to allow low-supply voltage operation and the reverse isolation is improved by using CCC across the two sides of a differential input stage. The work in [57, 58]

employed the CCC technique to improve the NF of the CGLNA. In this chapter, we will extend the analysis to the input matching, gain and reverse isolation.

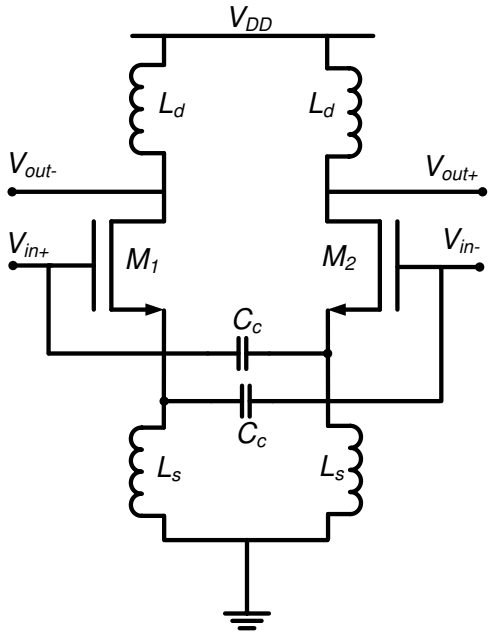

Figure 5.3: Schematic of LNA3

5.2 Performance analysis

5.2.1 Reverse isolation

In LNA3, the leakage self-cancellation mechanism helps to improve the LNA's reverse isolation. The simplified half circuits as shown in Figure 5.4 will be used to explain this mechanism. Since capacitor C_C is much larger than the parasitic capacitors, it is considered as short circuit in this analysis.

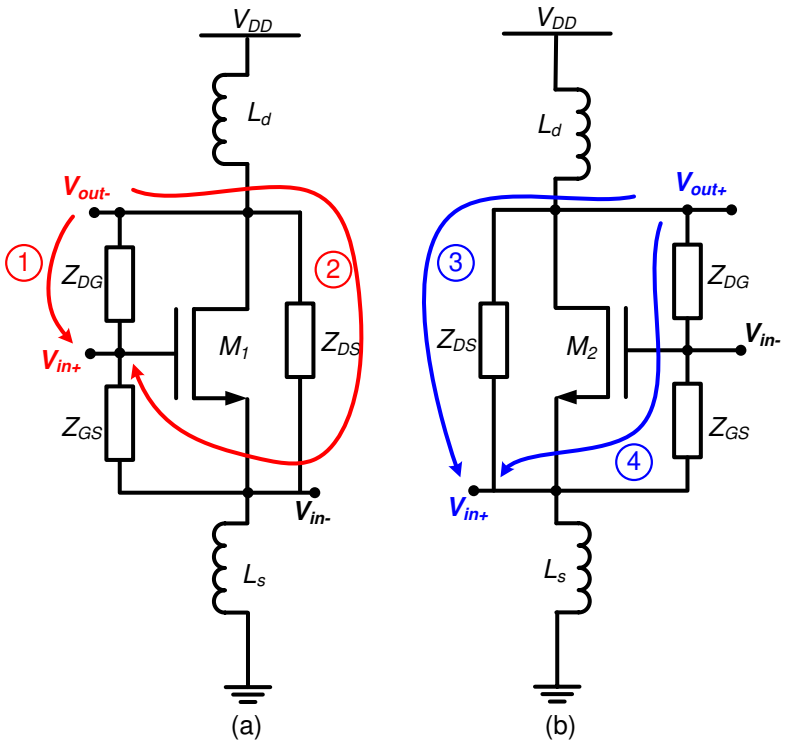

Figure 5.4: Leakage paths from (a) V_{out-} to V_{in+} (b) V_{out+} to V_{in+}

At each input node, there are leakage voltages from both V_{out+} and V_{out-} . V_{out-} is fed back to V_{in+} through paths 1 and 2 as shown in Figure 5.4(a). These two paths are the same as the leakage paths in the CSLNA. V_{out+} is fed back to V_{in+} through paths 3 and 4 as shown in Figure 5.4(b). The leakage voltages from V_{out+} and V_{out-} are 180° out of phase. This results in a leakage self-cancellation at the input which improves the reverse isolation. The same cancellation mechanism can be applied to V_{in-}. To analyze the leakage from the outputs, let us define the equivalent drain-source, drain-gate and gate-source parasitic impedances as Z_{DS}, Z_{DG} and Z_{GS} respectively. The total impedance at each input node is defined as Z_s which is equal to R_s at matching condition. Impedance Z_{DG} and Z_{GS} are:

$$Z_{DG} = 1/(sC_{gd}) \tag{5.1}$$

and

$$Z_{GS} = 1/(sC_{gs}) \tag{5.2}$$

When the substrate is connected to ground, impedance Z_{DS} is derived to be $[r_{ds}(1 + g_m Z_s)]$. At the frequency of interest, these three impedances are much larger than Z_s. The leakage factor from V_{out-} to V_{in+} is:

$$\beta_- = \frac{Z_s}{Z_{DG} + Z_s} + \frac{Z_s}{Z_{DS} + Z_s} \cdot \frac{Z_s}{Z_{GS} + Z_s} \tag{5.3}$$

The leakage factor from V_{out+} to V_{in+} is:

$$\beta_+ = \frac{Z_s}{Z_{DS} + Z_s} + \frac{Z_s}{Z_{DG} + Z_s} \cdot \frac{Z_s}{Z_{GS} + Z_s} \tag{5.4}$$

To maximize the leakage cancellation, the leakage factors from V_{out+} and V_{out-} to V_{in+} should be matched. Equalizing equation (5.3) with (5.4) results in a condition of $Z_{DS} = Z_{DG}$. Practically, it is hard to achieve a complete cancelation since matching of parasitic components is a difficult task. Luckily, in most of the applications, the reverse isolation requirement is not very strict. A value of better than -30 dB is acceptable for S_{12} parameter. Therefore, a complete leakage cancellation is not required. Over-designing the reverse isolation of the LNA may result in trade-offs with other performance parameters such as gain, NF and chip area. In non-cascode CS structure, high reverse isolation is hardly achievable due to the leakage paths from output to input through the parasitic capacitors. By reducing the transistor's size of the CSLNA, the parasitic capacitors become smaller, resulting in a better S_{12} but smaller gain and higher NF. In LNA3, the

leakage self-cancellation at the input makes the -30 dB target more achievable. The high reverse isolation in LNA3 is achieved by the leakage self-cancellation mechanism.

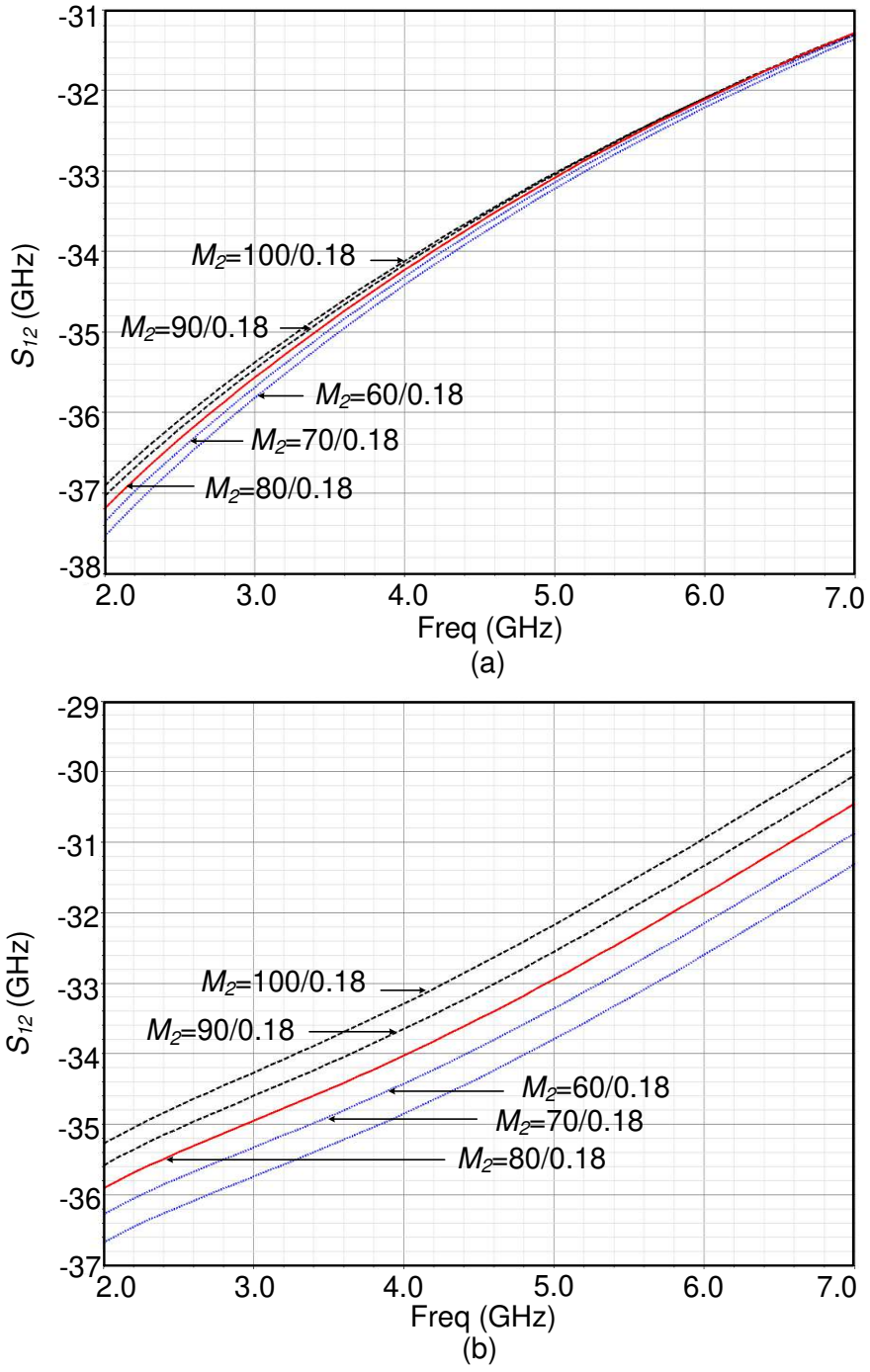

Figure 5.5: S_{12} variation due to transistor mismatch (a) LNA3 (b) CGLNA

Figure 5.5 shows the variation of the S_{12} of LNA3 and CGLNA with respect to the transistor mismatch of up to ± 25 %. M_1's size is fixed at 80 µm/0.18 µm while M_2 size is varied from 60 µm/0.18 µm to 100 µm/0.18 µm. Due to the cross-coupling structure; the mismatch leakage appears at both the negative and positive input. Therefore, the S_{12} value doesn't deviate much from its ideal case as compared to the CGLNA.

5.2.2 Noise

The noise factor [57] of the CGLNA ignoring the effects of gate noise is:

$$F_{CGLNA} = 1 + \frac{4kT\gamma g_{d0}\Delta f}{\frac{4kT}{R_s\Delta f}}\left(\frac{1}{g_m R_s}\right)^2 = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_s} \tag{5.5}$$

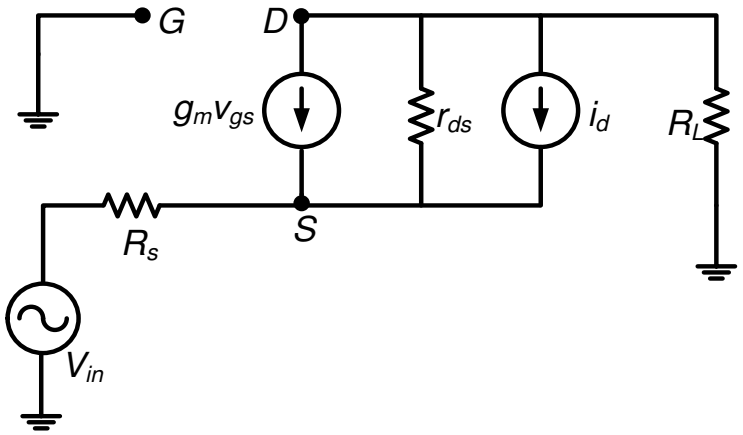

Figure 5.6: CGLNA small signal noise analysis

To find a way to improve the CG's NF, we investigated the NF derivation of the CGLNA. To simplify the derivation, we assume an infinite drain-source resistance of the input transistor. In this analysis, we will differentiate the small-signal transconductance of the MOSFET with the effective trans-conductance of the active stage at the source terminal. Equation (5.5) can be derived using the small signal circuit in Figure 5.6. There are two noise sources that mainly contribute to the circuit noise factor. One is the source

resistor current noise, $\overline{\iota_n^2(v_{in})}$, and the other is the transistor' channel thermal noise, $\overline{\iota_n^2(\iota_d)}$. Using superposition theorem, the output current noise [57] due to these two noise sources are, respectively:

$$\overline{\iota_n^2(v_{in})} = G_{m,eff}^2 \frac{\left(\frac{1}{G_{m,eff}}\right)^2}{\left(R_S + \frac{1}{G_{m,eff}}\right)^2} 4kTR_s\Delta f = G_{m,eff}^2 \frac{1}{\left(G_{m,eff}R_S + 1\right)^2} 4kTR_s\Delta f \tag{5.6}$$

and

$$\overline{\iota_n^2(\iota_d)} = \frac{1}{\left(1 + G_{m,eff}R_s\right)^2} 4kT\gamma g_{do}\Delta f = \frac{1}{\left(1 + G_{m,eff}R_s\right)^2} 4kT\frac{\gamma}{\alpha} g_{mi}\Delta f \tag{5.7}$$

where g_{do} equals to $g_{mi}\gamma/\alpha$. The total noise factor [57] is:

$$F_{CGLNA} = \frac{\overline{\iota_n^2(v_{in})} + \overline{\iota_n^2(\iota_d)}}{\overline{\iota_n^2(R_s)}} = 1 + \frac{\gamma}{\alpha}\frac{g_{mi}}{\frac{1}{R_s}}\left(\frac{1}{G_{m,eff}R_s}\right)^2 \tag{5.8}$$

In (5.8), g_{mi} represents the small-signal transconductance of the MOSFET and $G_{m,eff}$ is the effective trans-conductance of the active stage at the source terminal. In others words, g_{mi} is related to channel thermal noise and $G_{m,eff}$ to input matching. In a conventional CGLNA, the requirement of $G_{m,eff} = g_{mi} = 1/R_s$ constrains the lower bound on the noise factor to $(1 + \gamma/\alpha)$. Noted, however, that if $G_{m,eff}$ is boosted independently by modifying the input matching condition, F_{CGLNA} will be reduced [57].

LNA3 was designed based on the g_m-boosting scheme in [57] wherein an amplification, $-A$, is introduced between the source and the gate terminal of the input device, *M*, so that:

$$G_{m,eff} = (1 + A)g_{mi} \tag{5.9}$$

The inverting amplification value, A, for the topology of LNA3 is approximately given by the capacitor voltage division ratio:

$$A = \frac{C_c}{C_c + C_{gs}} \tag{5.10}$$

When C_c is chosen to be much larger than C_{gs}, the amplification amplitude, A, can be approximated to one. Therefore, the transconductance is effectively boosted to:

$$G_{m,eff} \approx 2g_{mi} \tag{5.11}$$

and the noise factor [57] is:

$$F_{CCCLNA} = 1 + \frac{\gamma}{\alpha}\frac{g_{mi}}{\frac{1}{R_s}}\left(\frac{1}{2g_{mi}R_s}\right)^2 = 1 + \frac{\gamma}{\mathbf{2}\alpha}\frac{1}{\mathbf{2}g_{mi}R_s} \tag{5.12}$$

When the input is matched, the LNA3's noise factor is $1 + \gamma/(\mathbf{2}\alpha)$. This NF is lower than that of the CGLNA which is $1 + (\gamma/\alpha)$. In addition, to achieve the same matching condition as the LNA3, the CGLNA requires double amount of power consumption. Detailed analysis on LNA3's input matching condition will be shown in section 5.2.3.

5.2.3 Gain and input matching

The voltage gain is:

$$A_{v,CCC} = G_{m,eff} Z_L = 2 g_{mi} Z_L \tag{5.13}$$

where Z_L is the load impedance. Drawing the same current consumption, LNA3 provides double gain when compared to the conventional CGLNA. The input impedance of the LNA3 can be found using the small signal circuit in Figure 5.7. Capacitors C_c are very large so they were considered as short circuit in this analysis.

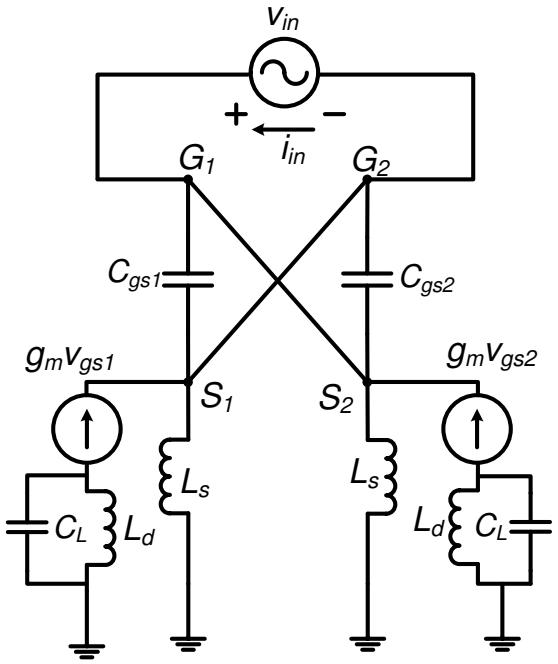

Figure 5.7: LNA3's small signal input impedance analysis

The differential input impedance is defined as:

$$R_{in,CCC,diff} = \frac{v_{in}}{i_{in}} \tag{5.14}$$

where i_{in} is:

$$i_{in} = v_{in}sC_{gs1} + \frac{v_{in}}{2sL_2} + g_{mi}v_{in} + v_{in}sC_{gs2} \tag{5.15}$$

$$= v_{in}\left(sC_{gs1} + sC_{gs2} + \frac{1}{2sL_2} + g_{mi}\right)$$

By taking $C_{gs1} = C_{gs2} = C_{gs}$, $L_1 = L_2 = L$ and substituting (5.15) into (5.14), R_{in} can be expressed in greater detail:

$$R_{in,CCC,diff} = \frac{v_{in}}{i_{in}} = \frac{1}{2sC_{gs} + \frac{1}{2sL} + g_{mi}} \tag{5.16}$$

The single input impedance is therefore:

$$R_{in,CCC} = \frac{R_{in,CCC,diff}}{2} = \frac{1}{4sC_{gs} + \frac{1}{sL} + 2g_{mi}} \tag{5.17}$$

At resonance frequency, $R_{in,CCC}$ simply becomes $1/(2g_{mi})$. Therefore, the matching condition for the LNA3 is:

$$1/(2g_{mi}) = R_s \tag{5.18}$$

The resonance frequency is:

$$\omega_{0,CCC} = \frac{1}{\sqrt{4LC_{gs}}} \tag{5.19}$$

In the case of the CGLNA, the matching condition and the resonance frequency are, respectively:

$$1/g_{mi} = R_s \tag{5.20}$$

and

$$\omega_{0,CG} = \frac{1}{\sqrt{LC_{gs}}} \tag{5.21}$$

From equations (5.13) and (5.18)-(5.20), we can see that the CGLNA requires double value of g_{mi} or double current consumption and four times larger source inductor, L_s, to achieve the same matching condition and same voltage gain with LNA3.

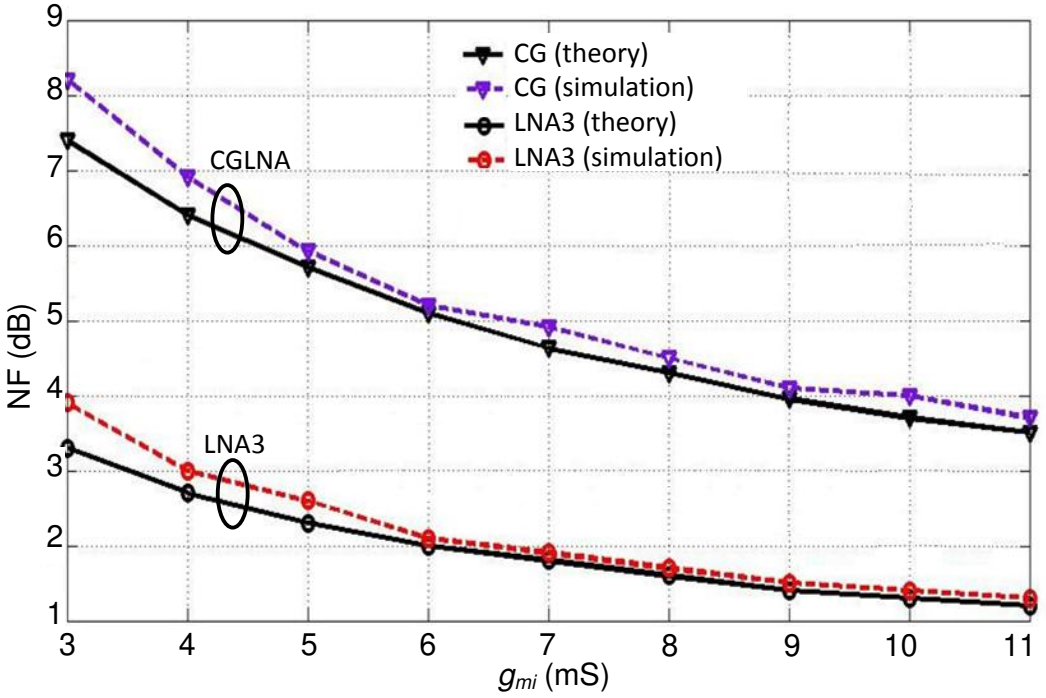

Figure 5.8: NF of CGLNA and LNA3

In order to verify the analysis, a CGLNA was simulated to compare its performance with LNA3. The current consumption and circuit components are the same as LNA3. Plotting of NFs and input impedances of the two LNAs versus the input device's transconductance, g_{mi}, at the resonance frequency are shown in Figure 5.8 and

Figure 5.9. The dotted lines represent the simulation data and the solid lines represent the theoretical analysis data. The simulation results agree well with the analysis. As shown in Figure 5.8, the NF of LNA3 is much better than of the CGLNA (3 dB lower). Figure 5.9 illustrates the advantage of LNA3 over CGLNA in term of input matching. At the same g_{mi} value or the same power consumption, LNA3 achieves a much better match to the 50 Ω source impedance than the CGLNA.

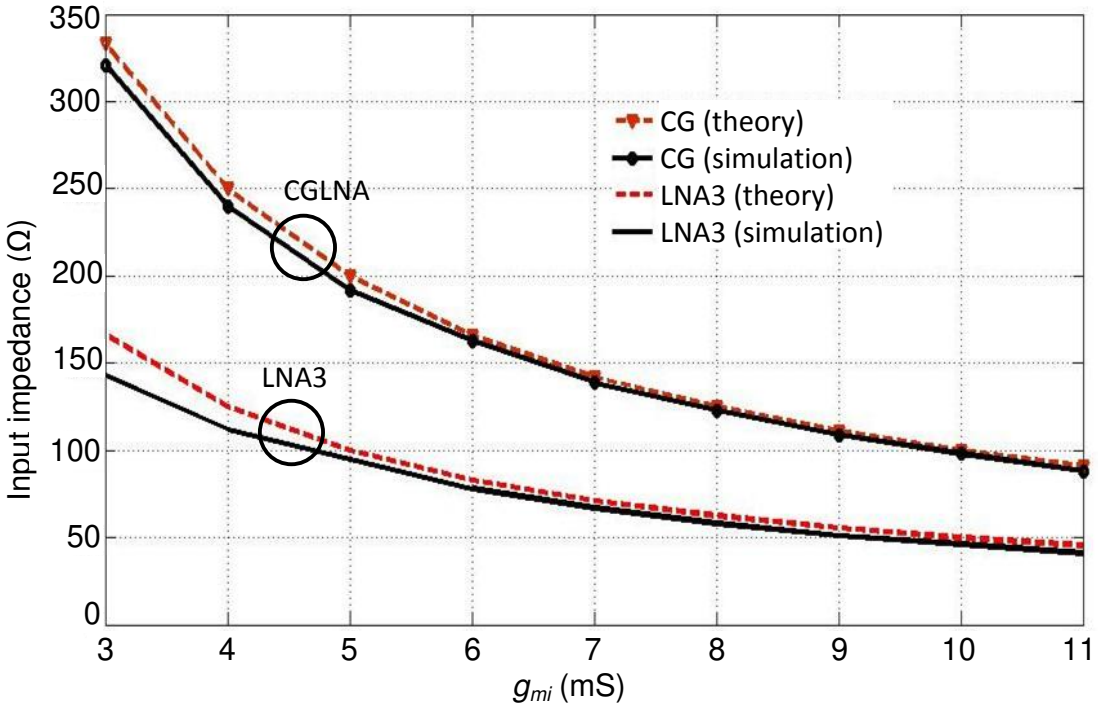

Figure 5.9: Input impedance of CGLNA and LNA3

5.3 Circuit Implementation

Figure 5.10 shows the schematic of LNA3 designed to operate at 0.6 V supply voltage. The second stage of the LNA acts as an output buffer. It has 50 Ω output impedance to match with the 50 Ω load of the measurement equipment. The loading effect of the buffer is determined to be about the same as the mixer loading effect on the LNA stage. On-chip inductors L_d act as output impedance. Since the LNA is designed for

low supply voltage such as 0.6 V, an inductive load is preferred than a resistive load. The use of resistive load will reduce the voltage headroom across the transistor significantly. Capacitors C_c are used to cross couple M_1 and M_2. Capacitors C_1 and C_2 are bypass capacitors. On-chip inductors L_s are used to tune out the total capacitances at the source nodes including pad capacitances. The design parameters are summarized in Table 5.1.

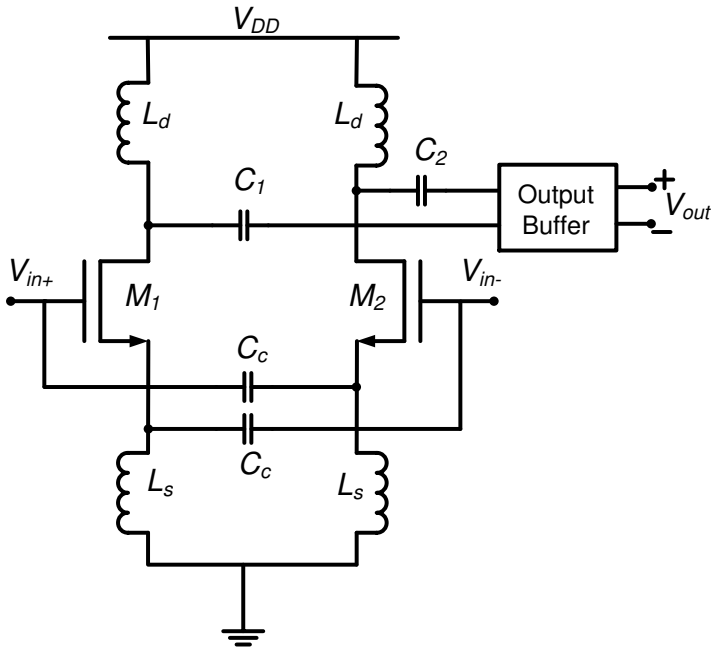

Figure 5.10: Schematic of LNA3

Table 5.1: Design parameters of LNA3

Parameter	M_1 , M_2	L_S	L_d	C_c	C_1 ,C_2
Value	72 µm	4.2 nH	8 nH	8 pF	10 pF

5.4 Measurement results and discussions

The prototype of LNA3 is fabricated in a six-metal 0.18 µm RF CMOS technology for the 2.4 GHz ISM band. The chip micrograph is shown in Figure 5.11. The total die area including the output buffer and pads is 1.2x1.0 mm^2.

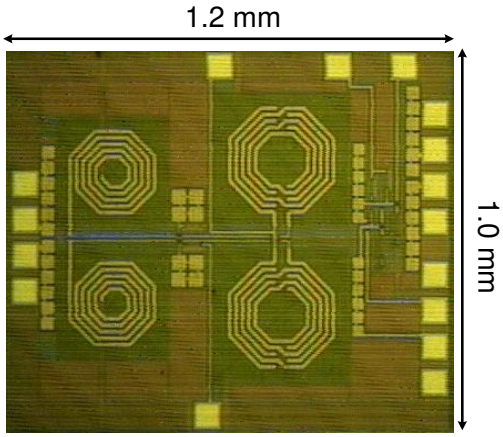

Figure 5.11: Chip micrograph of LNA3

The simulated and measured voltage gain is plotted in Figure 5.12. LNA3's voltage gain is 14 dB at 2.4 GHz. Gain can be improved by increasing the power consumption to meet the target 15 dB gain.

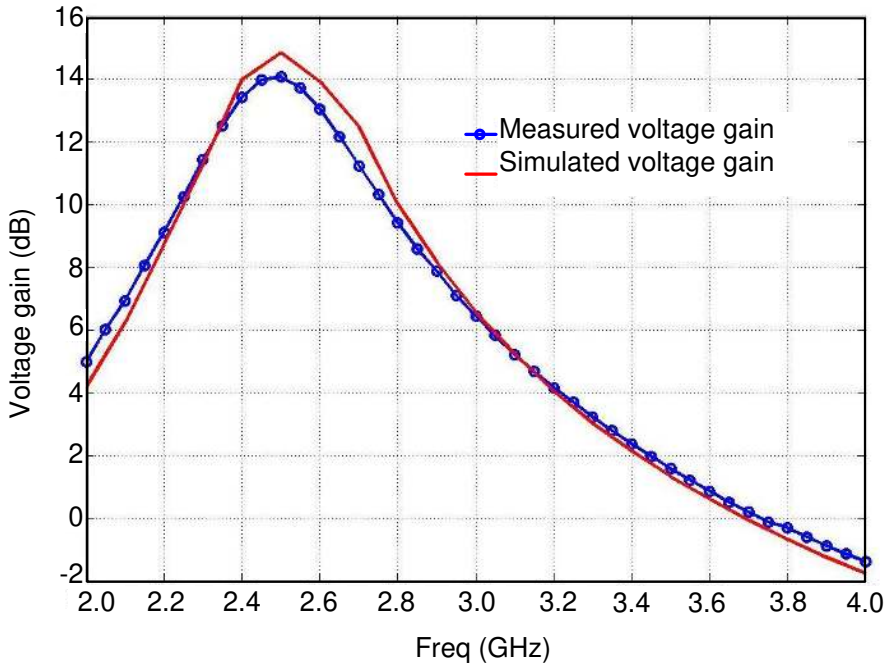

Figure 5.12: Simulated and measured voltage gain of LNA3

The simulated and measured NF is shown in Figure 5.13. LNA3 achieves a NF of 3.55 dB at 2.4 GHz.

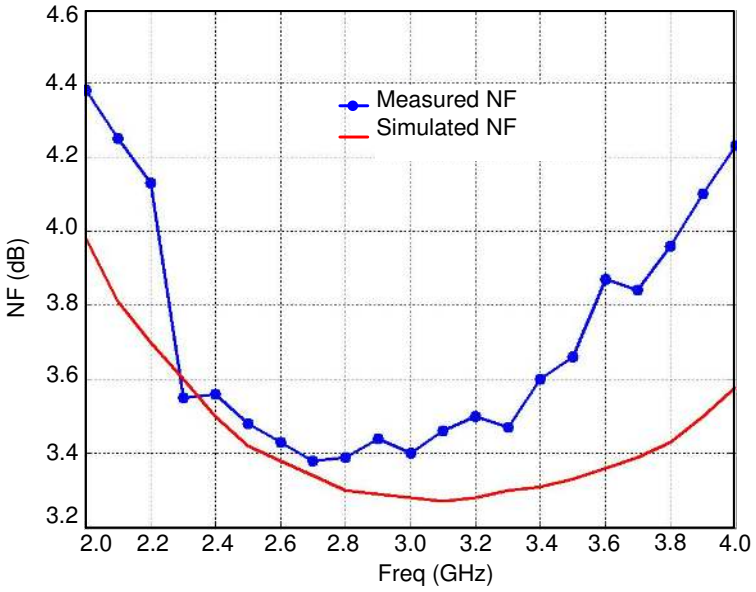

Figure 5.13: Simulated and measured NF of LNA3

The comparison between the measured and simulated S_{11} and S_{22} is plotted in Figure 5.14. LNA3 has good input/output matching. The S_{11} value is better than -22 dB and the S_{22} value is better than -15 dB at 2.4 GHz.

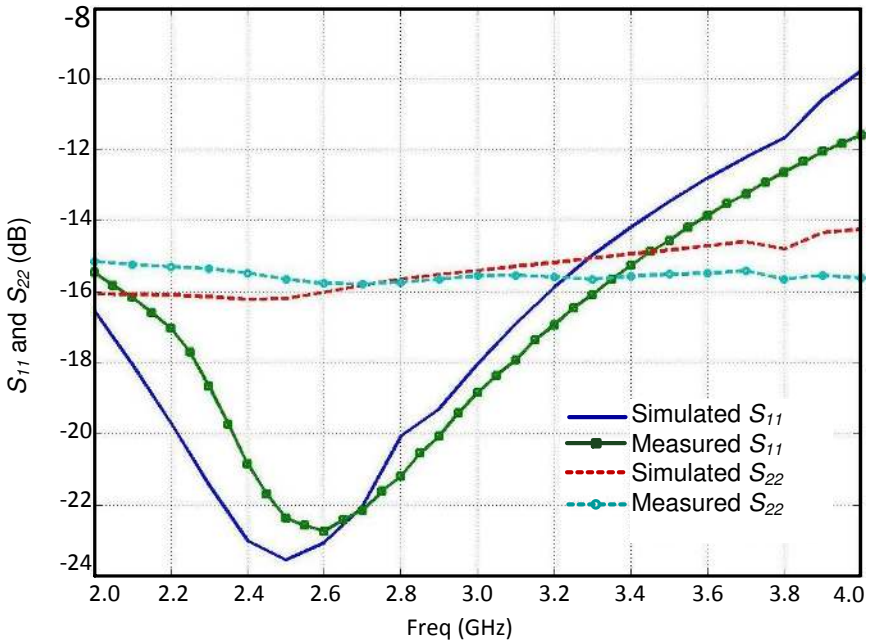

Figure 5.14: S_{11} and S_{22} of LNA3

The simulated and measured S_{12} is shown in Figure 5.15. LNA3 has good reverse isolation of -35 dB. There is a 2 dB discrepancy between the two plots. This can be explained through the deviation of transistor's parasitic capacitor and resistor in silicon vs. simulation models.

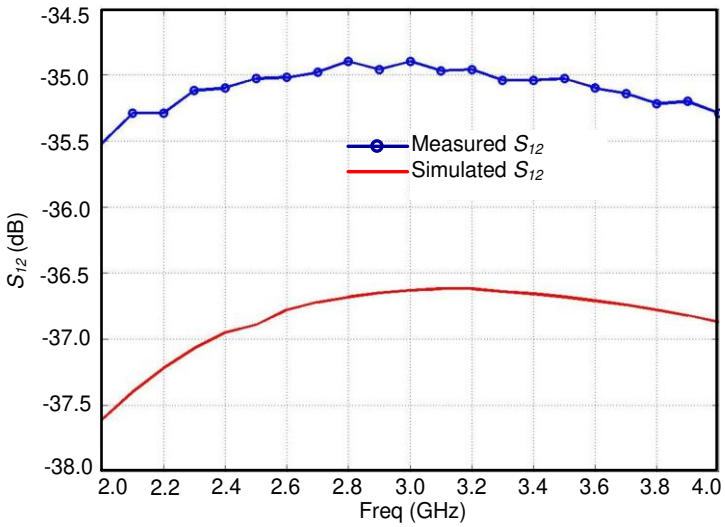

Figure 5.15: S_{12} of LNA3

The LNA is also stable at the frequency of interest as shown in Figure 5.16 (K=9 and Δ=0.24 at 2.4 GHz). The core of LNA3 draws 0.83 mA from a 0.6 V voltage supply. Total power consumption is 0.5 mW.

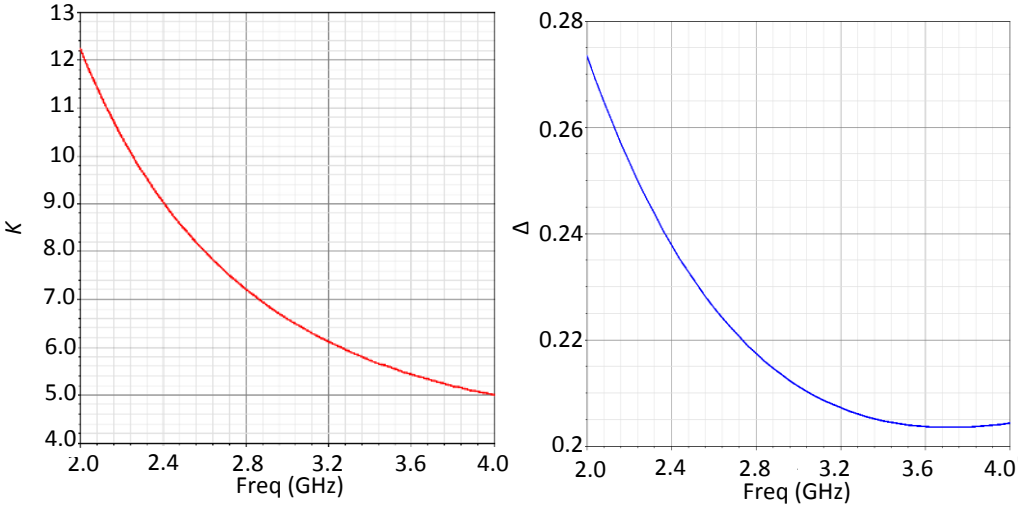

Figure 5.16: K and Δ of LNA3

Table 5.2: LNA3's measurement results

LNA's Specification	Requirement	Measurement results
Gain	15 dB	14 dB
NF	< 16.19 dB	3.55 dB
IIP3	> -19.77 dBm	-6.8 dBm
S_{11}	< -10 dB	-22 dB
S_{12}	< -30 dB	-35 dB

Table 5.3: LNA3's performance comparisons

	[77]	[95]	[21]	[30]	[92]	[93]	[43]	LNA1	LNA2	LNA3
Tech (nm)	130	130	180	130	130	130	90	180	180	180
Freq (GHz)	3.0	5.1	2.4							
Pdc (mW)	0.4	1.03	1.13	6.5	17	3.2	3	0.98	0.95	0.5
Gain (dB)	9.1	10.3	21.4	13	10	16.5	15	15	14.8	14
NF (dB)	4.7	5.3	5.2	3.6	3.7	2.66	3	5.2	4.5	3.55
S_{11} (dB)	-17	-18	-19	-14	-25	-11.8	-30	-11	-20	-22
***IIP3* (dBm)**	-11	n/a	-11	n/a	-6.7	-4.93	-7	-19	-5.7	-6.8
V_{DD} (V)	0.6	0.4	1.8	1.2	1.2	1.2	0.6	1	1	0.6
***FOM1* (dB)**	10.4	8.32	10.33	1.07	-4.7	7.73	6.55	8.04	8.83	12.88
***FOM2* (dB)**	-0.6	n/a	-0.67	n/a	-11.49	2.8	-0.4	-11.24	3.13	6.08

LNA3's performance is summarized in Table 5.2. The comparisons of LNA3 with published literatures are shown in Table 5.3. The power consumption of LNA3 is among the lowest. The power consumption of [77] is quite comparable to our design. However its NF is 1.2 dB higher and its gain is 4.9 dB lower than that of LNA3 which explain the lower FOMs. The LNA in [77] employs the cascode structure to provide high reverse isolation. However, due to the low voltage headroom across each transistor, it has worst linearity than that of LNA3. Based on the FOMs calculated in Table 5.3, LNA3 shows comparable performances to the other designs.

5.5 Conclusion

LNA3 was designed based on the CCC technique. The conventional single-stage non-cascode CSLNA normally has better NF but lower reverse-isolation. The CGLNA on the other hand has better reverse-isolation but much higher NF. The CCC technique introduces the self-cancellation of the output-to-input leakage, therefore solves the reverse-isolation problem in CSLNA. The LNA using this technique can also achieve NF much lower than the CGLNA. Novel analysis on the reverse-isolation and input matching of LNA3 was performed. Other analysis on gain and NF was also presented to show the advantages over the conventional CS and CGLNA. The design is very suitable for low supply voltage such as 0.6 V. At 2.4 GHz, it has good reverse-isolation of -35 dB and good input matching of -22 dB. The total voltage gain is 14 dB and the LNA draws only 0.83 mA from a 0.6 V supply voltage.

Chapter 6: LNA4- A high gain LNA utilizing π-match and capacitive feedback input network

In the previous chapters, three ultra-low power LNAs were proposed. They were optimized for low power and low NF. The three LNAs were based on the CG topology which may limit their gain performance. The fourth LNA (LNA4) was designed for the receiver system where high LNA gain is required. For example, if passive mixer is used after the LNA for frequency conversion, high LNA gain is needed to compensate for the mixer's loss. The L-CSLNA is commonly used for narrow-band applications due to its high gain and low noise. However, due to the input matching condition, the value of the inductor connecting the source terminal to ground, L_s, is normally quite small and sensitive to process variation. In addition, the requirement of small inductor sometimes becomes a nuisance for the LNA design because not all the inductor values are available in the Process Design Kit (PDK). In this chapter, we propose an LNA where the input matching is realized through the capacitive feedback scheme and π-match network. The capacitive feedback helps to eliminate the need of inductor L_s for the input matching. Moreover, higher gain and an additional degree of design freedom are achieved with the use of the π-match network. The concept of utilizing capacitive feedback for input matching was implemented in [102]. However, the LNA in [102] has a non-cascode structure. In order to have a high reverse isolation, multi-stage structure was used which resulted in very high power consumption. The proposed LNA4 is a single stage cascode LNA. The detailed analysis on input matching, gain and NF will be presented. LNA4

achieves very high gain of 21.7 dB while provides good input matching at 2.4 GHz and consumes only 0.6 mW.

6.1 Extended noise analysis of the inductive source-degeneration common-source LNA (L-CSLNA)

In this section, we will perform the noise and input matching analysis of the cascode L-CSLNA. The schematic of the L-CSLNA and its equivalent small signal circuit for input impedance analysis are shown in Figure 6.1 (a) and (b). For simplicity's sake, we assume an infinite drain-source resistance of the input transistor. C_Y includes all parasitic capacitances at node *Y* to ground . It is estimated as:

$$C_Y = C_{gs2} + C_{sb2} + C_{db1} \tag{6.1}$$

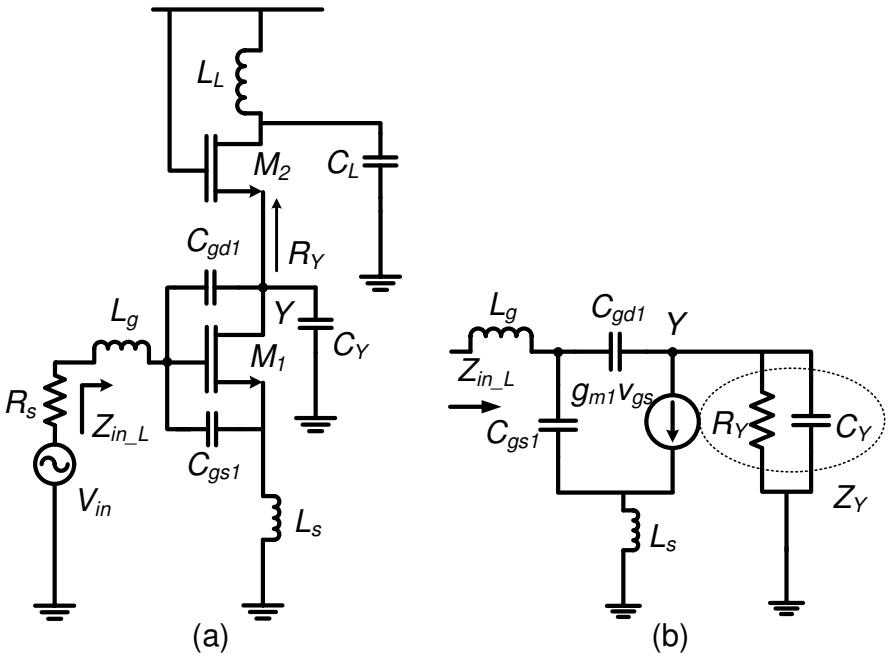

Figure 6.1: (a) Schematic and (b) Equivalent small signal circuit of the L-CSLNA

R_Y is the total impedance looking into the source of M_2 from node Y. In this circuit, R_Y can be approximated as to $1/g_{m2}$ where g_{m2} is the transconductance of transistor M_2. The L-CSLNA's input impedance is derived to be:

$$Z_{in\_L} = j\,\omega L_g + \frac{1 + (g_{m1} + j\,\omega C_{gs1}) j\,\omega L_s}{j\,\omega C_{gs1} + j\,\omega C_{gd1}\dfrac{1 + (g_{m1} + j\,\omega C_{gs1}) j\,\omega L_s + g_{m1} Z_Y}{1 + j\,\omega C_{gd1} Z_Y}} + r_{Lg} \tag{6.2}$$

where ω is the operating frequency, r_{Lg} is the parasitic resistance of inductor L_g, C_{gs1} and C_{gd1} are parasitic gate-source and gate-drain capacitance and g_{m1} is the transconductance of transistor M_1. When $C_{gd1} \to 0$, Z_{in_L} can be simplified to :

$$Z_{in} \approx j\left(\omega L_g + \omega L_s - \frac{1}{\omega C_{gs1}}\right) + \frac{g_{m1} L_s}{C_{gs1}} + r_{Lg} \tag{6.3}$$

which is consistent with the result given in textbooks. At resonance frequency, the input impedance, R_{in_L}, equals to $g_{m1} L_s / C_{gs1}$ and the transistor's transconductance, g_{m1}, is effectively boosted to $Q_{eff\_L} g_{m1}$ where Q_{eff_L} is:

$$Q_{eff\_L} = \frac{1}{\omega_0 C_{gs1}(g_{m1} L_s / C_{gs1} + r_{Lg})} = \frac{1}{\omega_0 C_{gs1} R_s} \tag{6.4}$$

and ω_0 is the resonance frequency. The noise factor of the L-CSLNA without cascode stage is derived as:

$$F_1 = 1 + \frac{r_{Lg}}{R_s} + \frac{\overline{i_{d1}^2}}{\overline{v_{in}^2}} \frac{1}{(g_{m1} Q_{eff\_L})^2} \tag{6.5}$$

where $\overline{i_{d1}^2}$ *is* the channel thermal noise of transistor M_1 and $\overline{v_{in}^2}$ is input source voltage noise. For simplicity, the noise factor of the cascode stage ignoring the effect of finite drain-source resistance is:

$$F_2 = 1 + \frac{\overline{i_{d2}^2}}{\overline{v_{in}^2}}\left(\frac{1}{g_{m2}}\right)^2 \tag{6.6}$$

where $\overline{i_{d2}^2}$ is the channel thermal noise of transistor M_2. The voltage gain from the input to the source of the cascode transistor is:

$$A_{v1} = g_{m1}Q_{eff\_L}(R_Y//C_Y) = g_{m1}Q_{eff\_L}\cdot\frac{1}{sC_Y + g_{m2}} \tag{6.7}$$

The cascode L-CSLNA can be treated as a two stage amplifier. Following the cascode network noise calculation theory, the noise factor of the L-CSLNA is derived as:

$$\begin{aligned} F_{CS\_L} &= F_1 + \frac{F_2 - 1}{A_{v1}} \\ &= 1 + \frac{r_{Lg}}{R_s} + \frac{1}{\left(g_{m1}Q_{eff\_L}\right)^2}\cdot\frac{\overline{i_{d1}^2}}{\overline{v_{in}^2}} + \frac{\sqrt{(g_{m2}^2 + \omega_0^2 C_Y^2)}}{g_{m1}Q_{eff\_L}g_{m2}^2}\cdot\frac{\overline{i_{d2}^2}}{\overline{v_{in}^2}} \end{aligned} \tag{6.8}$$

A large g_{m1} and small C_{gs1} are desired to achieve high gain and low noise. Due to the input matching condition, the value of L_s is normally quite small and is sensitive to process variations. In addition, the requirement of small L_s sometimes becomes a nuisance for the LNA design because not all the inductor values are available in the PDK.

6.2 Proposed capacitive feedback CSLNA with π-match network (LNA4)

The LNA introduced in [102] uses the parasitic gate-drain capacitance of the input device and the output capacitance, C_L to form the capacitive feedback matching network.

Only one inductor was used to realize the input matching. However, the analysis in [102] is only applicable to non-cascode structure. For CS topology, in order to have high reverse isolation and stability, a cascode structure is preferred. In this section, we will present the analysis for the cascode capacitive feedback LNA. Its schematic is shown in Figure 6.2(a).

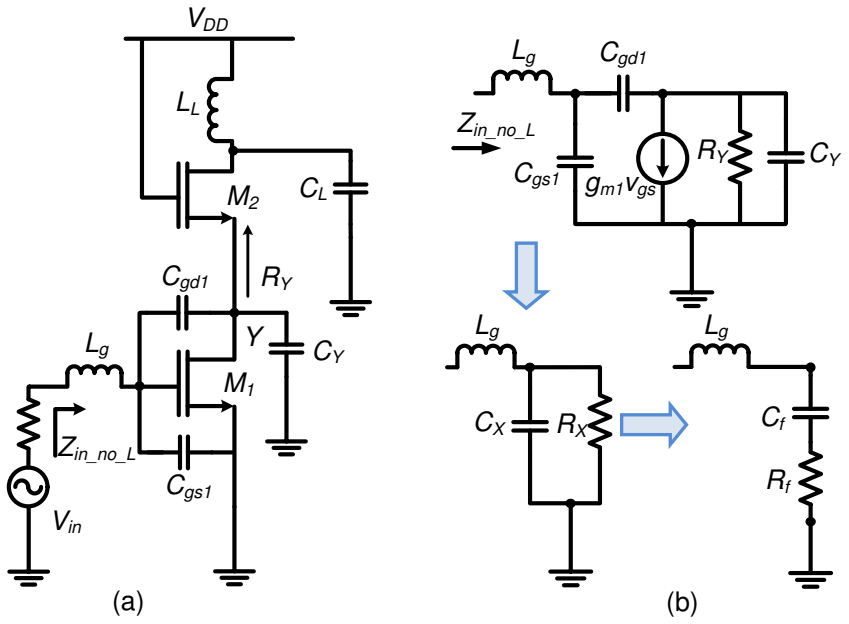

Figure 6.2: (a) Schematic and (b) Equivalent small signal circuit of the capacitive feedback LNA

Based on the small signal circuit in Figure 6.2(b), the input network of this LNA can be converted to a series RLC matching network including of L_g, C_f and R_f. The value of C_f and R_f can be derived as:

$$C_f = C_X[1 + (\omega C_X R_X)^2]/(\omega C_X R_X)^2 \tag{6.9}$$

and

$$R_f = R_X/[1 + (\omega C_X R_X)^2] \tag{6.10}$$

Here, C_X and R_X can be calculated as follow:

$$C_X = C_{gs1} + C_{gd1}\frac{\left[(g_{m2} + g_{m1})g_{m2} + \omega^2 C_Y\left(C_{gd1} + C_Y\right)\right]}{g_{m2}^2 + \omega^2\left(C_{gd1} + C_Y\right)^2} \tag{6.11}$$

$$R_X = \frac{g_{m2}^2 + \omega^2\left(C_{gd1} + C_Y\right)^2}{\omega^2 C_{gd1}\left[g_{m2}C_{gd1} + g_{m1}\left(C_{gd1} + C_Y\right)\right]} \tag{6.12}$$

The derivation of C_X and R_X can be found in Appendix B. To achieve the input matching, R_f is designed to be equal to R_s. The quality factor is defined as the ratio of the voltage across the gate-source terminal and the voltage at the input of the input matching network. The quality factor of this input matching network is:

$$\begin{aligned} Q_{eff\_no\_L} &= \frac{1/(sC_f) + R_f}{1/(sC_f) + sL_g + R_f} = 1 + \frac{1}{sC_f R_f} = \sqrt{1 + \frac{1}{\left(\omega_0 C_f R_f\right)^2}} \\ &= \sqrt{1 + \frac{1}{\left(\omega_0 C_f R_s\right)^2}} \end{aligned} \tag{6.13}$$

The total noise factor of the capacitive feedback LNA including the cascode stage is:

$$F_{CS\_no\_L} = 1 + \frac{r_{Lg}}{R_s} + \frac{4}{\left(g_{m1}Q_{eff\_no\_L}\right)^2}\cdot\frac{\overline{i_{d1}^2}}{\overline{v_{in}^2}} + \frac{2\sqrt{(g_{m2}^2 + \omega_0^2 C_Y^2)}}{g_{m1}Q_{eff\_no\_L}g_{m2}^2}\cdot\frac{\overline{i_{d2}^2}}{\overline{v_{in}^2}} \tag{6.14}$$

The derivation can be found in Appendix C. When compared to the inductive source degeneration CSLNA, this capacitive feedback LNA requires less number of inductor for input matching. But this benefit comes with a tradeoff of higher NF which can be observed from equations (6.8) and (6.14).

As seen from equations (6.4) and (6.13), the input network's quality factors of the two LNAs discussed above are limited by the 50 Ω matching condition. To achieve a good input matching, R_f and $(g_{m1}L_s/C_{gs1})$ must be matched to 50 Ω. This will restrict the selection of Q_{eff_L} and $Q_{eff\_no\_L}$, therefore limit the gains of these two LNAs. There exists a trade-off between high again and good input matching in these two LNAs.

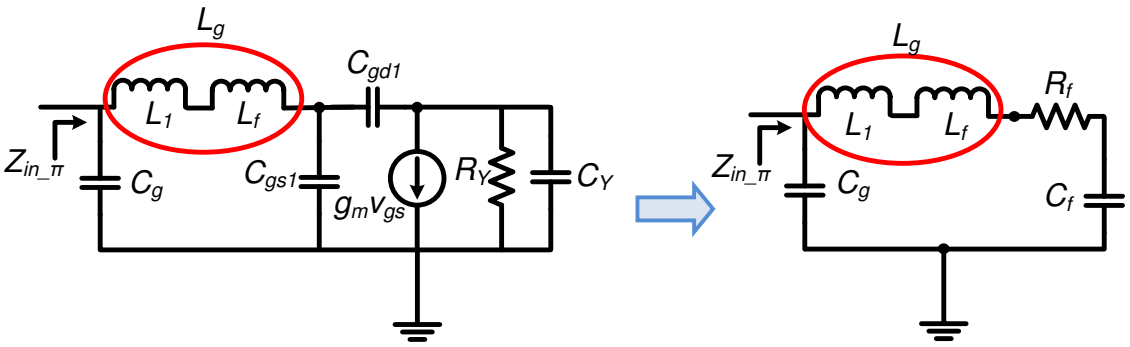

Figure 6.3: Equivalent small signal circuit of LNA4

The proposed LNA (LNA4) adds a parallel capacitor, C_g, preceding the gate inductor to create a π-match network. Figure 6.3 shows the small signal circuit for input impedance calculation of LNA4. R_f and C_f are formed by the capacitive feedback mechanism as described above. Inductor L_g can be divided into two smaller parts: L_1 and L_f. These two inductors will resonate with C_g and C_f respectively. The input impedance at resonance frequency is:

$$R_{in\_\pi} = \frac{1}{\omega_0^2 C_g^2 R_f} = \frac{\omega_0^2 L_1^2}{R_f} \tag{6.15}$$

The effective gain of the proposed input matching network is:

$$\begin{aligned} G_{eff\_\pi} &= \frac{1/(sC_f) + R_f}{1/(sC_f) + sL_g + R_f} = \frac{1/(sC_f) + R_f}{sL_1 + R_f} = \sqrt{\frac{1 + \left(\frac{1}{\omega_0 C_f R_f}\right)^2}{1 + \left(\frac{\omega_0 L_1}{R_f}\right)^2}} \\ &= \sqrt{\frac{1 + \left(\frac{1}{\omega_0 C_f R_f}\right)^2}{1 + \frac{R_S}{R_f}}} = \sqrt{\frac{R_f^2 + \left(\frac{1}{\omega_0 C_f}\right)^2}{R_f^2 + R_f R_S}} \end{aligned} \tag{6.16}$$

Equation (6.16) shows that the effective gain of LNA4 can be increased by adjusting the value of R_f and C_f. The input impedance then can be matched to 50 Ω by changing L_1 accordingly as explained in equation (6.15). Capacitor C_g and inductor L_1 adds an additional degree of freedom to the LNA design. The effective gain is no longer limited by the input matching condition. Therefore, LNA4 will be able to achieve much higher gain when compared to the L-CSLNA and the capacitive feedback LNA. Figure 6.4 shows the S_{21} and S_{11} responses of LNA3 and the L-CSLNA at the same power consumption level and output load condition. The LNAs were designed to have the same input matching at the frequency of interest. LNA4 clearly has much higher gain. The gain of LNA4 is 3 dB higher than that of the L-CSLNA. The bandwidth (BW) decreases as the effective gain of matching network increased. However, as shown in Figure 6.4, the BW of our LNA in this simulation is still sufficiently large for the required standard.

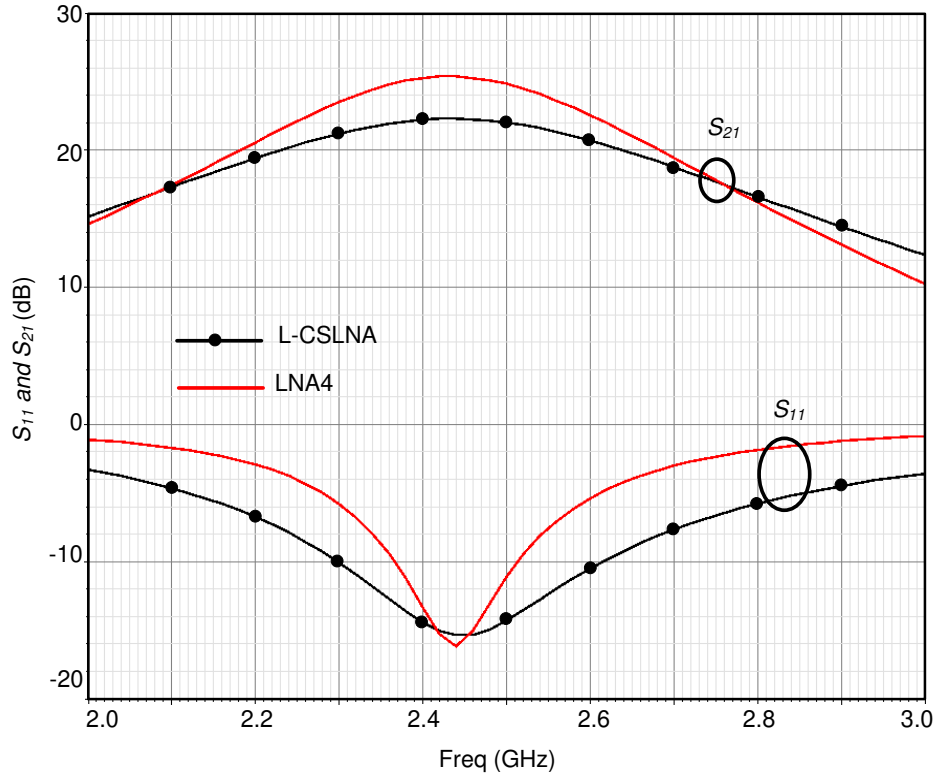

Figure 6.4: S_{21} and S_{11} responses of LNA4 and the L-CSLNA (simulation)

The noise factor of the proposed LNA is:

$$F_{CS\_\pi} = 1 + \frac{4\left[1+\left(\omega_0 L_1/R_f\right)^2\right]^2}{1+4\left(\omega_0 L_1/R_f\right)^2}\cdot\frac{r_{Lg}}{R_s} + \frac{4}{\left(g_{m1}G_{eff\_\pi}\right)^2}\cdot\frac{\overline{\iota_{d1}^2}}{\overline{v_{in}^2}} + \frac{2\sqrt{\left(g_{m2}^2+\omega_0^2 C_Y^2\right)}}{g_{m1}G_{eff\_\pi}g_{m2}^2}\cdot\frac{\overline{\iota_{d2}^2}}{\overline{v_{in}^2}} \tag{6.17}$$

Its derivation can be found in Appendix D. Compared to equation (6.14), the noise contribution of r_{Lg} has been increased due to the π-network. However, when the LNA is designed such that Q_{eff_π} is higher than $Q_{eff\_no\_L}$, the noise contribution from $\overline{\iota_{d1}^2}$ can be reduced. Therefore it can compensate for the loss caused by r_{Lg}. Moreover, the noise contribution of the cascode stage is also reduced when Q_{eff_π} is increased.

6.3 Circuit implementation

To demonstrate the idea, an LNA was designed and fabricated using the IBM 0.13 µm RF CMOS technology. For this fabrication, we shared the die area with another group which was using IBM 0.13 µm RF CMOS technology to save the fabrication cost. This resulted in the change of technology used.

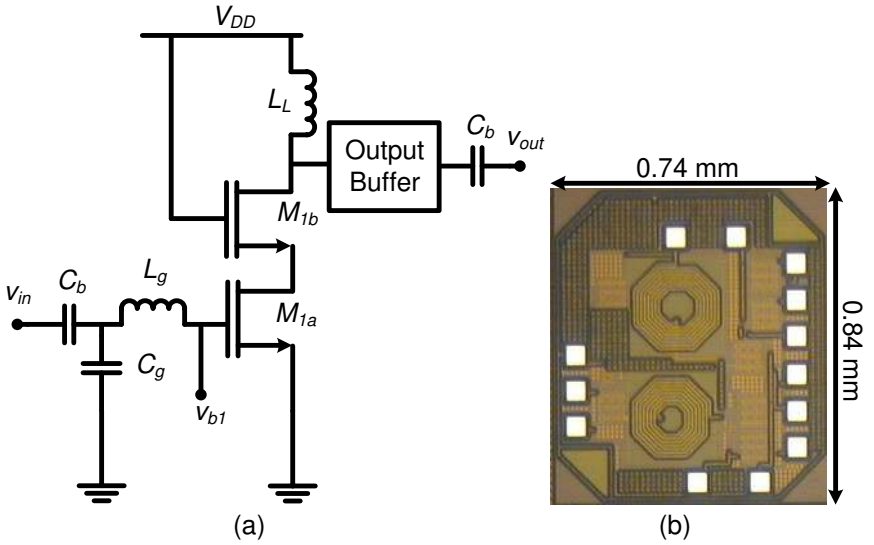

Figure 6.5: (a) Schematic and (b) Chip micrograph of LNA4

LNA4's schematic is shown in Figure 6.5(a). All inductors are on chip. Inductors L_L will resonate with the total capacitance at the drain node of transistor M_{1b} at the frequency of interest. Capacitors C_b are bypass capacitor. Inductors L_g and capacitor C_g are designed to satisfy the matching condition as analyzed in section 6.2. The second stage of this LNA is an output buffer. The design parameters are summarized in Table 6.1.

Table 6.1: Design parameters of LNA4

Parameter	$M_{1\,a}$, M_{1b}	L_g	L_L	C_g	C_b
Value	48 µm/0.18 µm	8 nH	9 nH	1.1 pF	10 pF

6.4 Measurement results and discussion

The LNA's chip micrograph is shown in Figure 6.5(b). The total area including the output buffer and pads is 0.74x0.84 mm^2. Figure 6.6 shows the voltage gain, S_{11} and S_{22} of the proposed LNA. The LNA's measured voltage gain at 2.4 GHz is 21.7 dB. A L-CSLNA at the same power consumption level and output load condition with LNA4 was also fabricated. LNA4's voltage gain at 2.4 GHz is 21.7 dB while the L-CSLNA's voltage gain is 18.8 dB. The measured gain of LNA4 is 2.9 dB higher than that of the L-CSLNA. The LNA has good input and output matching. The S_{11} value is better than -12 dB and the S_{22} value is better than -16 dB at 2.4 GHz. The NF at 2.4 GHz is 4.9 dB as shown in Figure 6.7. Due to process variation, the value of L_g and C_g are different from the desired one which results in a difference between measurement and simulation results.

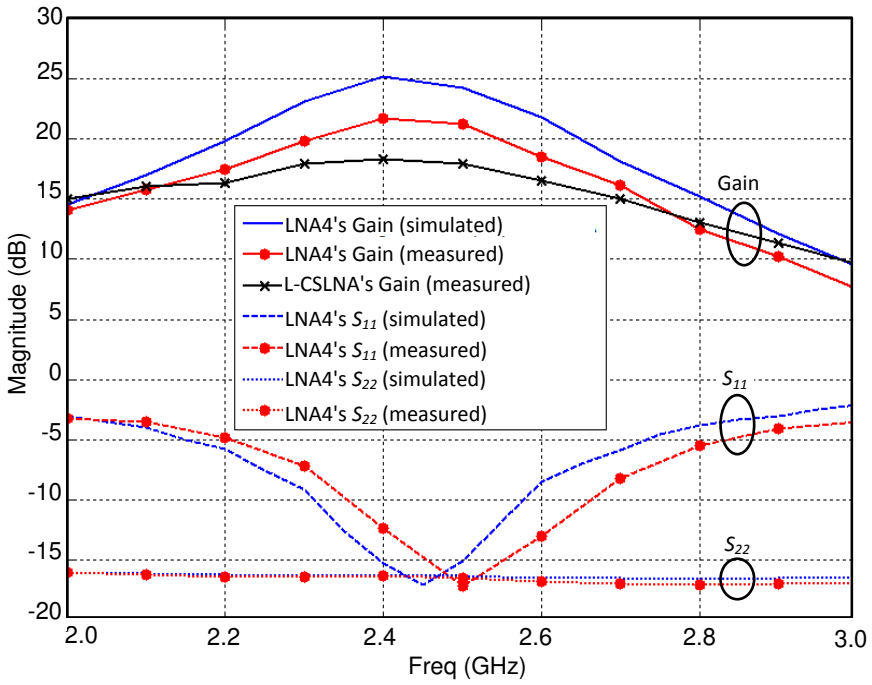

Figure 6.6: Voltage gain, S_{11} and S_{22} of LNA4

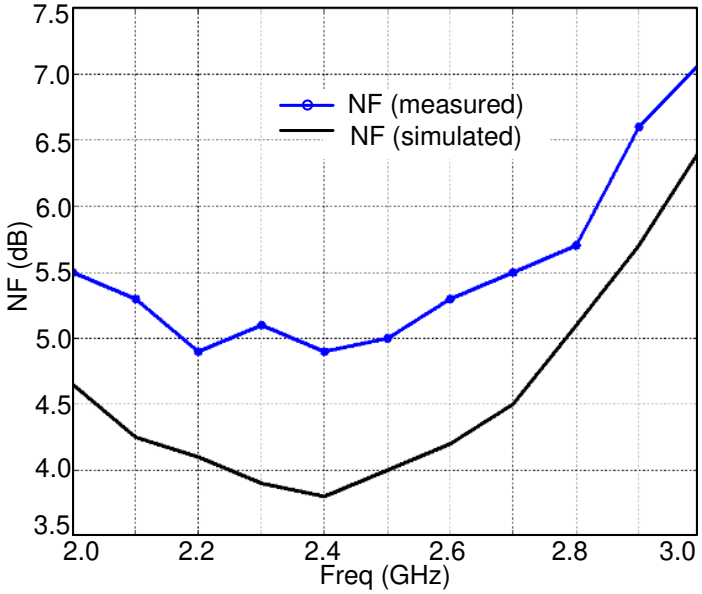

Figure 6.7: NF of LNA4

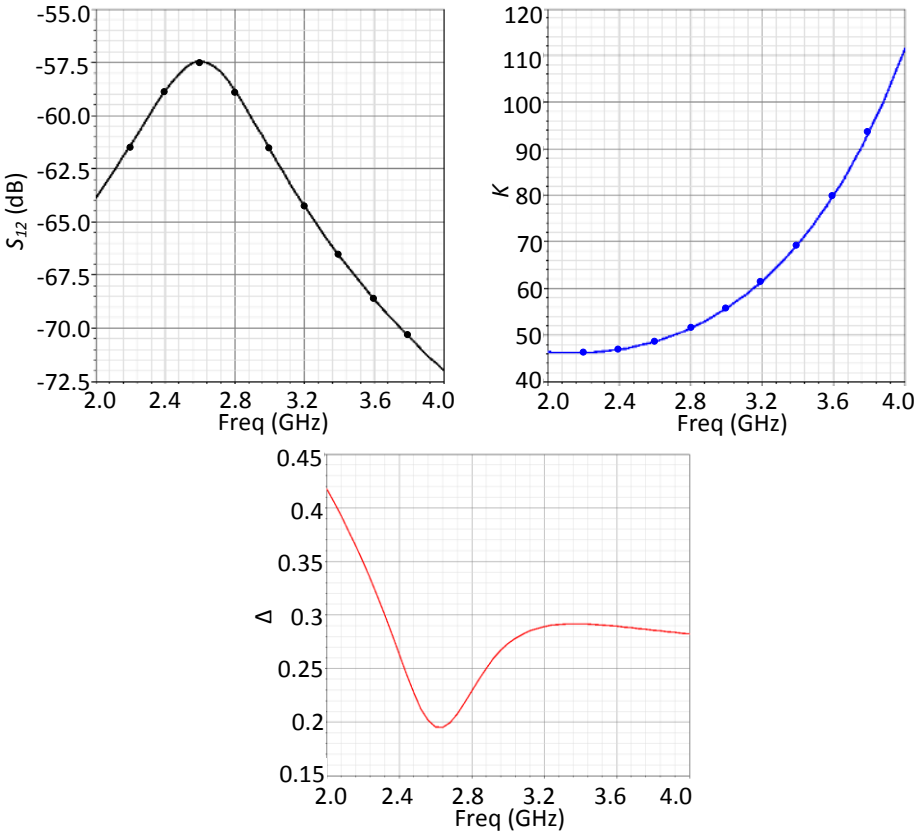

Figure 6.8: S_{12}, K and Δ of LNA4

LNA4 has high reverse isolation and is stable at the frequency of interest as seen on Figure 6.8. (S_{12} = -58 dB, K=48 and Δ=0.25 at 2.4 GHz). The *IIP3* is -12 dBm. The core of LNA4 draws 0.6 mA from a 1.0 V voltage supply. Total power consumption is only 0.6 mW. The overall performance is summarized in Table 6.2.

Table 6.2: LNA4's measurement results

LNA's Specification	Requirement	Measurement results
Gain	21 dB	21.7 dB
NF	<18.9 dB	4.9 dB
IIP3	>-20 dBm	-12 dBm
S_{11}	< -10 dB	-12 dB
S_{12}	< -30 dB	-58 dB

The comparison between LNA4 and recently published works is shown in Table 6.3. Among the LNAs, the work in [21], [103] and ours are able to achieve high gain. The LNA in [103] proposes a parallel LC input matching network for the CSLNA. It has a high gain of 25 dB but consumes very high power (15 mW). The transistors in this design are biased and sized for very high g_m in order to achieve high gain. The design in [21] as discussed before achieves high gain with the trade-off of high supply voltage (1.8 V). . The design in [102] also utilizes the capacitive feedback for input matching. However, it has a non-cascode structure. In order to have a high reverse isolation, multi-stage structure was used which resulted in very high power consumption (10 mW). Based on the FOMs calculated in Table 6.3, our LNA has the best *FOM1* and acceptable high *FOM2*.

Table 6.3: LNA4's performance comparisons

	[102]	[77]	[95]	[21]	[30]	[92]	[93]	[43]	[103]	LNA4
Tech (nm)	180	130	130	180	130	130	130	90	180	130
Freq (GHz)	12.8	3.0	5.1	2.4						
Pdc (mW)	10	0.4	1.03	1.13	6.5	17	3.2	3	15	0.6
Gain (dB)	13.2	9.1	10.3	21.4	13	10	16.5	15	24-25	21.7
NF (dB)	4.57	4.7	5.3	5.2	3.6	3.7	2.66	3	2.6-2.8	4.9
S_{11} (dB)	-11	-17	-17.7	-19	-14	-25	-11.8	-30	-14	-12
***IIP3* (dBm)**	-1	-11	n/a	-11	n/a	-6.7	-4.93	-7	n/a	-12
V_{DD} (V)	1	0.6	0.4	1.8	1.2	1.2	1.2	0.6	1.5	1
FOM1	4.97	10.4	8.32	10.33	1.07	-4.7	7.73	6.55	4.97	13.52
FOM2	3.97	-0.6	n/a	-0.67	n/a	-11.49	2.8	-0.4	n/a	1.52

6.5 Conclusion

A new input matching topology for CSLNA was presented in this chapter. The input network is realized using the capacitive feedback and the π-network. Based on this method, the novel CSLNA is able to achieve higher gain while maintaining good input matching and low power consumption. The design method was explained and the LNA was designed and fabricated. The need of source inductor L_s is eliminated; higher gain and an additional degree of design freedom are achieved when compared to the L-

CSLNA. The proposed LNA consumes only 0.6 mW while providing very high gain, good input matching and moderate NF.

Chapter 7: Conclusion and future works

7.1 Conclusion

In this thesis, the design issues of single-band CMOS LNA designs, especially for the IEEE 802.15.4 standard, are investigated extensively in order to find an approach that can help to achieve a low-power, compact, reliable and fully-integrated LNA design.

Design issues including performance trade-offs, input matching architectures, tuning techniques and different topologies in LNA designs are presented in detail. The LNA requirements in the IEEE 802.15.4 standard are next derived. This led us to propose several design techniques which take advantage of the relaxed performance requirements of the IEEE 802.15.4 standard.

Table 7.1: Performance summary of the four proposed LNAs

	Tech (µm)	**Freq (GHz)**	**Gain (dB)**	**NF (dB)**	S_{11} **(dB)**	***IIP3* (dBm)**	V_{DD} **(V)**	**Pdc (mW)**	***FOM1* *(dB)***	***FOM2* *(dB)***
LNA1	0.18	2.4	15	5.0	-11	-19	1	0.98	8.04	-10.96
LNA2	0.18		14.8	4.5	-20	-5.7	1	0.95	8.83	3.13
LNA3	0.18		14	3.55	-22	-6.8	0.6	0.5	12.88	6.08
LNA4	0.13		21.7	4.9	-12	-12	1	0.6	13.52	1.52
[21]	0.18		21.4	5.2	-19	-11	1.8	1.13	10.33	-0.67
[77]	0.13	3	9.1	4.7	-17	-11	0.6	0.4	10.4	-0.6

Performance analyses together with measurement results of the four LNAs are presented. In Table 7.1, we compare our work with references [21] and [77] which achieve one of the best FOM in the current literature. Both [21] and [77] employ the cascode CS structure and bias the transistors in sub-threshold region for high power efficiency. [21] has a high gain of 21.4 dB by using large resistive load. However, its total power consumption is limited by the high supply voltage of 1.8 V. [77] on the other hand uses inductive load in order to operate at low supply voltage of 0.6 V. However, its cascode structure has limited its linearity performance due to the low voltage headroom.

The first three LNA were optimized for low power consumption and low NF. LNA1 was designed by combining the merits of L-CSLNA and the CGLNA. LNA1 posses a great trade-off between NF and power consumption. Its noise performance satisfies the requirement of the IEEE 802.15.4 standard and it only consumes 0.98 mW. LNA2 and LNA3 were designed to achieve better FOMs and lower NF. In LNA2, a noise reduction technique using shunt inductor is proposed. LNA3 operates at 0.6 V supply voltage to reduce the total power consumption. It is a differential single-stage non-cascode LNA which explains a better IIP3 when compared to that of [77]. The poor reverse isolation problem in the single-stage non-cascode structure is improved by employing the capacitive cross-coupling (CCC) across the two sides of a differential input stage. Out of the three LNAs, LNA3 has the lowest NF, consumes the least power and achieve the best FOMs. The forth LNA was optimized for high gain. A new input matching based on capacitive feedback and π-network was proposed. By employing this new input matching network, LNA4 is able to achieve the desired goal. Its FOMs is better than that of [21] due to the lower supply voltage.

7.2 Future works

Due to the high potential of this work, here we propose several future works to be done. Firstly, while we have covered and explored deeply on the topic of LNA, other important blocks such as mixer, post-mixer baseband amplifier, channel-select filter, analog to-digital converter, and frequency synthesizer should be designed. The study on system level design for the IEEE 802.15.4 standard therefore should be deeply investigated. We believe that significantly power consumption can be saved by further exploring the performance trade-offs in the IEEE 802.15.4 standard. To achieve an ultra-low power system, novelty in both system and circuit design are required.

Secondly, while bringing in benefit such as higher level of integration and higher f_T, technology scaling also creates many issues for RFIC designer. Aggressive CMOS technology scaling results in supply voltage reductions to well below 1V. At low supply voltage, it is very challenging for critical blocks such as mixer and baseband circuits to achieve sufficient linearity. Moreover, RF/analog circuits are sensitive to leakage and process variations at deeply scaled CMOS technologies. This requires a more accurate device modeling.

Thirdly, the unlicensed band around 60 GHz presents interesting prospects for high-data-rate applications such as high-definition video streaming. Furthermore, the short wavelength makes it possible to integrate one or more antennas along with the transceiver, thus obviating the need for expensive, millimetre-wave packaging and high-frequency electrostatic discharge (ESD) protection devices. The heightened interest in this band for consumer applications has motivated research on the design of 60 GHz

building blocks in CMOS technology. This is very challenging due to the lossy substrate, low f_t and f_{max} of current CMOS technologies. Moreover, the low Q characteristic of an on-chip inductor has limited its usefulness in millimeter wave designs. New design methods incorporating microwave techniques and complex passive structures are needed to improve circuit performance. Example of such works are: transmission lines and distributed elements are being investigated and applied to the design of typical transceiver building blocks such as the LNA, VCO/PLL, mixer, and PA [104, 105].

Author's Publications

1. T.T.N. Tran, C.C. Boon, M.A. Do and K.S. Yeo, " Ultra-low power sub-mA series input resonance differential common gate LNA", IET electronic Letters, vol. 47, no. 12, pp.703-704, June 2011. (Impact factor = 1.01)

2. T. T. N. Tran, C. C. Boon, M. A. Do and K. S. Yeo, "A 0.6V high reverse-isolation through feedback self-cancellation for single-state non-cascode CMOS LNA" , Microwave and Optical Technology Letters, vol. 54, no. 02, pp. 374–379, Feb. 2012.

3. T. T. N. Tran, C. C. Boon, M. A. Do and K. S. Yeo, "An Input Matching Network without Gain Trade-off for Low-power CMOS LNA " has been accepted for publication in Microwave Journal, 2012.

4. T.T.N. Tran, C.C. Boon, M.A. Do and K.S. Yeo, "A noise reducing technique for common-gate LNA using shunt inductor" submitted to IEEE Microwave and Wireless Components Letters.

5. T.T.N. Tran, C.C. Boon, M.A. Do and K.S. Yeo, "Reciprocal Noise Canceling Low Power UWB LNA", IEEE International SoC Design Conference (IEEE ISOCC), pp.13-16, Busan, Korea, Nov.2009.

6. T.T.N. Tran, C.C. Boon, M.A. Do and K.S. Yeo, "A 2.4 GHz ultra low-power high gain LNA utilizing π-match and capacitive feedback input network", IEEE Midwest Symposium on Circuits and Systems (IEEE MWSCAS), Seoul, Korea, Aug. 7-10, 2011.

APPENDIX

APPENDIX A

DERIVATION OF NOISE FACTOR and GAIN OF CGLNA

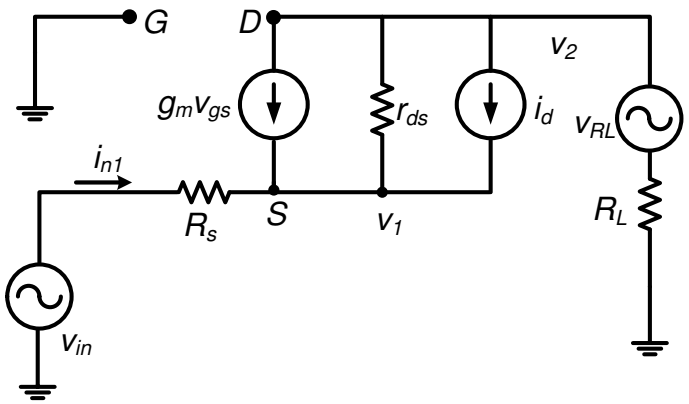

Figure A.1: Small signal circuit of the CGLNA for noise derivation

NF derivation

The three main noise sources that are considered in this noise analysis are: i_d , v_{in} and v_{RL} which are the transistor drain current noise , the input voltage noise due R_s and the voltage thermal noise due to R_L respectively. We will use superposition theorem to find the noise contribution from i_d , v_{in} and v_{RL} according to the small signal circuit in Figure A.1. Firstly, we will derive the output noise due to v_{in}.

$$v_1 = -v_{gs} \tag{A-1}$$

$$v_2 = i_{n1} R_L \tag{A-2}$$

$$v_1 = v_2 + i_{r0} r_{ds} \tag{A-3}$$

From (A-1) and (A-3):

$$-v_{gs} = i_{n1} R_L + \left(i_{n1} + g_m v_{gs}\right) r_{ds} \tag{A-4}$$

Or

$$v_{gs} = -\frac{(R_L + r_{ds})i_{n1}}{1 + g_m r_{ds}} \tag{A-5}$$

We have $v_{in} - v_1 = i_{n1}R_s$, hence

$$v_{in} + \left(-\frac{(R_L + r_{ds})i_{n1}}{1 + g_m r_{ds}}\right) = i_{n1}R_s \tag{A-6}$$

Rearrange

$$R_{in} = \frac{v_{in}}{i_{n1}} = R_s + \frac{R_L + r_{ds}}{1 + g_m r_{ds}} = R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}} \tag{A-7}$$

Output noise due to v_{in} is

$$\overline{\iota_{n1}^2} = \left(\frac{v_{in}}{R_{in}}\right)^2 = \frac{4kTR_s\Delta f}{\left(R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}\right)^2} \tag{A-8}$$

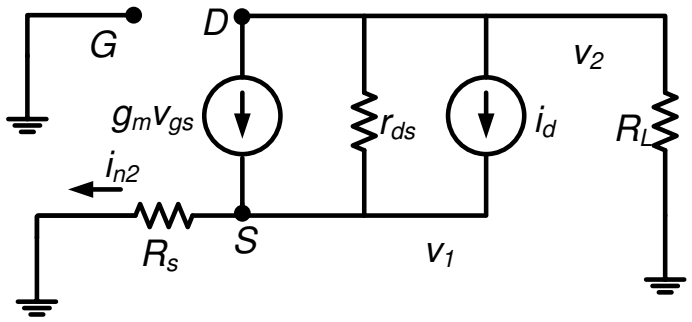

Figure A.2: Small signal circuit of the CGLNA for calculation of output noise due to i_d

Secondly, we will derive the output noise due to i_d according to the small signal circuit in Figure A.2.

$$v_2 = -v_1 \frac{R_L}{R_s} \tag{A-9}$$

Therefore

$$v_2 - v_1 = -v_1\left(1 + \frac{R_L}{R_s}\right) \tag{A-10}$$

$$v_1 = \left[g_m v_{gs} + i_d + (v_2 - v_1)/r_{ds}\right] R_s \tag{A-11}$$

Substitute $v_2 - v_1$ from (A-10) to (A-11):

$$v_1 = \left[-g_m v_1 + i_d - v_1\left(1 + \frac{R_L}{R_s}\right)\frac{1}{r_{ds}}\right] R_s \tag{A-12}$$

Rearrange (A-12) we have

$$v_1\left[\frac{1}{R_s} + g_m + \left(1 + \frac{R_L}{R_s}\right)\frac{1}{r_{ds}}\right] = i_d \tag{A-13}$$

Or

$$v_1 = \frac{i_d}{\frac{1}{R_s} + g_m + \left(1 + \frac{R_L}{R_s}\right)\frac{1}{r_{ds}}} \tag{A-14}$$

Output noise due to i_d is

$$\overline{i_{n2}^2} = \left(\frac{v_2}{R_L}\right)^2 = \left(\frac{v_1}{R_s}\right)^2 = \frac{i_d^2}{\left(1 + g_m R_s + (R_s + R_L)\frac{1}{r_{ds}}\right)^2} \tag{A-15}$$

$$= \frac{4kT\gamma g_{d0}\Delta f}{\left(1 + g_m R_s + (R_s + R_L)\frac{1}{r_{ds}}\right)^2}$$

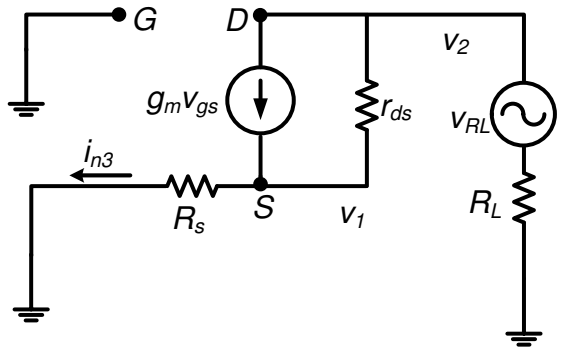

Figure A.3: Small signal circuit of the CGLNA for calculation of output noise due to v_{RL}

Thirdly, we will derive the output noise due to v_{RL} according to the small signal circuit in Figure A.3 .

$$v_2 = v_1 + v_{rds} = i_{n3}R_s + \left(i_{n3} - g_m v_{gs}\right)r_{ds} = i_{n3}R_s + (i_{n3} + g_m i_{in}R_s)r_{ds} \quad \text{(A-16)}$$

$$v_2 = v_{RL} - i_{n3}R_L \quad \text{(A-17)}$$

Therefore:

$$i_{n3}R_s + (i_{n3} + g_m i_{in}R_s)r_{ds} = v_{RL} - i_{n3}R_L \quad \text{(A-18)}$$

Hence

$$i_{n3}[R_s + R_L + (1 + g_m R_s)r_{ds}] = v_{RL} \quad \text{(A-19)}$$

Output noise due to v_{RL} is

$$\overline{i_{n3}^2} = \left(\frac{v_{RL}}{R_s + R_L + (1 + g_m R_s)r_{ds}}\right)^2 = \frac{4kTR_L\Delta f}{[R_s + R_L + (1 + g_m R_s)r_{ds}]^2} \quad \text{(A-20)}$$

From equations (A-8), (A-15) and (A-20), total noise factor is:

$$F = 1 + \frac{\overline{\iota_{n2}^2}}{\overline{\iota_{n1}^2}} + \frac{\overline{\iota_{n3}^2}}{\overline{\iota_{n1}^2}}$$

$$= 1 + \frac{4kT\gamma g_{d0}\Delta f}{4kTR_s\Delta f}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_L)\frac{1}{r_{ds}}}\right)^2$$

$$+ \frac{4kTR_L\Delta f}{4kTR_s\Delta f}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}}{R_s + R_L + (1 + g_m R_s)r_{ds}}\right)^2 \quad \text{(A-21)}$$

$$= 1 + \frac{\gamma}{\alpha}\frac{g_m}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_L)\frac{1}{r_{ds}}}\right)^2$$

$$+ \frac{R_L}{R_s}.\left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_L}{1 + g_m r_{ds}}}{R_s + R_L + (1 + g_m R_s)r_{ds}}\right)^2$$

Gain derivation

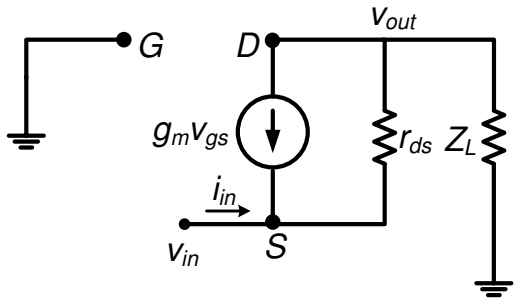

Figure A.4: Small signal circuit of the CGLNA for gain derivation

We will use the small signal circuit in Figure A.4 to derive the voltage gain of the CGLNA.

$$v_{in} = -v_{gs} \quad \text{(A-22)}$$

$$v_{out} = i_{in} Z_L \quad \text{(A-23)}$$

$$v_{out} = v_{in} - (i_{in} + g_m v_{GS}) r_{ds} \tag{A-24}$$

Therefore (A-25)

$$i_{in} Z_L = v_{in} - (i_{in} - g_m v_{in}) r_{ds}$$

Or

$$i_{in} = v_{in} \frac{1 + g_m r_{ds}}{Z_L + r_{ds}} \tag{A-26}$$

Hence

$$v_{out} = Z_L \frac{1 + g_m r_{ds}}{Z_L + r_{ds}} v_{in} = \frac{1/r_0 + g_m}{1/r_0 + 1/Z_L} v_{in} \tag{A-27}$$

$$A = \frac{\frac{1}{r_{ds}} + g_m}{\frac{1}{r_{ds}} + \frac{1}{Z_L}} \tag{A-28}$$

APPENDIX B

DERIVATION OF C_X AND R_X

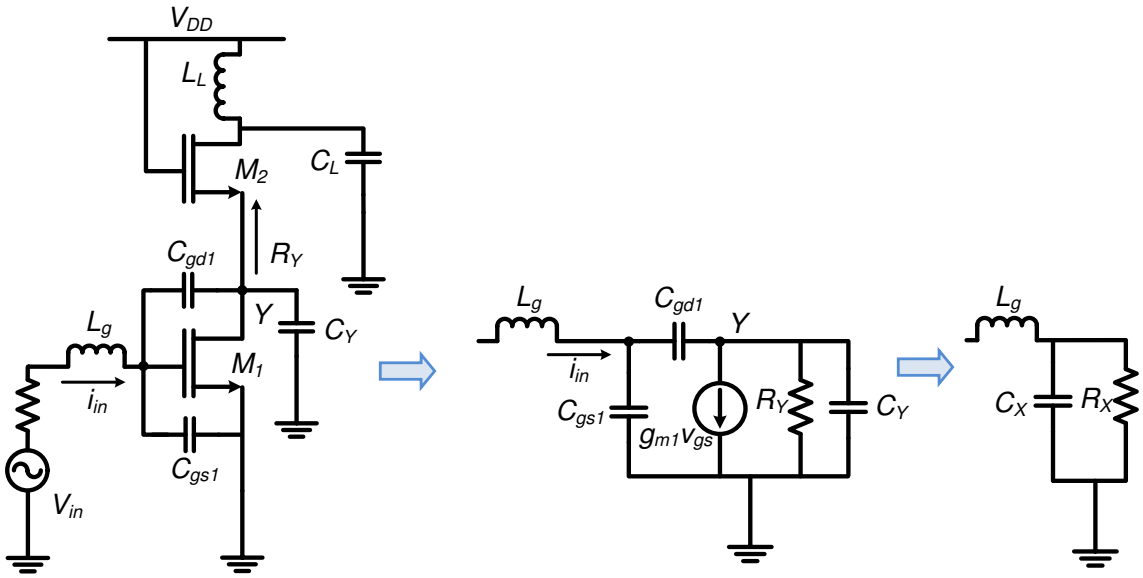

Figure B.1: Small signal circuit of the CSLNA with capacitive feedback

In Figure B.1, C_Y is the total capacitance at note Y to ground and R_Y is the total impedance looking into the source of M_2 from node Y. R_Y can be approximated as to $1/g_{m2}$ where g_{m2} is the transconductance of transistor M_2. By applying Thevenin theory at node D in Figure B,1, we have the following equation:

$$(v_g - v_d)sC_{gd1} = g_{m1}v_{gs} + v_d(g_{m2} + sC_Y) = g_{m1}v_g + v_d(g_{m2} + sC_Y) \qquad \text{(B-1)}$$

The input current, i_{in}, is derived to be:

$$i_{in} = v_g sC_{gs1} + (v_g - v_d)sC_{gd1} = v_g sC_{gs1} + \frac{g_{m2} + g_{m1} + sC_Y}{sC_{gd1} + sC_Y + g_{m2}} sC_{gd1}v_g \qquad \text{(B-2)}$$

From (B-1), we have:

$$v_d = \frac{sC_{gd1} - g_{m1}}{sC_{gd1} + sC_Y + g_{m2}} v_g \qquad \text{(B-3)}$$

Or

$$v_g - v_d = \frac{g_{m2} + g_{m1} + sC_Y}{sC_{gd1} + sC_Y + g_{m2}} v_{\mathrm{g}} \tag{B-4}$$

which, upon substitution into (B-2), yields:

$$i_{in} = j\omega C_{gs1} v_g + j\omega C_{gd1} \frac{\left[(g_{m2} + g_{m1})(g_{m2}) + \omega^2 C_Y \left(C_{gd1} + C_Y\right)\right]}{(g_{m2})^2 + \omega^2 \left(C_{gd1} + C_Y\right)^2} v_g \tag{B-5}$$

$$+ \frac{\omega^2 \left[g_{m2} C_2^2 + g_{m1}\left(C_{gd1} + C_Y\right) C_{gd1}\right]}{(g_{m2})^2 + \omega^2 \left(C_{gd1} + C_Y\right)^2} v_g$$

From (B-3), the formula for R_X and C_X can be derived as:

$$R_X = \frac{g_{m2}^2 + \omega^2 \left(C_{gd1} + C_Y\right)^2}{\omega^2 \left[g_{m2} C_2^2 + g_{m1}\left(C_{gd1} + C_Y\right) C_{gd1}\right]} \tag{B-6}$$

and

$$C_X = C_{gs1} + C_{gd1} \frac{\left[(g_{m2} + g_{m1}) g_{m2} + \omega^2 C_Y \left(C_{gd1} + C_Y\right)\right]}{g_{m2}^2 + \omega^2 \left(C_{gd1} + C_Y\right)^2} \tag{B-7}$$

APPENDIX C

NOISE FACTOR OF THE CASCODE CAPACITIVE FEEDBACK CSLNA

To find the noise factor of a cascode capacitive feedback CSLNA, we first derive the noise factor of its non-cascode structure. Figure C.1 shows the small signal circuit of the non-cascode capacitive feedback LNA. Z_Y is the equivalent load impedance. For simplicity, three main noise sources are considered for the noise factor derivation, namely input voltage thermal noise due to R_s, v_{in}, voltage thermal noise due to the parasitic resistance of L_g, v_{Lg} and transistor channel thermal noise, i_{d1}. To find the total noise factor, we employ the super position theory to find the noise contribution from each noise source.

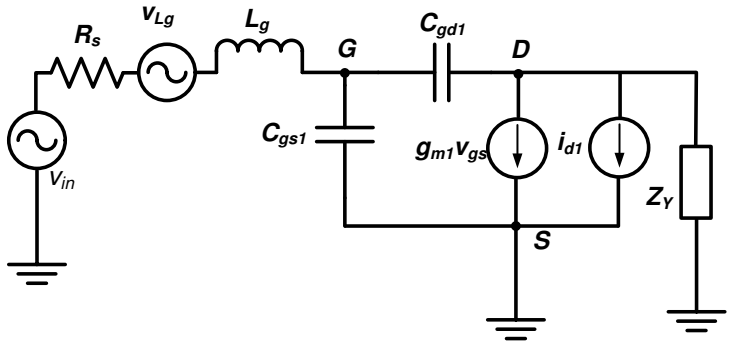

Figure C.1: Small signal circuit of the non-cascode capacitive feedback LNA

In a cascode LNA, Z_Y is equivalent $\left[(1/g_{m2})//C_y\right]$ where g_{m2} is the transconductance of the cascode transistor and C_y is the total capacitance at the input transistor's drain terminal to ground. Therefore, Z_Y is much smaller than the total impedance looking to the left side of node D in Figure C.1. Firstly, we find the current noise appeared at node D due to i_{d1}. When v_{in} and v_{Lg} are short-circuited, since Z_Y is

much smaller than the total impedance looking to the left side of node D, the current noise appeared at node D due to i_{d1} is:

$$\overline{i_{out,id1}^2} \approx \overline{i_{d1}^2} \tag{C-1}$$

Secondly, we find the current noise appeared at node D due to v_{in}. When v_{Lg} is short-circuited and i_{d1} is open-circuited, the current noise appeared at node D due to v_{in} is:

$$\overline{i_{out,vin}^2} = g_{m1}^2 \overline{v_{gs}^2} \tag{C-2}$$

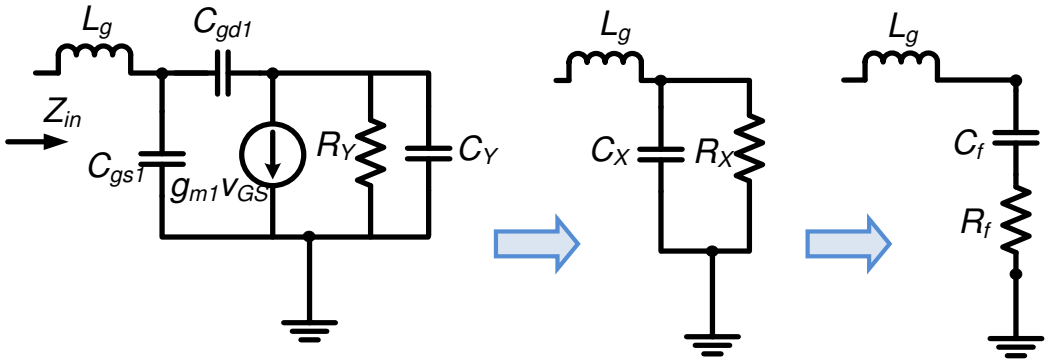

Figure C.2: Input impedance small signal model

In Figure C.2, R_f and C_f are the equivalent series resistance and capacitance of the parallel RC R_X and C_X. Based on Figure C.2, the gate source voltage, v_{GS}, due to v_{in} is:

$$v_{gs,in} = \frac{Z_{in}}{R_s + Z_{in}} \cdot \frac{R_f + \frac{1}{sC_f}}{R_f + sL_g + 1/(sC_{gs1})} v_{in} \tag{C-3}$$

where Z_{in} is the input impedance. With the input matching condition where $Z_{in} = R_s$ and at the resonance frequency equation (C-3) becomes:

$$v_{gs,in} = \frac{1}{2}\frac{R_f + \frac{1}{sC_f}}{R_f} v_{in} = \frac{1}{2}\left(1 + \frac{1}{sC_f R_f}\right) v_{in} \tag{C-4}$$

Substituting (C-4) into (C-2) yields:

$$\overline{\iota_{out,vin}^2} = \frac{1}{4} Q_{eff\_no\_L}^2 g_{m1}^2 v_{in}^2 \tag{C-5}$$

where $Q_{eff_{no_L}}$ at matching is defined as :

$$Q_{eff\_no\_L} = 1 + \frac{1}{sC_f R_f} = \sqrt{1 + \frac{1}{\left(\omega_0 C_f R_f\right)^2}} = \sqrt{1 + \frac{1}{\left(\omega_0 C_f R_s\right)^2}} \tag{C-6}$$

Similarly, the current noise appeared at node *D* due to v_{Lg} is:

$$\overline{\iota_{out,vLg}^2} = \frac{1}{4} Q_{eff\_no\_L}^2 g_{m1}^2 v_{Lg}^2 \tag{C-7}$$

The total noise factor of the non-cascode capacitive feedback LNA is:

$$F_{CS\_no\_L\_1} = 1 + \frac{\overline{\iota_{out,Lg}^2}}{\overline{\iota_{out,vin}^2}} + \frac{\overline{\iota_{out,id1}^2}}{\overline{\iota_{out,vin}^2}} = 1 + \frac{r_{Lg}}{R_s} + \frac{\overline{\iota_{d1}^2}}{\overline{v_{in}^2}} \frac{4}{\left(g_{m1} Q_{eff\_no\_L}\right)^2} \tag{C-8}$$

Now, we will find the noise factor of a cascode capacitive feedback CSLNA. The cascode stage (M_2) as shown in Figure C.3 can be consider as a CG-amplifier.

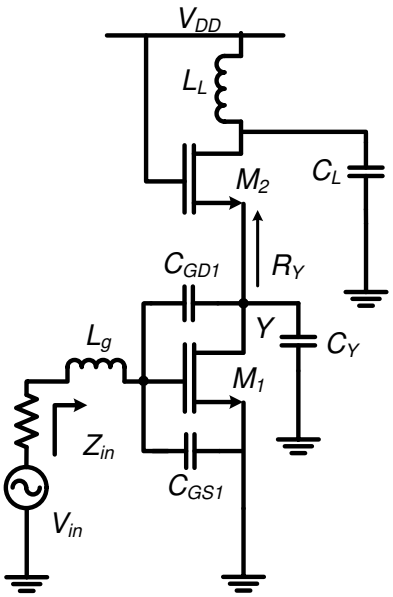

Figure C.3: Cascode capacitive feedback LNA

The total gain from input to the drain terminal of $M_1$is:

$$A_{v1} = \frac{1}{2} g_{m1} Q_{eff\_no\_L} (R_Y // C_y) = \frac{1}{2} g_{m1} Q_{eff\_no\_L} \left(\frac{1}{g_{m2} + sC_Y} \right) \tag{C-9}$$

For simplicity, the noise factor of the cascode stage ignoring the effect of finite drain-source resistance is:

$$F_2 = 1 + \frac{\overline{\iota_{d2}^2}}{\overline{v_{in}^2}} \left(\frac{1}{g_{m2}} \right)^2 \tag{C-10}$$

The total noise factor of the capacitive feedback LNA including the cascode stage is:

$$\begin{aligned} F_{CS\_no\_L} &= F_{CS\_no\_L\_1} + \frac{F_2 - 1}{A_{v1}} \\ &= 1 + \frac{r_{Lg}}{R_s} + \frac{\overline{\iota_{d1}^2}}{\overline{v_{in}^2}} \frac{4}{\left(g_{m1} Q_{eff\_no\_L} \right)^2} + \frac{\overline{\iota_{d2}^2}}{\overline{v_{in}^2}} \frac{2\sqrt{(g_{m2}^2 + \omega_0^2 C_Y^2)}}{g_{m1} Q_{eff\_no\_L} g_{m2}^2} \end{aligned} \tag{C-11}$$

APPENDIX D

NOISE FACTOR OF LNA4

The derivation steps will be similar to Appendix C. To find the total noise factor, we employ the super position theory to find the noise contribution from each noise source. Z_Y is the equivalent load impedance. For simplicity, three main noise sources are considered for the noise factor derivation, namely input voltage noise due to R_s, v_{in}, voltage thermal noise due to the parasitic resistance of L_g, v_{Lg} and transistor channel thermal noise, i_{d1}.

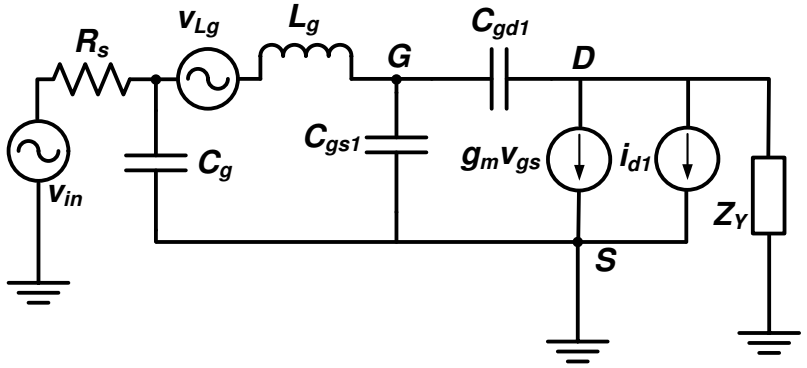

Figure D.1: Small signal model for noise analysis of LNA4

Firstly, we find the current noise appeared at node *D* due to i_{d1}. When v_{in} and v_{Lg} are short-circuited, the current noise appeared at node *D* due to $i_{d1}$is:

$$\overline{i^2_{out,id1}} \approx \overline{i^2_{d1}} \tag{D-1}$$

Secondly, we find the current noise appeared at node *D* due to v_{in}. When v_{Lg} is short-circuited and i_{d1} is open-circuited, the current noise appeared at node *D* due tov_{in} is:

$$\overline{\iota_{out,in}^2} = g_m^2 \overline{v_{gs,Rs}^2} = \frac{1}{4} Q_{eff\_\pi}^2 g_{m1}^2 v_{Rs}^2 \tag{D-2}$$

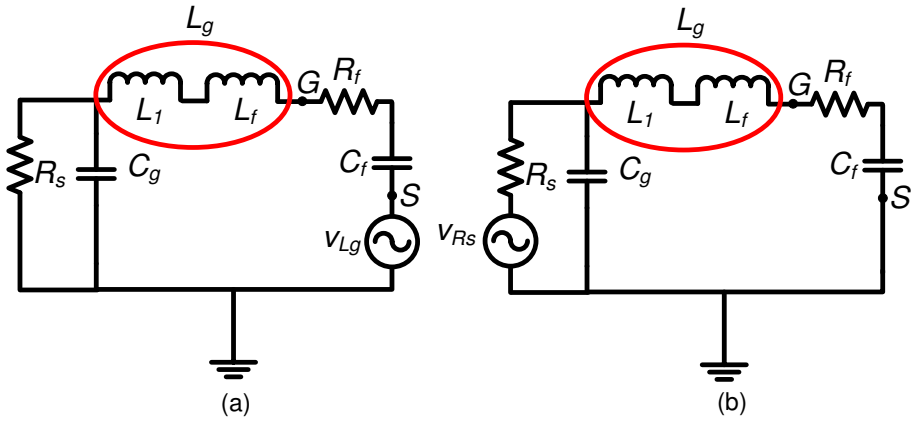

Figure D.2: Induced v_{gs} due to (a) v_{Lg} (b) v_{Rs}

Lastly, we find the current noise appeared at node *D* due to v_{Lg}. From Figure D.2(a), the induced v_{gs} due to v_{Lg} is:

$$v_{gs,Lg} = v_{Lg} \frac{R_f + \frac{1}{sC_f}}{R_f + \frac{1}{sC_f} + sL_g + \frac{1}{\frac{1}{R_s} + sC_g}} = v_{Lg} \frac{R_f + \frac{1}{sC_f}}{R_f + sL_1 + \frac{1}{\frac{1}{R_s} + sC_g}} \tag{D-3}$$

From Figure D.2 (b), the induced v_{gs} due to v_{in} at matching is:

$$v_{gs,vin} = \frac{1}{2} v_{in} \frac{R_f + \frac{1}{sC_f}}{R_f + \frac{1}{sC_f} + sL_g} = \frac{1}{2} v_{in} \frac{R_f + \frac{1}{sC_f}}{R_f + sL_1} \tag{D-4}$$

Dividing (D-3) by (D-4) we have:

$$\frac{v_{out,Lg}}{v_{out,in}} = \frac{v_{gs,Lg}}{v_{gs,vin}} = 2 \frac{v_{Lg}}{v_{in}} . \frac{R_f + sL_1}{R_f + sL_1 + \frac{1}{\frac{1}{R_s} + sC_g}} \tag{D-5}$$

The following three equations will be used to simplify equation (D-5)

$$Q_L = \frac{\omega_0 L_1}{R_f} \rightarrow \omega_0 L_1 = Q_L R_f \tag{D-6a}$$

$$Q_L = \frac{1}{\omega_0 C_g R_f} \rightarrow \omega_0 C_g = \frac{1}{Q_L R_f} \tag{D-6b}$$

$$R_{in\_\pi} = \frac{1}{\omega_0^2 C_g^2 R_f} = \frac{\omega_0^2 L_1^2}{R_f} = Q_L^2 R_f = R_S, \text{therefore } \frac{R_f}{R_S} = \frac{1}{Q_L^2} \tag{D-6c}$$

Substitute D-6(a-c) to (D-5) we have:

$$\frac{v_{n,out,Lg}}{v_{n,out,Rs}} = \frac{v_{Lg}}{v_{in}} . 2. \frac{R_f + sL_1}{R_f + sL_1 + \frac{1}{\frac{1}{R_s} + sC_g}} = \frac{v_{Lg}}{v_{in}} . 2. \frac{R_f + jQ_L R_f}{R_f + jQ_L R_f + \frac{1}{\frac{1}{R_s} + \frac{j}{Q_L R_f}}}$$

$$= \frac{v_{Lg}}{v_{in}} . 2. \frac{1 + jQ_L}{1 + jQ_L + \frac{1}{\frac{R_f}{R_s} + \frac{j}{Q_L}}} = \frac{v_{Lg}}{v_{in}} . 2. \frac{1 + jQ_L}{1 + jQ_L + \frac{1}{\frac{1}{Q_L^2} + \frac{j}{Q_L}}} \tag{D-7}$$

$$= \frac{v_{Lg}}{v_{in}} . 2. \frac{1 + jQ_L}{1 + jQ_L + \frac{Q_L^2}{1 + jQ_L}} = \frac{v_{Lg}}{v_{in}} . \frac{2(1 + jQ_L)^2}{(1 + jQ_L)^2 + Q_L^2}$$

$$= \frac{v_{Lg}}{v_{in}} \frac{2(1 + jQ_L)^2}{1 + j2Q_L}$$

Therefore:

$$\frac{\overline{v_{n,out,Lg}{}^2}}{\overline{v_{n,out,in}{}^2}} = \frac{4(1 + Q_L^2)^2}{1 + 4Q_L^2} \frac{r_{Lg}}{R_S} = \frac{4\left[1 + \left(\omega_0 L_1 / R_f\right)^2\right]^2}{1 + 4\left(\omega_0 L_1 / R_f\right)^2} \frac{r_{Lg}}{R_S} \tag{D-8}$$

Similarly to equation (C-9) in Appendix C, the total noise factor of the capacitive feedback LNA including the cascode stage is:

$$F_{CS\_\pi} = 1 + \frac{\overline{v_{n,out,Lg}{}^2}}{\overline{v_{n,out,in}{}^2}} + \frac{\overline{i_{out,id1}^2}}{\overline{i_{out,in}^2}} + \frac{F_2 - 1}{A_{v1}}$$

$$= 1 + \frac{4\left[1 + \left(\omega_0 L_1 / R_f\right)^2\right]^2}{1 + 4\left(\omega_0 L_1 / R_f\right)^2} \frac{r_{Lg}}{R_S} + \frac{\overline{i_{d1}^2}}{\overline{v_{in}^2}} \frac{4}{\left(g_{m1} Q_{eff\_\pi}\right)^2} \qquad \text{(D-9)}$$

$$+ \frac{\overline{i_{d2}^2}}{\overline{v_{in}^2}} \frac{2\sqrt{\left(g_{m2}^2 + \omega_0^2 C_Y^2\right)}}{g_{m1} Q_{eff\_no\_L} g_{m2}^2}$$

REFERENCES

1. M. Shouxian, " Dual Band Low-Noise Amplifier Designs For Bluetooth And HiperLAN Applications", Ph.D dissertation in Electrical & Electronic Engineering, Nanyang Technological University, 2006.
2. S. Joo, T. Choi, and B. Jung," A 2.4 GHz Resistive Feedback LNA in 0.13um CMOS", *IEEE J. Solid-State Circuits*, vol. 44, no. 3019-3029, Nov. 2009.
3. C. C. Boon, *RF IC Design Course Notes*, Nanyang Technological University, 2008.
4. J. A. M. Jarvinen, J. Kaukovuori, J. Ryynanen, J. Jussila, K. Kivekas, M. Honkanen, and K. A. I. Halonen," 2.4 GHz receiver for sensor applications", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 07, p. 1426 - 1433, Jul. 2005.
5. B. L. Wei, Y. J. Dai, X. X. Zhang, and Y. J. Lu, " A 2.4 GHz low-IF front-end receiver in 0.18-µm CMOS for IEEE 802.15.4 WPAN applications", *IEEE 8th International Conference on ASIC*, Changsha, Hunan, p. 1137 - 1140, Oct. 2009.
6. E. P. Hong, Y. S. Hwang, and H. J. Yoo, " A Low Power Folded RF Front-end with Low Flicker Noise for Direct Conversion Receiver", *IEEE Conference on Electron Devices and Solid-State Circuits*, p. 453-456, 2007.
7. E. P. Hong, Y. S. Hwang, and H. J. Yoo, " A Low Flicker Noise RF Front-end with Resonating Inductor for 2.4 GHz ISM Band", *IEEE International Workshop onRadio-Frequency Integration Technology*, p. 222-226, 2007.
8. E. P. Hong, Y. S. Hwang, and H. J. Yoo," Direct conversion RF front-end with a low-power consumption technique for 2.4 GHz ISM band", *IET Microwaves, Antennas & Propagation*, vol. 2, no. 8, p. 898-903, 2008.

9. A. Morici, S. Rodriguez, A. Rusu, M. Ismail, and C. Turchetti, " A 3.6mW 90 nm CMOS 2.4 GHz receiver front-end design for IEEE 802.15.4 WSNs", *International Symposium on Signals, Circuits and Systems*, p. 1-4, 2009.

10. I. Nam, C. Kyudon, L. Joonhee, C. Hyouk-Kyu, S. Bo-Ik, K. Kwon, and L. Kwyro," A 2.4-GHz Low-Power Low-IF Receiver and Direct-Conversion Transmitter in 0.18um CMOS for IEEE 802.15.4 WPAN Applications", *IEEE Transactions on Microwave Theory and Techniques,*, vol. 55, no. 4, p. 682-689, 2007.

11. T. J. Jung, K. S. Cheung, and J. Lau, " A 2.4 GHz four port mixer for direct conversion used in telemetering", *IEEE International Symposium on Circuits and Systems*, p. 378-381, 2001.

12. T. K. Nguyen, V. Krizhanovskii, J. Lee, S. K. Han, S. G. Lee, N. S. Kim, and C. S. Pyo," A Low-Power RF Direct-Conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 Standard in 0.18-um CMOS Technology", *IEEE Transactions on Microwave Theory and Techniques,* , vol. 54, no. 12, p. 4062-4071, 2006.

13. J. G. Atallah, S. Rodriguez, L. R. Zheng, and M. Ismail, " A Direct Conversion WiMAX RF Receiver Front-End in CMOS Technology", *International Symposium on Signals, Circuits and Systems*, p. 1-4, 2007.

14. B. R. Carlton, J. S. Duster, S. S. Taylor, and J. H. C. Zhan, " A 2.2dB NF, 4.9-6.0GHz direct conversion multi-standard RF receiver front-end in 90nm CMOS", *IEEE Radio Frequency Integrated Circuits Symposium*, p. 617-620, 2008.

15. E. P. Hong, Y. S. Hwang, and H. J. Yoo, " A Low Power Folded RF Front-end with Low Flicker Noise for Direct Conversion Receiver", *IEEE Conference on Electron Devices and Solid-State Circuits*, p. 453-456, 2007.

16. M. Hafizi, F. Shen, F. Taoling, K. Schulze, R. Ruth, R. Schwab, P. Karlsen, D. Simmonds, and G. Qizheng," RF front-end of direct conversion receiver RFIC for cdma-2000"*, IEEE Journal of Solid-State Circuits,* , vol. 39, no. 10, p. 1622-1632, 2004.

17. M. Hotti, J. Kaukovuori, J. Ryynanen, J. Jussila, K. Kivekas, and K. Halonen, " Dual-mode direct-conversion RF receiver with IIP2 calibration", *IEEE Compound Semiconductor Integrated Circuit Symposium*, p. 183-186, 2004.

18. N. Won and T. H. Meng," Direct-conversion RF receiver design"*, IEEE Transactions on Communications*, vol. 49, no. 3, p. 518-529, 2001.

19. B. Razavi, " RF Microelectronics": Prentice Hall PTR, chap.2, 2006.

20. N.-J. Oh and S.-G. Lee," Building a 2.4-GHz radio transceiver using IEEE 802.15.4"*, IEEE Circuits Devices Mag.*, vol. 21, no. 43-51, Jan.-Feb. 2006.

21. A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk," A subthreshold low-noise amplifier optimized for ultra-low-power applications in the ISM band", *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 02, p. 286-292, 2008.

22. D. K. Shaeffer, " The Design and Implementation of Low-Power CMOS Radio Receivers", Stanford University, 1998.

23. B. Razavi, " RF Microelectronics", Prentice Hall PTR, chap. 2, p. 15-25, 2006.

24. J. Chang, " An Integrated 900 MHz Spread-Spectrum Wireless Receiver in 1-µm CMOS and a Suspended Inductor Technique", University of California, 1998.

25. L. Zhu, *RF Engineering Techniques Course Notes*, Nanyang Technological University, 2008.

26. T. H. Lee, " The Design of CMOS Radio-Frequency Integrated Circuits", ed. 1st, New York: Cambridge University Press, chap.6, p. 134-140, 1998.

27. T. H. Lee, " The Design of CMOS Radio-Frequency Integrated Circuits", ed. 1st, New York: Cambridge University Press, chap.11, p. 277-289, 1998.

28. B. Razavi, " RF Microelectronics", Prentice Hall PTR, chap. 5, p. 144-146, 2006.

29. B. Razavi, " RF Microelectronics", Prentice Hall PTR, chap. 5, p. 139-144, 2006.

30. M. E. Kaamouchi, M. S. Moussa, P. Delatte, G. Wybo, A. Bens, J. P. Raskin, and J. V. Vanhoenacker," A 2.4-GHz Fully Integrated ESD-Protected Low-Noise Amplifier in 130-nm PD SOI CMOS Technology", *IEEE Transaction on Microwave Theory and Techniques*, vol. 55, no. 12, p. 2822 - 2831, 2007.

31. X. Chunyu and E. Sanchez-Sinencio," A GSM LNA using mutual-coupled degeneration ", *IEEE Transaction on Microwave and Wireless Components Letters*, vol. 15, no. 02, p. 68 - 70, 2005.

32. W. C. Cheng, J. G. Ma, K. S. Yeo, and M. A. Do, " Design of a Fully Integrated Switchable Transistor CMOS LNA for 2.1 / 2.4 GHz Application", *European Microwave Integrated Circuits Conference*, p. 133 - 136, Sep. 2006.

33. R. Point, M. Mendes, and W. Foley, " A differential 2.4 GHz switched-gain CMOS LNA for 802.11b and Bluetooth", *IEEE Radio and Wireless Conference*, p. 221 - 224, 2002.

34. B. G. Perumana, J.-H. C. Zhan, S. S. Taylor, B. R. Carlton, and J. Laskar, " A 9.2 mW, 4-8 GHz Resistive Feedback CMOS LNA with 24.4 dB Gain, 2 dB Noise Figure, and 21.5 dBm Output IP3 ", *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, p. 34 - 37, 2008.

35. D. H. Shin, J. Park, and C. P. Yue, " A low-power, 3-5-GHz CMOS UWB LNA using transformer matching technique", *IEEE Asian Solid-State Circuits Conference*, p. 95 - 98, Nov. 2007.

36. S. Vishwakarma, J. S. Jung, and J. Youngjoong, " Ultra wideband CMOS low noise amplifier with active input matching", *Joint with Conference on Ultrawideband Systems and Technologies.* , p. 415 - 419, May 2004.

37. D. Linten, S. Thijs, M. I. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere," A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS"*, IEEE Journal of Solid-State Circuits*, vol. 40, no. 07, p. 1434 - 1442, Jul. 2005.

38. H. Samavati, H. R. Rategh, and T. H. Lee," A 5-GHz CMOS Wireless LAN Receiver Front End"*, IEEE Journal of Solid-State Circuits*, vol. 35, no. 05, p. 765 - 772, May 2000.

39. J. H. C. Zhan and S.S.Taylor, " A 5GHz resistive-feedback CMOS LNA for low-cost multi-standard applications", *IEEE International Solid-State Circuits Conference*, San Francisco, CA, p. 721 - 730, Feb. 2006.

40. C. S. Chen, W. S. Wuen, and K. A. Wen, " A 2.5GHz 90nm CMOS Triple Gain Mode LNA for WiMAX Applications", *International Symposium on Signals, Systems and Electronics*, Montreal, Que, p. 367 - 369, Jul. 30 2007-Aug. 2 2007.

41. P. Orsatti, F. Piazza, and Q. T. Huang," A 20-mA-receive, 55-mA-transmit, single-chip GSM transceiver in 0.25-mm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, p. 1869-1880, Dec. 1999.

42. J. C. Rudell," A 1.9 GHz wide-band IF double conversion CMOS receiver for cordless telephone applications", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, p. 2071-2087, Dec. 1997.

43. A. Balankutty, Y. Shih-An, F. Yiping, and P. R. Kinget," A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 03, p. 538 - 553, Mar. 2010.

44. D. K. Shaeffer and T. H. Lee.," A 1.5-V 1.5-GHz CMOS low noise amplifier", *IEEE J. Solid-State Circuits*, vol. 32, no. 05, p. 745-759, May 1997.

45. B. Park, K. Lee, S. Choi, and S. Hong, " A 3.1-10.6 GHz RF Receiver Front-end in 0.18 mu m CMOS for Ultra-Wideband Applications", *IEEE MTT-S International microwave symposium digest*, p. 1616-1619, 2010.

46. C. C. Wu, X. Sun, A. V. Sangiovanni, and J. Rabaey, " A 2.2mW CMOS LNA for 6-8.5GHz UWB Receivers", *IEEE International Symposium on circuit and systems*, p. 1631-1634, 2010.

47. D. Im, I. Nam, and K. Lee," A Low Power Broadband Differential Low Noise Amplifier Employing Noise and IM3 Distortion Cancellation for Mobile Broadcast Receivers", *IEEE Microwave and wireless components letters*, vol. 20, no. 10, p. 566-568, 2010.

48. J. Y. Li, W. J. Lin, M. P. Houng, and L. S. Chen," A low power consumption and wide-band input matching CMOS active balun for UWB system applications ", *Journal of electromagnetic waves and applications*, vol. 24, no. 11-12, p. 1449-1457, 2010.

49. G. H. Z. Fatin, Z.D. Koozehkanani, and H. Sjoland," A technique for improving gain and noise figure of common-gate wideband LNAs", *Analog integrated circuits and signal processing*, vol. 65, no. 02, p. 239-244, 2010.

50. M. Sato, T. Takahashi, and T. Hirose," 68-110-GHz-Band Low-Noise Amplifier Using Current Reuse Topology", *IEEE Transaction on Microwave Theory and Techniques*, vol. 58, no. 7, p. 1910-1916, 2010.

51. S. Du, C. Wang, X. Shi, and S. Guo," A 3.1-10.6GHz high linear Low Noise Amplifier for Ultra-wideband Receivers", *FREQUENZ*, vol. 65, no. 1-2, p. 10-13, 2010.

52. R. S. M. Hasan," Analysis and Design of a Multistage CMOS Band-Pass Low-Noise Preamplifier for Ultrawideband RF Receiver", *IEEE transaction on very large scale integration systems*, vol. 18, no. 4, p. 638-651 , 2010.

53. L. Cai, Z. Fu, and L. Huang, " Design of Common Gate UWB LNA in CMOS", *IEEE 8th international conference on ASIC*, Changsha, China, p. 1201-1204, 2009.

54. C. F. Liao and S. I. Liu," A Broadband Noise-Canceling CMOS LNA for 3.1–10.6-GHz UWB Receivers", *IEEE J. Solid-State Circuits*, vol. 42, no. 02, p. 329-339, Feb. 2007.

55. C. W. Hung, L. Gang, B. Zdravko, and A. M. Niknejad," A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation", *IEEE J. Solid-State Circuits*, vol. 43, no. 05, p. 1164 - 1176, May 2008.

56. S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta," Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 06, p. 1341-1350, Jun. 2008.

57. W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. d. Gyvez, D. J. Allstot, and E. Sanchez-Sinencio," A capacitor cross-coupled common-gate low-noise amplifier", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 12, p. 875- 879, Dec. 2005.

58. W. Zhuo, S. Embabi, J. P. d. Gyvez, and E. Sanchez-Sinencio, " Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design", *Proceedings of the 26th European Solid-State Circuits Conference*, p. 77- 80, 19-21, Sept. 2000.

59. Y. M. Ge and K. Mayaram, "A comparative analysis of CMOS low noise amplifiers for RF applications", in *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, p. 349-352, 1998

60. F. Bruccoleri, E. A. M. Klumperink, and B. Nauta," Wide-band CMOS low-noise amplifier exploiting thermal noise canceling", *IEEE J. Solid-State Circuits*, vol. 39, no. 02, p. 275 - 282, Feb. 2007.

61. M. Shouxian, " Dual Band Low-Noise Amplifier Designs For Bluetooth And HiperLAN Applications", Nanyang Technological University, 2006.

62. V. A. Do, C. C. Boon, M. A. Do, and K. S. Yeo," A subthreshold low-noise amplifier optimized for ultra-low-power applications in the ISM band", *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 02, p. 286-292, 2008.

63. G. Gramegna, M. Paparo, P. G. Erratico, and P. D. Vita," A sub-1-dB NF±2.3-kV ESD-protected 900-MHz CMOS LNA"*, A sub-1-dB NF±2.3-kV ESD-protected 900-MHz CMOS LNA*, vol. 36, no. 07, p. 1010 - 1017, Jul. 2001.

64. D. Ho and S. Mirabbasi, " Design Considerations for Sub-mW RF CMOS Low-Noise Amplifiers", *Canadian Conference on Electrical and Computer Engineering*, p. 376 - 380, 2007.

65. W. Da-Ke, H. Ru, and W. Yang-Yuan, " A Low-Voltage and Low-Power CMOS LNA Using Forward-Body-Bias NMOS at 5GHz", *International Conference on Solid-State and Integrated Circuit Technology*, p. 1658-1660, 2006.

66. Q. Hong and J. Zhang, " A 1.5V Low Power CMOS LNA Design", *International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications*, p. 1379-1382, 2007.

67. E. Kargaran, H. Kargaran, and H. Nabovati, " A 0.6v Ultra-High-Gain Ultra-Low-Power CMOS LNA at 1.5GHz in 0.18um Technology", *Second International Conference on Computer and Electrical Engineering*, p. 123-125, 2009.

68. W. Muh-Dey, C. Sheng-Fuh, and L. Yu-Chun, " A Low-Power Ultra-Compact CMOS LNA with Shunt-Resonating Current-Reused Topology", *European Microwave Integrated Circuit Conference*, p. 350-353, 2008.

69. J. Zhang and Q. Hong, " A 1GHz low power CMOS LNA", *International Conference on Microwave and Millimeter Wave Technology*, p. 1-3, 2007.

70. C. Chieh-Pin, C. Ja-Hao, and W. Yeong-Her," A Fully Integrated 5 GHz Low-Voltage LNA Using Forward Body Bias Technology", *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 3, p. 176-178, 2009.

71. J. H. Lee, C. C. Chen, and Y. S. Lin," 3.7 mW 24 GHz LNA with 10.1 dB gain and 4.5 dB NF in 0.18 um CMOS technology", *Electronics Letters*, vol. 46, no. 19, p. 1310-1312, 2010.

72. Y. S. Wang and L. H. Lu," 5.7 GHz low-power variable-gain LNA in 0.18 um CMOS", *Electronics Letters*, vol. 41, no. 2, p. 66-68, 2005.

73. A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk," A weak-inversion low-power active mixer for 2.4 GHz ISM band applications", *IEEE Microwave and wireless components letters*, vol. 19, no. 11, p. 719-721, Nov. 2009.

74. A. Meaamar, C. C. Boon, M. A. Do, and K. S. Yeo," A 3-8 GHz Low-noise CMOS amplifier", *IEEE Microwave and wireless components letters*, vol. 19, no. 04, p. 245-247, 2009.

75. A. Meaamar, C. C. Boon, K. S. Yeo, and M. A. Do," A Wideband Low Power Low-Noise Amplifier in CMOS Technology", *IEEE transactions on Circuits and Systems I: Regular papers*, vol. 57, no. 04, p. 773-782, 2010.

76. T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang, and S. G. Lee," CMOS low-noise amplifier design optimization techniques", *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 05, p. 1433, 2004.

77. H. Lee and S. Mohammadi, "A 3 GHz sub threshold CMOS low noise amplifier", in *Proc. Radio Freq. Integrated Circuits (RFIC) Symp.*, Jun. 2006.

78. K. L. Chan, M. A. Do, K. S. Yeo, and J. G. Ma," A 1.5V 1.8GHz bandpass amplifier"*, IEE Proceedings on Circuits, Devices and Systems*, vol. 147, no. 06, p. 331-333, Dec. 2000.

79. E. A. Allan, T. Manku, and E. I. El-Masry," Q-enhanced 1.9GHz tuned CMOS RF amplifier"*, Electronics Letters*, vol. 32, no. 05, p. 448-449, Feb. 1996.

80. C. Y. Wu and S. Y. Hsiao," The design of a 3-V 900MHz CMOS bandpass amplifier"*, IEEE Journal of Solid-State Circuits*, vol. 32, no. 02, p. 159–168, Feb. 1997.

81. W. Zhuo, J. G. Pineda, and E. Sanchez-Sinenci, " Programmable low noise amplifier with active-inductor load", *Proceedings of IEEE International Symposium on Circuits and Systems*, p. 365 –368, 1998.

82. R. Akbari-Dilmaghani and A. Payne, " An RF CMOS differential bandpass amplifier using an active inductor", *IEE Colloquium on Systems on a Chip*, p. 161 -166, 1998.

83. C. C. Hsiao, C. W. Kuo, C. C. Ho, and Y. J. Chan," Improved quality-factor of 0.18-µm CMOS active inductor by a feedback resistance design"*, IEEE Microwave and Wireless Components Letters*, vol. 12, no. 12, p. 467 - 469, Dec. 2002.

84. A. Thanachayanont and A. Payne," CMOS floating active inductor and its applications to bandpass filter and oscillator designs"*, IEE Proceedings on Circuits, Devices and Systems*, vol. 147, no. 01, p. 42-48, Feb. 2000.

85. Y. Wu, X. H. Ding, M. Ismail, and H. Olsson," RF bandpass filter design based on CMOS active inductors", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 12, p. 942-949, Dec. 2003.

86. W. Yang, " CMOS Broadband Low Noise Amplifiers for Software Radio", Master Thesis, Nanyang Technological University, 2001.

87. C. P. Chang, J. H. Chen, and Y. H. Wang," A Fully Integrated 5 GHz Low-Voltage LNA Using Forward Body Bias Technology", *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 3, p. 176-178, Mar. 2009.

88. B. W. Cook, " Low energy RF transceiver design", University of California at Berkeley, May 2007.

89. N. Trung-Kien, V. Krizhanovskii, L. Jeongseon, H. Seok-Kyun, L. Sang-Gug, K. Nae-Soo, and P. Cheol-Sig," A Low-Power RF Direct-Conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 Standard in 0.18-um CMOS Technology", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 12, p. 4062-4071, 2006.

90. W. Zhuo, S. Embabi, J. P. d. Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design", in *Proceedings of the 26th European Solid-State Circuits Conference*, p. 77- 80, Sep. 2000.

91. S. Joo, T. Choi, and B. Jung," A 2.4GHz Resistive Feedback LNA in 0.13um CMOS", *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3019-3029, Nov. 2009.

92. M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari," A CMOS Low-Noise Amplifier With Reconfigurable Input Matching Network ", *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, p. 1054 - 1062, May 2009.

93. A. Esteves, J. Dores, P. Matos, Martins, A. Miguel, and J. R. Fernandes, " An ISM 2.4 GHz low-IF receiver frontend ", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio de Janeiro, Brazil, p. 546 - 549, 05 Jul. 2011.

94. J. Li and S. M. R. Hasan," A 0.7 V 850 μW CMOS LNA for UHF RFID reader", *Microwave and Optical Technology Letters*, vol. 52, no. 12, p. 2780–2782, Dec. 2010.

95. D. Wu, R. Huang, W. Wong, and Y. Wang," A 0.4-V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application", *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 07, p. 543-545, Jul. 2007.

96. M. Iwai, A. Oishi, T. Sanuki, Y. Takegawa, T. Komoda, Y. Morimasa, K. Ishimaru, M. Takayanagi, K. Eguchi, D. Matsushita, K. Muraoka, K. Sunouchi, and T. Noguchi, " 45 nm CMOS platform technology (CMOS6) with high density embedded memories", *Symposium on VLSI Technology, Digest of Technical Papers*, p. 12-13, Jun. 2004.

97. M. Brandolini, M. Sosio, and F. Svelto," A 750 mV Fully Integrated Direct Conversion Receiver Front-End for GSM in 90-nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 06, p. 1310-1317, Jun.2007.

98. H. Chih-Lung and H. Yi-Lun, " A low supply voltage dualband low noise amplifier design", *IEEE 13th International Symposium on Consumer Electronics*, Kyoto, p. 339 - 341, 25-28 May 2009.

99. T. Kihara, P. Hae-Ju, I. Takobe, F. Yamashita, T. Matsuoka, and K.Taniguchi., " A 0.5 V Area-Efficient Transformer Folded-Cascode CMOS Low-Noise Amplifier", *IEEE International Conference on Integrated Circuit Design and Technology and Tutorial*, Auxtin,TX, p. 21 - 24, 2-4 Jun. 2008.

100. A. Balankutty, S.-A. Yu, Y. Feng, and P. R. Kinget," A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 03, p. 538-553, 2010.

101. M. Cimino, H. Lapuyade, Y. Deval, T. Taris, and J.-B. Begueret," Design of a 0.9 V 2.45 GHz Self-Testable and Reliability-Enhanced CMOS LNA", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 05, p. 1187-1194, May 2008.

102. Y. W. Chung and F. R. Shahroury, " A Low-Voltage CMOS LNA Design Utilizing the Technique of Capacitive Feedback Matching Network", *IEEE International Conference on Electronics Circuits and Systems,*, p. 78-81, Dec. 2006.

103. S. Mou, J. G. Ma, K. S. Yeo, and M. A. Do," A modified architecture used for input matching in CMOS low-noise amplifiers", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 11, p. 784- 788, Nov. 2005.

104. C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen," Millimeter-wave CMOS design", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 144-155, Jan. 2005.

105. S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, " A 60-GHz down-converting CMOS single-gate mixer", *IEEE RFIC Symp. Dig.*, p. 163-166, Jun. 2005.