Journal of
Low Power Electronics and Applications

MDPI

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Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications

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Abstract: This paper presents a capacitively coupled chopper instrumentation amplifier (CCIA) with ultra-low power consumption and programmable bandwidth for biomedical applications. To achieve a flexible bandwidth from 0.2 to 10 kHz without additional power consumption, a programmable Miller compensation technique was proposed and used in the CCIA. By using a Squeezed inverter amplifier (SQI) that employs a 0.2-V supply, the proposed CCIA addresses the primary noise source in the first stage, resulting in high noise power efficiency. The proposed CCIA is designed using a 0.18 µm CMOS technology process and has a chip area of 0.083 mm^2. With a power consumption of 0.47 µW at 0.2 and 0.8 V supply, the proposed amplifier architecture achieves a thermal noise of 28 nV/$\sqrt{}$Hz, an input-related noise (IRN) of 0.9 μV_{rms}, a closed-loop gain (A_V) of 40 dB, a power supply rejection ratio (PSRR) of 87.6 dB, and a common-mode rejection ratio (CMRR) of 117.7 dB according to post-simulation data. The proposed CCIA achieves a noise efficiency factor (NEF) of 1.47 and a power efficiency factor (PEF) of 0.56, which allows comparison with the latest research results.

Keywords: ultra-low power; low noise; chopper amplifier; biomedical amplifier

Citation: Pham, X.T.; Kieu, X.T.; Hoang, M.K. Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications. *J. Low Power Electron. Appl.* **2023**, *13*, 37. https://doi.org/10.3390/jlpea13020037

Academic Editor: Orazio Aiello

Received: 9 April 2023
Revised: 15 May 2023
Accepted: 19 May 2023
Published: 24 May 2023

1. Introduction

Wireless sensor biomedicine (WSB) is becoming increasingly popular to monitor our daily activities for early detection of cardiovascular diseases [1–3]. Due to its use in wearable or implantable devices, low-power sensors are required to monitor human biopotential signal. In addition to developing standard applications to improve patients' quality of life, long-term monitoring, mobile monitoring, sports and rehabilitation applications, and brain-computer interfaces will also be realized [4]. Typically, WSBs use a low-noise, low-power instrumentation amplifier (IA) to interface with many types of biomedical sensors. These biopotential signals include electrocardiograms (ECGs) and electroencephalograms (EEGs) from the heart and brain, respectively. Local field potentials (LFPs) and action potentials (APs) are biomarkers useful for both neuroscience research and treatment [5]. Biopotential signals, as shown in Figure 1, have a very low amplitude, ranging from 10 to 100 µV for EEG and about 1 mV for ECG. The biosignals range from 0.5 to 150 Hz [6]. LFP has a bandwidth of 1 to 200 Hz and a peak amplitude of about 1 mV, while APs have a peak amplitude of about 100 µV and occupy a frequency band of 200 Hz to 5 kHz [7]. Therefore, these neural signals must first be amplified before signal processing can be performed.

To improve the quality of neural signals, the readout system often includes an instrumentation amplifier (IA) implemented in CMOS technology. However, the IA has two important noise sources that must be taken into account, flicker noise ($1/f$) and thermal noise [8]. The chopper stabilization technique is commonly used on IA [9,10] to mitigate 1/f noise by up-modulating this noise at low frequencies beyond the spectrum of IA, while leaving thermal noise unresolved. For example, although the designs in [11,12] consume only 2 µW and 1.89 µW, thermal noise remains a concern with values of 100 and 240 nV/Hz,

respectively. In addition, the CCIAs in [13,14] only have a bandwidth of about 500 Hz. Therefore, CCIAs should have a variable bandwidth to allow better bandwidth selection, while biopotential signals are often bandlimited. This work is an extension of the work originally presented at ICCE'22 [15].

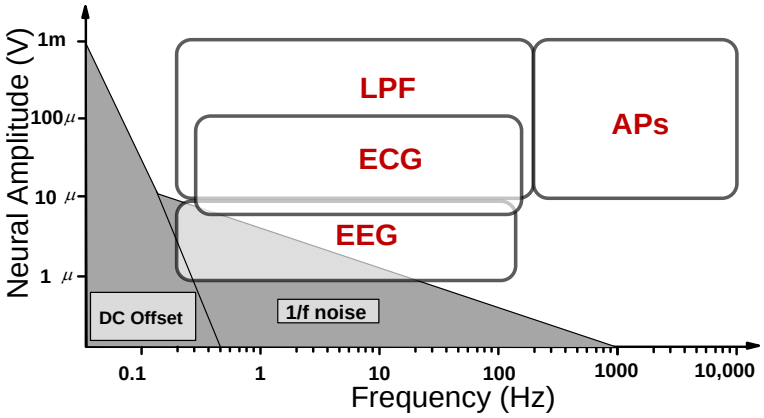


Figure 1. Amplitude and frequency ranges of the characteristics of neural signals.

This paper presents an ultra-low-power CCIA with programmable bandwidth for biomedical applications. To achieve high noise power efficiency, a squeezed inverter amplifier (SQI) operating with a 0.2-V supply is used in the CCIA. In addition, a programmable Miller compensation capacitor is used in the CCIA to obtain flexible bandwidth without additional power consumption. Simulated with a 0.18 µm CMOS technology process, the chip area of the proposed CCIA is only 0.083 mm^2. While the power consumption of 0.47 µW is achieved at the supply voltage of 0.2 and 0.8-V, the proposed amplifier architecture achieves a thermal noise of 28 $nV/\sqrt{Hz}$, an input-related noise (IRN) of 0.9 μV_{rms} over a bandwidth of 1 kHz, a closed-loop gain of 40 dB, a power supply rejection ratio (PSRR) of 87.6 dB, and a common-mode rejection ratio (CMRR) of 117.7 dB according to post-simulation data. The proposed CCIA compares well with the latest research results, with a noise efficiency factor (NEF) of 1.47 and a power efficiency factor (PEF) of 0.56.

2. Design

As we know, to reduce the thermal noise, there are two approaches: (1) The transistors of the amplifier are enlarger, resulting in an increase in chip area; (2) The DC current bias for the amplifier must be increased [8]. However, to achieve low power consumption, the supply voltage must be reduced to a minimum so that the transistor still works well. This is the biggest challenge in designing an amplifier. Therefore, the Squeeze inverter amplifier (SQI) with a supply voltage of 0.2 V is dropped in the proposed design. The multistage capacitively coupled chopper amplifier (CCIA) is shown schematically in Figure 2. Since the input stage (G_{m1}) causes most of the input noise, the low-power and low-noise SQI amplifier is implemented in the first stage to mitigate the noise. To achieve high transconductance, the CMOS transistors are operated at a comparatively high current of 800 nA in the subthreshold region. A low supply voltage $V_{DD,L}$ of 0.2-V is used to power the high-current input stage G_{m1}, which corresponds to two drain-source saturation voltages (V_{DSAT}) of both the PMOS and NMOS transistors in the SQI to reduce power consumption to only about 320 nW. The combination of the output stage of an amplifier with a common source (CS) is used to achieve a large output swing with the middle stage using a folded—cascode amplifier (FC) to achieve high gain. Since the output common mode voltage of the first stage is only 0.1 V, the FC stage must be used with PMOS transistor input pairs. To handle the low-frequency flicker noise ($1/f$), the chopper CH_I is connected before the input capacitor to modulate the input signal V_{in} to the chopper frequency f_{CH} = 10 kHz, which is then modulated down to the baseband by the chopper CH_O. The proposed multistage CCIA creates multiple poles, which reduce the stabilization of the circuit. To ensure stability

while maintaining bandwidth, Miller compensation capacitors $C_{C1,2}$ and resistors $R_{Z1,2}$ are added to the last stage feedback loop.

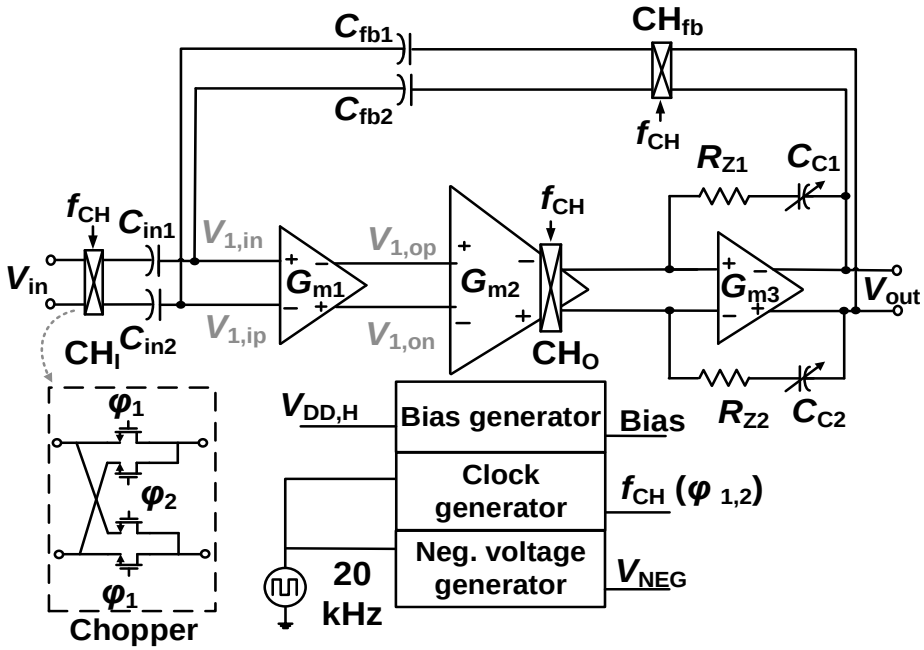


Figure 2. Schematic of the proposed CCIA with $C_{in1,2}$ = 4 pF, $C_{fb1,2}$ = 40 fF, $R_{Z1,2}$ = 0.9 MΩ, $C_{C1,2}$ = 0.62/6.2/30 pF.

As we know, the amplifier is stable when the phase at the loop gain crossover is higher than −180 degrees when the loop gain is 0 dB. By moving either the loop gain crossover or the phase crossover point, i.e., the point where the phase reaches −180 degrees, away from the origin, you can increase the stability. Thus, decreasing $C_{C1,2}$ causes the loop gain crossover of CCIA to move away from the origin, increasing the bandwidth of CCIA. Moreover, the serial nulling resistors $R_{Z1,2}$ are used to reduce the null in the right half plane (RHP) caused by the feedforward using the compensation capacitors. The multi-stage CCIA proposed in this work has a flexible bandwidth from 0.2 to 10 kHz thanks to the programmable Miller compensation capacitors $C_{C1,2}$. In contrast, previous designs [16,17], which also use a multi-stage circuit in the main path, use fixed values of the Miller compensation components so that the bandwidth of these designs is 0.67 and 0.8 kHz, respectively. The midband gain of the CCIA is determined by the ratio of the input capacitances $C_{in1,2}$ and the feedback capacitances $C_{fb1,2}$. In this work, $C_{in1,2}$ = 4 pF, $C_{fb1,2}$ = 40 fF are realized by the metal-insulator-metal (MIM) capacitor technique to reduce the active chip area so that the midband gain of the CCIA reaches 40 dB.

3. Circuit Implementation

3.1. Squeezed-Inverter Amplifier

As shown in Figure 3, the first stage uses the scheme of SQI with a common mode feedback circuit (CMFB) sharing to increase the CMRR. By using an ultra-low voltage supply $V_{DD,L}$ = 0.2-V, the CMOS transistors in the SQI operate in the subthreshold region. The IRN of the first stage can be calculated as follows:

$$\overline{V_{n,in,Gm1}^2} = \frac{8kT}{g_{m,n} + g_{m,p}} \cong \frac{4kTnV_T}{I_{BIAS}} \quad (1)$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductance of the NMOS NM and PMOS PM transistors, respectively, the bias current I_{BIAS} is 0.8 µA, thermal voltage V_T = 26 mV, and the subthreshold factor [18] n = 1.5. The SQI stage operates with low noise by increasing the

bias current. Moreover, due to using an ultra-low-voltage supply of 0.2 V, SQI archives high noise power efficiency.

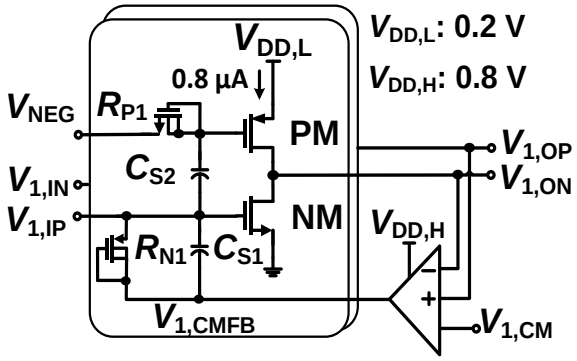


Figure 3. Schematic of SQI C_{S1} = 1 pF, C_{S2} = 4 pF.

The input stage G_{m1} is the main source of noise in the design and requires a large bias current to limit the output noise with $1/f$ noise and thermal noise [15]. The chopping approach can be used to remove the flicker noise while the thermal noise is not compatible with the bias current. Therefore, an acceptable bias current of 0.8 µA was chosen to compensate for an extremely low supply voltage of 0.2 V to reduce noise floor while keeping power dissipation low. To operate at the 0.2 V supply voltage, the negative bias voltages of the input PM and NM transistors in SQI are regulated by a negative bias generator and a CMFB loop. A negative voltage V_{NEG} generated by the negative bias generator (see Figure 3) is used to bias the PM input transistor via a pseudo-resistor $R_{P1,2}$. The gate voltage of the transistor NM is controlled by a common CMFB loop [10] driven by a high voltage source $V_{DD,H}$ = 0.8-V to maintain the common output voltage of SQI at $V_{DD,L}/2$. Capacitors $C_{S1,2}$ are used for AC coupling. Since the subthreshold transistors operate without a tail current source, it is challenging to balance the bias current for the input pairs using the CM voltage. Therefore, a common CMFB circuit, as shown in Figure 4, is required for the SQI differential branches to solve this problem. By using a voltage of $V_{1,CM}$ = 0.1-V as a reference, a negative feedback loop is created to monitor and adjust the output common mode voltage of the SQI. The output of the CMFB, $V_{1,CMFB}$, is used to control the gate voltage of the transistor NM in each SQI branch through a pair of pseudo-resistors $R_{N1,2}$. This approach provides balanced bias currents for the SQI stage since any change in $V_{1,CMFB}$ affects the input pair by the same amount.

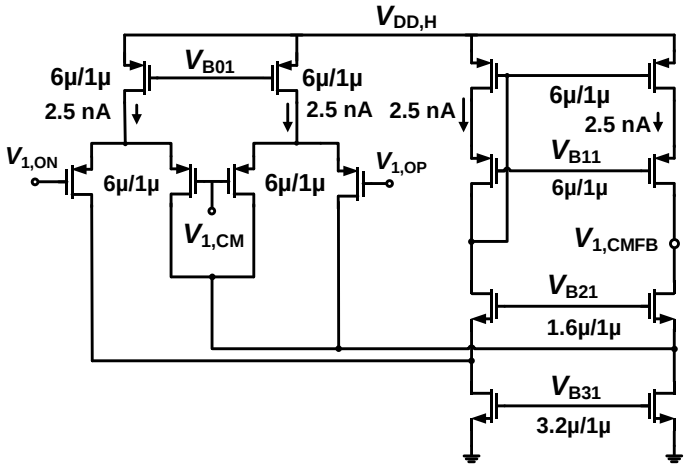


Figure 4. Schematic of CMFB circuit of the SQI.

3.2. Bias Circuit for Squeezed-Inverter Amplifier

As we know, CMOS transistors must be biased in SQI, but the extremely low supply voltage $V_{DD,L}$ = 0.2-V makes this difficult. While PM transistors need a negative bias voltage lower than ground, the voltage drives the gate of the NM transistors using a CMFB through the high voltage supply $V_{DD,H}$ = 0.8-V. In the conventional negative voltage generator [16], a switched capacitor loop (SC) is used, in which a 1/10 scaled replica M_{PB} of the PMOS input transistor is used to generate the negative voltage to regulate the bias current of the SQI. M_{PB} and the FC work together to provide a negative feedback loop that continuously regulates V_G during the time that the drain voltage is held at $V_{DD,L}/2$. An SC network is also used by the feedback loop to hold V_G below ground. A low-noise copy of V_G is created using a low-pass filter replica (V_{NEG}). To prevent switching spikes from affecting the desired signals, a frequency of 20 kHz is used by this SC. To turn off the switches completely, a negative level shifter is driven by V_G or V_{NEG}. However, after each switching period, the level shifter supplies its "ground" rail, increasing the voltage differences between V_G and V_{NEG} during startup. The negative feedback loop has V_G fixed, so inaccurate replication of V_{NEG} will result in an unexpected bias current. V_{NEG} will be higher than V_G, when the level shifter uses V_{NEG}. As a result, the bias current of SQI will be reduced, which will increase the input noise. On the other hand, the bias current will be lower than predicted when this level shifter is driven by V_G, which drastically increases the power consumption. Therefore, an auxiliary path is needed to generate a voltage V_B, a replica of the voltage V_G to supplement the negative voltage generator circuit. The proposed negative bias voltage generator is shown in Figure 5. The V_B-fed negative voltage for the level shifter does not affect V_G and V_{NEG}. Therefore, the bias current of SQI is set to the appropriate value, and V_{NEG} is an exact duplicate of V_G. According to the simulation results shown in Figure 6, the expected level of V_{NEG} is about −150 mV after V_G or V_{NEG} is used by the level shifter but is changed to about −100 mV or −210 mV accordingly after the start time. Since only V_B is supplied by the dynamic current of the level shifter, V_G and V_{NEG} are controlled by an equal voltage of −150 mV when V_B is injected. The improved negative bias generator in the SQI circuit achieves a bias current of 1.56 µA or an almost theoretical value of 1.6 µA.

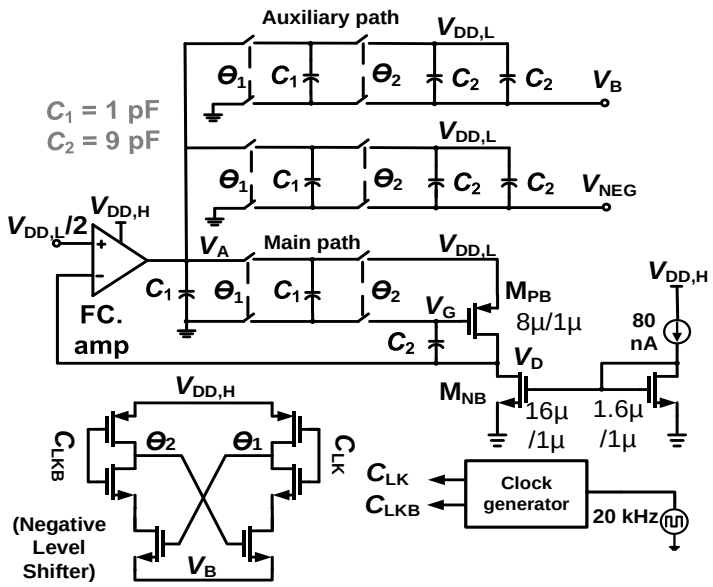


Figure 5. Schematic of negative voltage bias generator circuit.

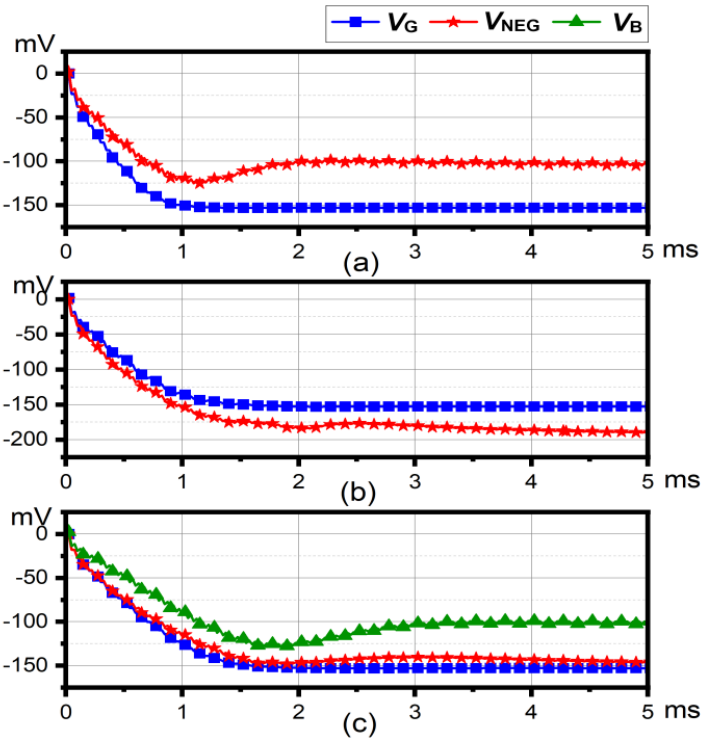


Figure 6. Simulated results of the negative voltage generator when the level shifter is powered by (**a**) V_{NEG}, (**b**) V_G, (**c**) V_B.

Monte Carlo simulation results of the negative voltage V_{NEG} and bias current of SQI (one branch) are shown in Figure 7, where both random process variations and mismatches were considered. The results of the Monte Carlo simulation with 200 samples show that the average value of V_{NEG} is −147.6 mV and the bias current of SQI is 785.6 nA with a standard deviation of 14.9 mV and 15.2 nA, respectively. The effect of temperature and variable $V_{DD,L}$ on the open-loop gain of SQI is shown in Figure 8. The temperature and variable $V_{DD,L}$ are examined from −15 to 70 degrees Celsius and 0.1 to 0.3-V, respectively. At a temperature of 27 degrees Celsius and a $V_{DD,L}$ of 0.2-V, the open-loop gain of the SQI reaches about 30 dB.

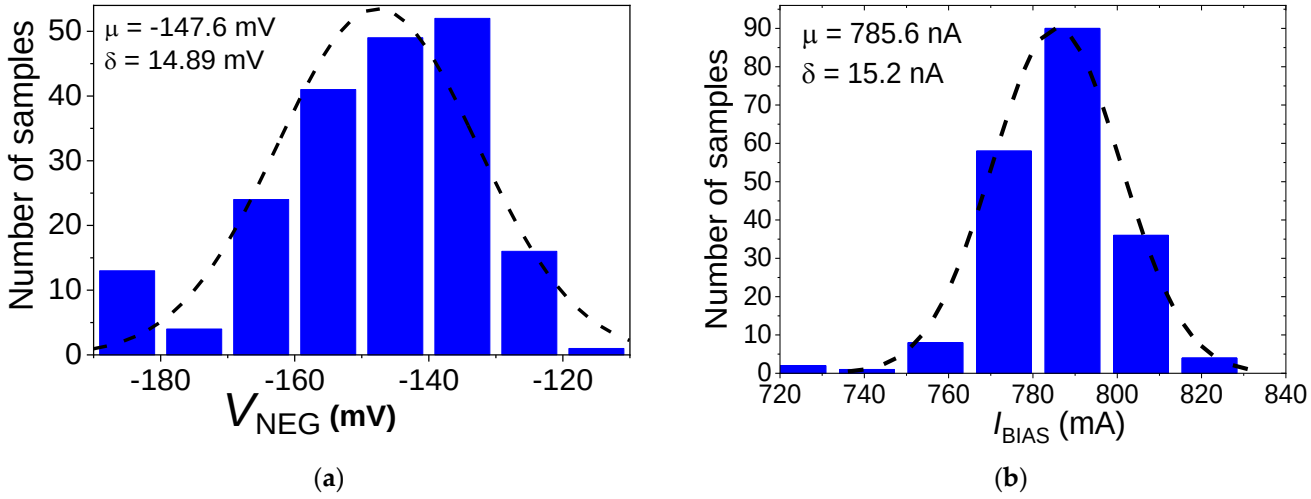


Figure 7. The result of Monte Carlo simulation of (**a**) negative voltage V_{NEG} (**b**) the bias current of SQI.

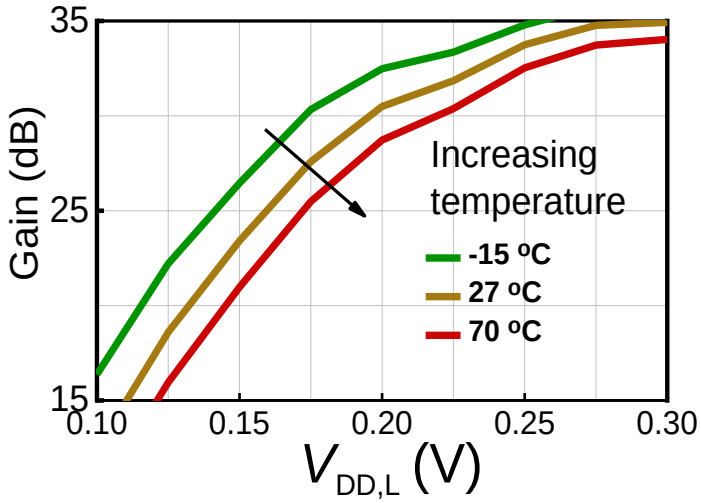


Figure 8. Simulated gain of the SQI stage depending on $V_{DD,L}$ and temperature.

3.3. Middle and Output Stage

To obtain high gain and output swing, the middle and last stage of CCIA employs the FC and the CS amplifiers, respectively. The schematic of FC is shown in Figure 9, while the schematic of CS with the phase margin compensation circuit is shown in Figure 10. Using a supply voltage $V_{DD,H}$ of 0.8-V, the FC is biased a DC current of 40 nA while CS draws a DC current of 80 nA. Although the current consumption is much lower than SQI's current drawing, the effect that the noise of the G_{m2} and G_{m3} have on the input is very small because it is divided into the gain of G_{m1} (normally 30 dB). The FC input pair must use PMOS transistors interfacing to SQI's low output voltage of around 0.1-V. The G_{m3} that employs CS with a passive CMFB circuit built by the pseudo resistors in parallel with MIM capacitors is also shown in Figure 10a. The network compensation capacitor $C_{C1,2}$ is shown in Figure 10b. $C_{C1,2}$ is built from three parallel capacitors (0.62 pF, 5.58 pF, and 23.8 pF); therefore, the value of $C_{C1,2}$ can be changed from 0.62 pF to 30 pF by the controlling switches $SW_{1,2,3}$.

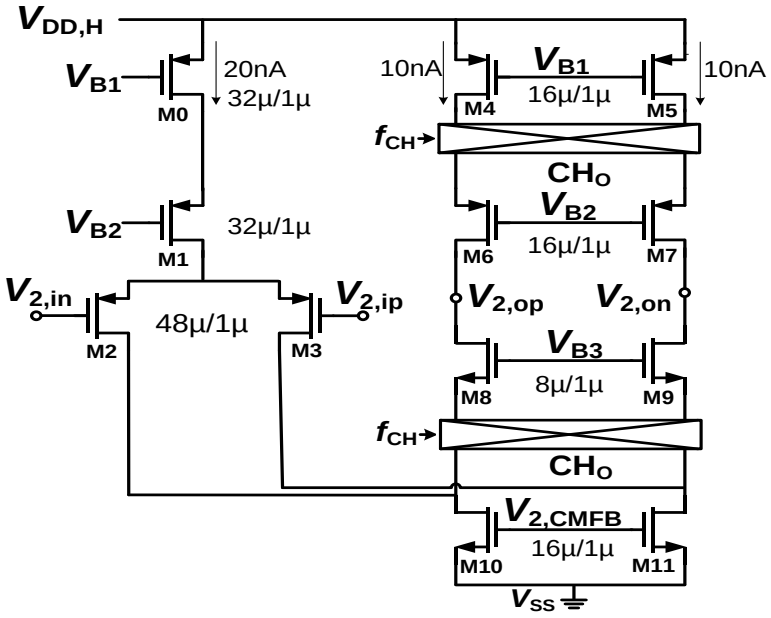
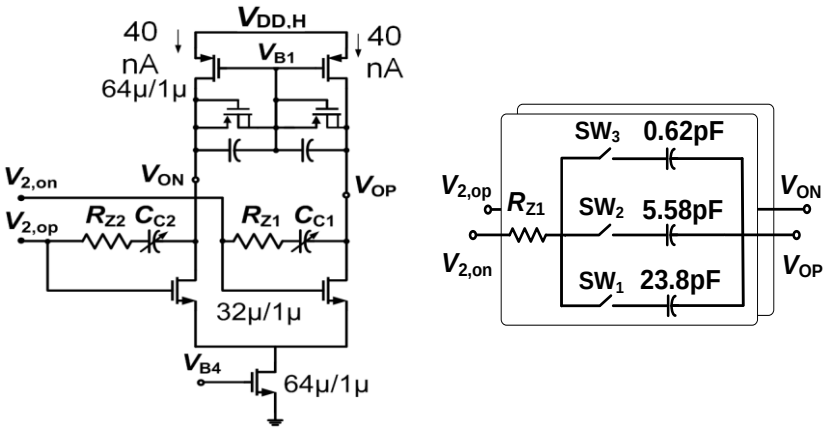


Figure 9. The schematic of the FC amp circuit.



(**a**) (**b**)

Figure 10. (**a**) The schematic of CS amp circuit, (**b**) the schematic of phase margin compensation circuit.

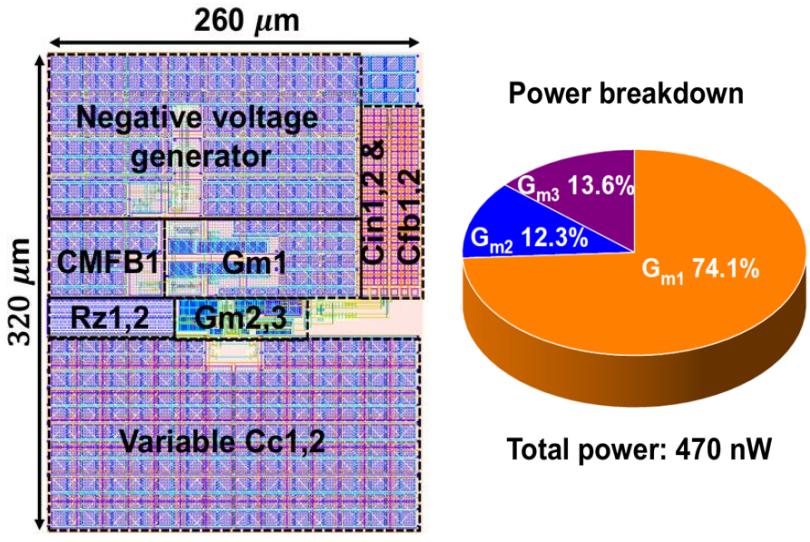
The IRN of the proposed CCIA, $\overline{V_{n,in}^2}$ can be calculated as

$$\begin{aligned}\overline{V_{n,in}^2} &= \left(\frac{C_{tot}}{C_{in1,2}}\right)^2\left(\overline{V_{n,in,Gm1}^2} + \frac{\overline{V_{n,in,Gm2}^2}}{A_{V1}}\right) \\ &= \left(\frac{C_{tot}}{C_{in1,2}}\right)^2\left[\frac{4kTnV_{th}}{I_{BIAS}} + \frac{8kTn}{A_{V1}g_{m1,2}}\left(1 + \frac{g_{m3,4}+g_{m9,10}}{g_{m1,2}}\right)\right]\end{aligned} \quad (2)$$

where $C_{tot} = C_{in1,2} + C_{fb1,2} + C_p$, C_p is the parasitic capacitance of the first stage, $\overline{V_{n,in,Gm1}^2}$ and $\overline{V_{n,in,Gm2}^2}$ are the IRN of G_{m1} and G_{m2}, respectively.

4. Simulation Results

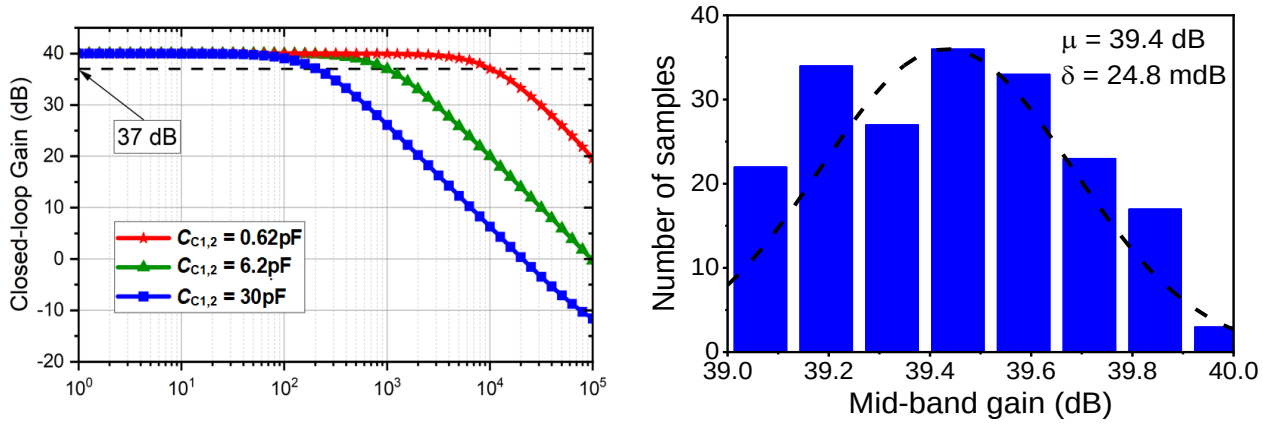
In the 0.18 µm CMOS technology, Figure 11 shows the microphotography of the layout and the power decay of the CCIA. The chip area of the CCIA layout occupies only 0.083 mm^2. With a $V_{DD,L}$ of 0.2-V and a $V_{DD,H}$ of 0.8-V, the simulated total power dissipation of the CCIA is 470 nW. G_{m1}, G_{m2}, and G_{m3} consume 74.1%, 12.3%, and 13.6% of the power, respectively.



(**a**) (**b**)

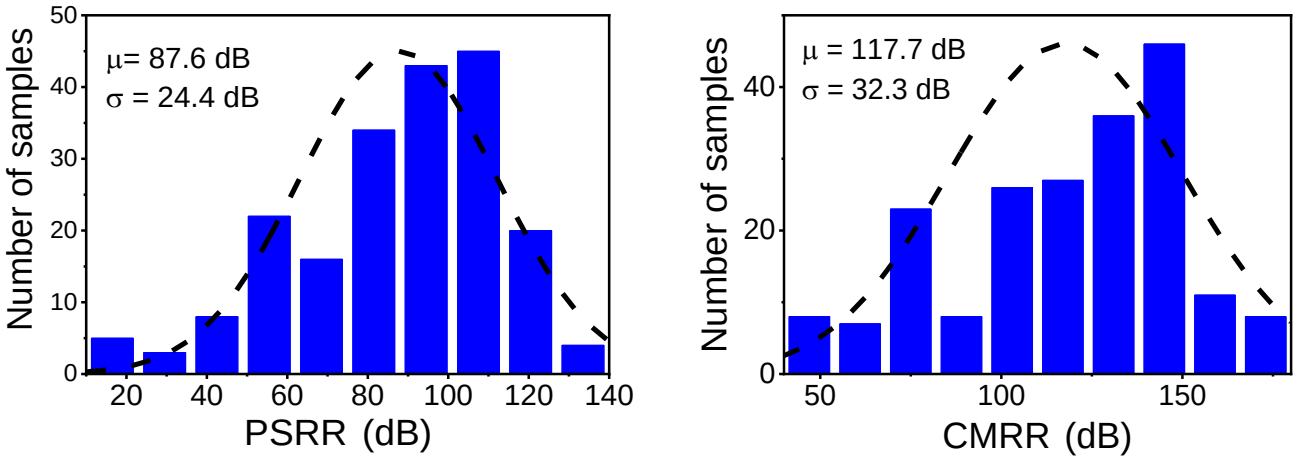
Figure 11. (**a**) Microphotograph and (**b**) the power breakdown of the fabricated CCIA.

The amplitude–frequency response and Monte Carlo simulation of the midband gain of the proposed CCIA are shown in Figure 12. The closed-loop gain reaches 40 dB while passing 200 samples, the Monte Carlo simulation results of the midband gain show that the closed-loop mean value of the CCIA gain is 39.4 dB with a standard deviation of 24.8 mdB. Since the capacitance value of $C_{C1,2}$ is programmable, the bandwidth of the CCIA can be successfully adjusted from 0.2 to 10 kHz. This design is suitable for recording biomedical signals with variable frequency bands. The Monte Carlo simulation results of the power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) are shown in Figure 13 after a run of 200 samples. Figure 13 shows the average value of PSRR of 87.6 dB at a supply voltage of 0.2-V and CMRR of 117.7 dB with standard deviations of 24.4 and 32.3 dB, respectively.



(**a**) (**b**)

Figure 12. (**a**) The CCIA's variable bandwidth of the transfer function, (**b**) CCIA's the Monte Carlo Simulation of the middle-band gain.



(**a**) (**b**)

Figure 13. The Monte Carlo simulation result of (**a**) the CCIA's PSRR, (**b**) the CCIA's CMRR.

Figure 14 shows the input noise of the proposed CCIA. At a bandwidth of 1 kHz, the IRN of the CCIA is 0.9 μV_{rms} with a thermal noise of 28 nV/$\sqrt{\text{Hz}}$ and a $1/f$ corner of 4 Hz. To investigate the effect of process corners on noise, Monte Carlo simulations were performed with random mismatches of the devices with 200 samples. Figure 15a shows how the IRN of the proposed amplifier changes from 0.894 to 0.963 μV_{rms} over several process corners, while Figure 15b shows the average IRN, which is 0.916 μV_{rms}, with a standard deviation of 62.2 $\text{n}V_{\text{rms}}$. The performances of the proposed CCIA operating in different bandwidth modes are summarized in Table 1. The IRN of the proposed CCIA

over the bandwidths of 0.2/1/10 kHz is 0.4/0.9/2.8 μV_{rms}. NEF and PEF show practically comparable values of 1.49 and 0.56, respectively, when the bandwidth changes as the IRN scales with the integrated bandwidths.

$$^{\dagger}\text{NEF} = V_{\text{ni,rms}} \times \sqrt{\frac{I_{\text{DC}}}{\pi V_T 4kT \times BW}};\ ^{\dagger\dagger}\text{PEF} = V_{\text{ni, rms}}^2 \frac{2P_{\text{DC}}}{\pi V_T 4kT \times BW} = \text{NEF}^2 \times V_{\text{DD}} \quad (3)$$

where I_{DC} is the total current consumption, V_{T} is the thermal voltage, k is the Boltzmann constant, BW is the bandwidth of the proposed CCIA over which the noise is integrated, and V_{DD} is the voltage supply.

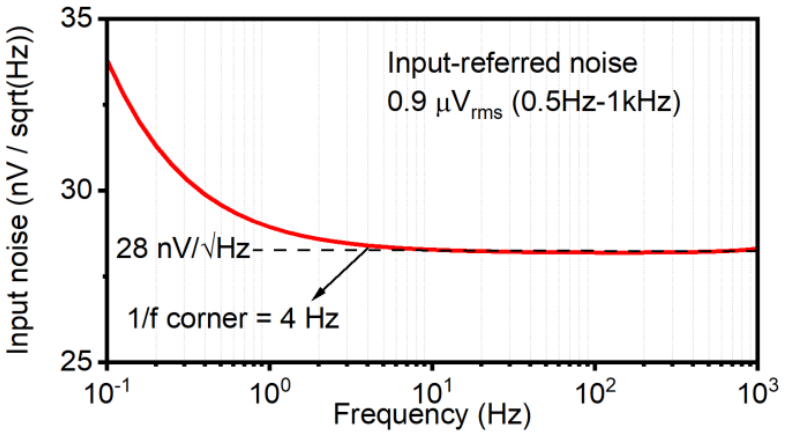
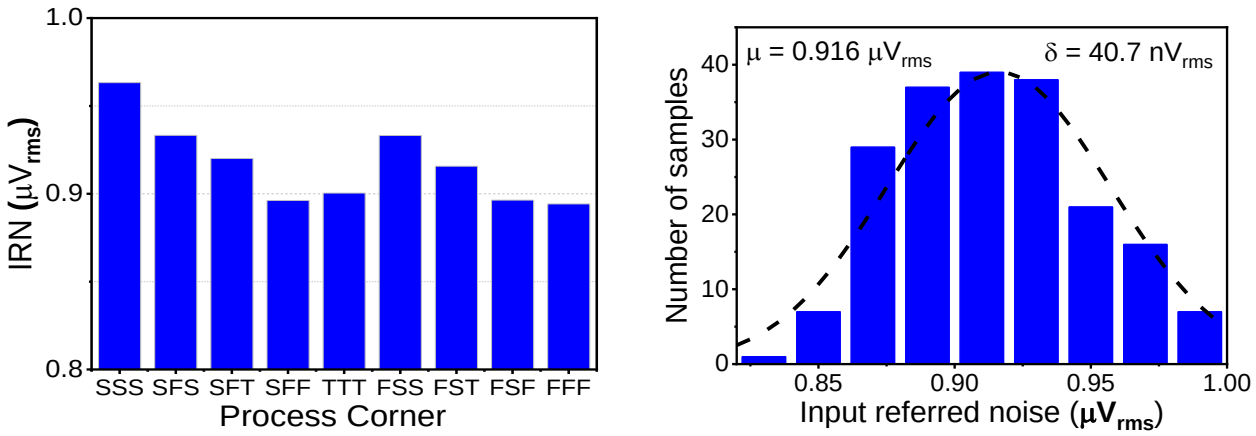


Figure 14. The simulation result of the CCIA's input-referred noise.



(**a**) (**b**)

Figure 15. The simulation result of (**a**) the CCIA's IRN depending on the process corners and (**b**) the CCIA's input-referred noise.

Table 1. Performance analysis with varying bandwidth.

Miller Compensate Capacitors $C_{C1,2}$ (pF)	**30**	**6.2**	**0.62**
Bandwidth—BW (kHz)	0.2	1	10
Thermal noise (nV/$\sqrt{}$H z)	28	28	28
Input-referred noise—$V_{\text{ni,rms}}$ (μV_{rms})	0.4	0.9	2.8
Noise Efficiency Factor (†NEF)	1.49	1.49	1.47
Power Efficiency Factor (††PEF)	0.56	0.56	0.55

Table 2 contains several references with simulation results, including [6,19–21] for a fair comparison. The key design specifications such as power consumption, bandwidth, thermal noise, CMRR, PSRR, NEF, and PEF are summarized in this table to compare the achieved performance of the proposed design with the state-of-the-art designs. By choosing different bandwidths, the proposed CCIA achieves a competitive PEF of about 0.56 with a low input noise of 28 nV/$\sqrt{}$Hz and a noise corner of up to 4 Hz with a power consumption of 0.47 µW.

Table 2. Performance comparison of the proposed CCIA.

Ref.	[6]	[16]	[17]	[19]	[20]	[21]	[22]	[23]	**This Work**
Year	2022	2017	2021	2020	2020	2018	2022	2018	2023
Supply (V)	1	0.2/0.8	0.2/0.8	1.8	1.2	1	0.5/1.8	1.5/3.3	0.2/0.8
Power (µW)	1.21	0.79	0.52	3.96	1.9	0.96	4.5	330	0.47
Gain (dB)	40	57.8	39.6	31.7	58.4	62	60	1/12/20/40	40
Bandwidth (kHz)	0.8	0.67	0.8	9	8.7	0.23	300	1250	0.2/1/10
Flexible Bandwidth	N	N	N	N	Y	N	N	N	Y
Thermal noise (nV/$\sqrt{}$Hz)	121	36	32	49.5	N/A	N/A	13	60	28
CMRR (dB)	108	85	104	85	110	88	84	90	117.7
PSRR (dB)	87	80	82	87	87	101	88	100	87.6
†NEF	5.4	2.1	1.7	2.08	1.47	3.34	1.3	29	1.49
††PEF	29.7	1.6	0.7	7.78	2.59	9.06	1.1	N/A	0.56
Tech. (nm)	180	180	180	180	130	180	180	180	180
Sim./Meas.	Sim.	Meas.	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.	Sim.

5. Conclusions

This paper describes the design and simulation of an ultra-low-power, programmable bandwidth, capacitively coupled instrumentation amplifier operating on a 0.2 V supply for biomedical applications. By implementing it in a standard 0.18 µm CMOS technology, the chip area of the CCIA occupies only 0.083 mm^2. By using programmable Miler compensation capacitors, the bandwidth of the CCIA can be changed from 200 Hz to 10 kHz. Thanks to the SQI in the first stage and the chopping technique, the CCIA can achieve high power efficiency and low noise. With a power consumption of only 470 nW at $V_{DD,L}$ of 0.2-V and $V_{DD,H}$ of 0.8-V, the prototype ultra-low-power amplifier IC achieves a closed-loop gain of 40 dB, a CMRR of 117.7 dB and a PSRR of 87.6 dB. The CCIA thermal noise is 28 nV/$\sqrt{}$Hz, resulting in an IRN of 0.9 µV_{rms} over a bandwidth of 1 kHz. Therefore, NEF of 1.49 and PEF of 0.56 are achieved. This shows that the performance of the proposed CCIA can be compared with the latest studies.

Author Contributions: Conceptualization, X.T.P., X.T.K. and M.K.H.; methodology, X.T.P., X.T.K. and M.K.H.; software, X.T.P.; formal analysis, X.T.K. and M.K.H.; writing—original draft preparation, X.T.P.; writing—review and editing, X.T.K. and M.K.H.; visualization, X.T.P. and M.K.H.; supervision, X.T.K.; project administration, X.T.P.; funding acquisition, X.T.P., X.T.K. and M.K.H. All authors have read and agreed to the published version of the manuscript.

Funding: The research was funded by Hanoi University of Industry Research Fund under grant number 19-2022-RD/HD-DHCN.

Conflicts of Interest: The authors declare no conflict of interest.

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