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Ultra-low power transmit/receive ASIC for battery operated ultrasound measurement systems

Jonny Johansson*, Martin Gustafsson, Jerker Delsing

EISLAB, Luleå University of Technology, SE-971 87 Luleå, Sweden

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Absract

This paper describes the design of the complete transmit and receive electronics circuitry for a piezoelectric transducer in one single ASIC. The chip will be one building block in a thumb size battery operated ultrasound measurement system. The main design target has been to achieve extremely low power consumption while keeping the number of external components minimal.

To overcome the dynamic range limitations imposed by a battery supply an on-chip boost converter uses one external inductor to generate up to 40 V for excitation of the transducer. The transducer itself is used as a storage capacitor, whereafter it is rapidly discharged to generate an ultrasound pulse. An on-chip amplifier with intermittent operation is controlled by a state machine and used to amplify incoming echoes. The chip has been fabricated in a 0.8 μm high voltage CMOS process, with a total chip area of 12 mm^2.

Measurements verify the design approach. The power consumption for the system reaches within a factor of 2 of the power needed to charge the capacitance of the piezoelectric transducer from a fixed voltage source. The results show the possibility to achieve extremely low power consumption in a battery operated pulse–echo ultrasound measurement system.

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Keywords: Ultrasound; ASIC; Low power; Sensor; Microelectronics

1. Introduction

Ultrasound measurement equipment are used in a vast array of areas, e.g. medical imaging and non-destructive evaluation (NDE) [1]. Many of these systems are pulse–echo systems, where a piezoelectric or micro-machined transducer is used to generate the ultrasound pulse, as well as to receive the reflected echo. Traditionally the transducer or transducer elements are built in a probe head or scanner, which is connected via coaxial cabling to the electronics unit used for pulse excitation and reception. If all the electronics needed for pulse generation and reception could be integrated in the scanner or probe head, and the unit be equipped with wireless communication, all cabling could be omitted. The flexibility, e.g. in a medical environment would be greatly enhanced. Further, if the probe head is equipped with a CPU core and wireless communication, applications within sensor networking and ambient intelligence would be feasible [2,3].

One important step to reach this target is to miniaturize driver and receiver electronics for the system. Several papers have recently been published in this field. On the receiver side, they concern the integration of amplifiers, A/D converters and signal conditioning [4–7]. On-chip drivers for single element piezoelectric transducers and transducer arrays have been published [8,9]. For capacitive micro-machined ultrasonic transducers (CMUTs), complete front end [10] as well as the integration of a high voltage dc/dc converter has been reported [11].

For a portable wireless probe head or scanner it is not only the size of the electronics that is important. Also the power consumption is crucial, as the device will be battery operated. Further, the limitation imposed the low supply voltage of the battery must be overcome for pulse generation.

This paper describes the design of the complete transmit and receive electronics for a piezoelectric transducer into one single application specific integrated circuit (ASIC). The chip is intended to be operated from a single lithium battery with a supply voltage of 3.6 V. Such a low supply voltage limits the amount

* Corresponding author. Tel.: +46 920 491703; fax: +46 920 492082.
E-mail address: jonny.johansson@1tu.se (J. Johansson).

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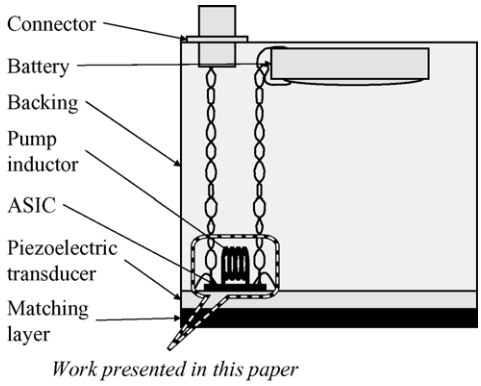

Fig. 1. Proposed sensor design with battery cast into the backing material. The work presented in this paper concerns the electronics integrated in a single ASIC as indicated in the figure.

of ultrasound energy that can be generated. To overcome this, the piezoelectric transducer is charged with an on-chip boost converter, which uses one external inductor to generate up to 40 V on the crystal. The design has three main building blocks: a charge/discharge unit, an amplifier and a state machine to control the functionality. The function of the chip is completely autonomous and does not require any external control signals or clocks.

The main design target has been to achieve extremely low power operation while the number of external components is kept minimal. Adiabatic charging achieved by an inductive pump together with intermittent operation of the on-chip amplifier helps to achieve this target. The use of system level simulation including both ultrasonic devices and electronics is an important tool in this design process. To achieve this, SPICE models for the piezoelectric device has been used directly in the development environment used for chip simulation and layout.

Section 2 in this paper presents an in depth discussion of the system level considerations that have been taken to achieve the set target. Strategies for pulse generation and system level power optimization as well as the requirements set on the amplifier are discussed. Section 3 presents the circuit solutions chosen to achieve the required functionality. Measurement results and discussion are presented in Section 4, whereafter conclusions are drawn.

2. System level considerations

The aim with the work presented in this paper is to form one of the building blocks for a portable, battery operated ultrasound sensor system as discussed in Section 1 above. A proposed sensor design is shown in Fig. 1. Here, the battery is cast into the rear part of the backing which is used to tailor the shape of the generated ultrasound pulse [12]. The electronics is integrated in one single ASIC which is mounted directly on the piezoelectric transducer [13].

The output of the sensor system is here depicted as a coaxial connector. This could be replaced with a direct connection to a microprocessor system with integrated wireless communication, e.g. as discussed in [14].

The building block presented in this paper is an ASIC containing the complete transmit and receive electronics for a piezoelectric transducer. The initial design requirements were:

- *Autonomous operation*. The chip must be capable to operate fully autonomously, without external clocks or bias generators.
- *Battery operation*. The chip shall be able to operate from power supplies ranging between 3.6 and 5.2 V, enabling operation from one single lithium battery. The power consumption must be minimized to provide long battery life time.
- *HV pulse generation*. The use of only one battery voltage to generate the excitation pulse for the transducer will limit the amount of output ultrasound energy. This will highly impair the dynamic range of the measurement system. Thus, a high voltage generation circuit shall be incorporated on the chip.
- *External components*. The number of external components to generate the high voltage shall be kept to a minimum. This provides easier assembly and lower cost for production.
- *Amplifier*. The chip shall host an amplifier for the received pulses in a pulse–echo system. The amplifier shall be optimized for intermittent operation to minimize the power consumption.

The following subsections describe strategies for pulse generation, system level power optimization and amplifier design. Also, the models used to perform system level simulations are presented.

2.1. Pulse generation strategy

The target system for this design is a pulse–echo system where the transducer oscillates at its natural oscillating frequency. Traditional high energy excitation systems discharge a capacitor over the piezoelectric disc to generate a spike type excitation pulse [15]. Other solutions are to use a gated sinusoidal waveform, a square wave pulse, or an arbitrary waveform generated by a digital-to-analog converter [16,17]. For an on-chip integration, both the losses in the system as well as the complexity of the electronics must be taken into account. The use of a square wave excitation combines fairly simple circuitry with very good pulse control and low internal loss [9,13]. Generation of a gated sinusoidal or an arbitrary waveform increases the complexity of the electronics. The drawback of these solutions is that they require a high voltage power supply from which to generate the desired waveforms, e.g a storage capacitor at the output of an on-chip dc/dc converter.

The design presented in this paper takes a different approach. Here, the piezoelectric transducer itself is used as storage capacitor. The transducer is slowly charged by the high voltage generation block, whereafter it is rapidly discharged to create an ultrasound pulse. Key features of the approach are:

- No external storage capacitor is required. This reduces the size as well as the power consumption for low pulse repetition rates, as no high voltage buffer needs to be maintained in between pulses.

- It requires only one transistor sized to handle the peak currents for discharging. This is significant, as these transistors occupy a fair amount of chip area.
- The single edge excitation trades pulse control for simplicity. It requires no control of any pulse widths. This significantly reduces the complexity of the electronics, as the pulse width of a square wave excitation needs to be controlled down to ns-level.
- Adiabatic charging of the transducer can be achieved. This can reduce the energy consumption for the excitation with almost a factor of 2 compared to charging and discharging from a fixed voltage source [18]. It should however here be noted that excitation with a single edge does not generate as much output energy as does the excitation with a square wave.

Two main paths are available to generate the high voltage; either a capacitive charge pump [19,20] or an inductive boost converter [21,22]. The requirements for high efficiency (low power) on one hand and no external components on the other are highly contradictive. Best case efficiencies of up to 85–90% can be achieved with external components for low voltage increase ratios. The efficiencies for solutions with on-chip inductors and pump capacitors are highly dependent on the load conditions and voltage increase ratio. For a converter with an on-chip inductor an efficiency of 28% has been reported [21], while the capacitive pump has achieved 65% [23]. The large value of the target capacitance of the piezoelectric transducer (nF-range) further hampers the efficiency of an on-chip solution, as the achievable capacitance and inductance values are low.

This work aims at a 10-fold increase in voltage level. This will reduce the efficiency for the capacitive charge pump also in the case where discrete components are used, as the number of stages has to be high. Further, several stages in a charge pump would require several external capacitors. The solution with an inductor based boost converter requires only one external component. The circuit complexity is also lower than that for a charge pump. Thus, the decision was taken to use an inductive boost converter with a single external inductor to generate the high voltage required for excitation.

2.1.1. Transducer capacitance

The capacitive behavior of the used piezoelectric transducer is an important design parameter both for the inductive charge pump and the discharge block. The intention with this section is to give an introduction to this behavior and to give approximate values for the target transducers of this design.

A piezoelectric ceramic transducer can, as an approximation outside of its resonance regions, electrically be viewed as a parallel plate capacitor with a capacitance:

$$C_0 = \frac{A\varepsilon_0 K}{d}. \tag{1}$$

Here ε_0 is the permittivity in free air, K the dielectric constant of the material, A the area of the transducer, and d is its thickness [24]. The governing parameter here is K, which varies with frequency and mechanical state for a piezoelectric material. The *free* dielectric constant K^{T} is often measured at 1 kHz where the transducer is free to move. The *clamped* dielectric constant K^{S} on the other hand is measured on a frequency above all resonances and their harmonics (several MHz), where inertia blocks the movement of the transducer. In a sensor application, the amount of clamping depends on the materials used in the design as well as the frequencies considered. For the experiments and simulations performed in this paper, the transducer is mounted on a backing of plexiglas (PMMA) with water on the opposite side.

Thus, for the low frequencies encountered, e.g. during the charging from a charge pump or boost converter, the disc can be regarded as free.

In the remainder of this paper, the notations C_0^{K} and C_0^{S} are used for the capacitance of the piezoelectric disc in free and clamped states, respectively. Approximate values of C_0^{K} for Pz27 piezoceramic discs with diameters from 5 to 20 mm with frequencies from 1 to 4 MHz range from 0.2 to 10 nF [25]. The values of C_0^{S} are approximately a factor of 2 lower. The resistivity of the Pz27 material is about 5×10^{10} Ωm. Thus, the unloaded free time constant for a circular transducer as those considered here is about 800 s.

2.2. Power saving strategies

Low power consumption is vital to preserve battery lifetime in a portable system. This section describes system level power saving strategies applied in this design.

A pulse–echo system works intermittently by its nature, with the pulse repetition rate f_{rep} set by the application. Somewhere in the time interval $T_{\mathrm{rep}} = 1/f_{\mathrm{rep}}$ between two excitation pulses, an echo is assumed to arrive. The duration of the echo is normally much shorter than T_{rep}. Thus, an efficient way to save power in these types of systems is to power up the receiver and signal conditioning electronics only when an echo is awaited. Obviously, this places the added requirement that the approximate arrival time of the echo must be known beforehand. If a reception window of:

$$T_{\mathrm{amp}} = \frac{T_{\mathrm{rep}}}{10} \tag{2}$$

can be used, 90% of the power consumed by the amplifier is saved. As the power consumption of the digital control clocks and logic required to achieve the functionality is low compared to that of the amplifier (μW versus mW), large power savings can be made.

Another aspect of power concerns the dynamic range on system level, i.e. the attenuation that can be tolerated for the ultrasound pulse. This is decided by both the amount of energy that is transmitted and the possibility to amplify a received pulse–echo. The system in this paper opens the possibility to increase the received signal level from both ends; either by an increase in excitation voltage or by an increase in amplification. The system energy efficiency can be further enhanced if this possibility is used correctly.

Assuming adiabatic charging, the electrical energy required to increase the ultrasound pulse energy by a factor k^2 by an

increase in the excitation voltage is:

$$\Delta W_{\text{exc}} = \frac{1}{2} C_0^{\text{K}} U^2 (k^2 - 1). \quad (3)$$

Here, U is the initial excitation voltage. An amplifier that consumes a current I_{amp} from a supply voltage V_{sup} will consume the energy:

$$W_{\text{amp}} = I_{\text{amp}} V_{\text{sup}} T_{\text{amp}} \quad (4)$$

during the on time T_{amp}. Thus, by setting $W_{\text{amp}} = \Delta W_{\text{exc}}$ we can get

$$I_{\text{amp}} = \frac{C_0^{\text{K}} U^2 (k^2 - 1)}{2 V_{\text{sup}} T_{\text{amp}}}. \quad (5)$$

This gives an indication of the supply current that can be used for the amplifier in a given system as compared to an increase in the excitation voltage.

As an example consider a 10 mm diameter Pz27 disc with a center frequency of 4 MHz. This has a free capacitance of about 2.6 nF. Thus, the energy cost to increase the transmitted pulse energy a factor of 100 ($k = 10$) is $\Delta W_{\text{exc}} = 1.7\,\mu\text{J}$, assuming that the initial excitation voltage is 3.6 V. This amount of energy can supply an amplifier with 4.6 mA from a 3.6 V supply during a time of 100 μs. Thus, in this specific case, the amplifier is more energy efficient if it can achieve a voltage amplification higher than 10 times on this supply current.

One important factor must be taken into account when considering whether to increase the excitation energy or the amplification: the signal-to-noise ratio (SNR) of the received and amplified echo signal. An increase in the transmitted pulse energy will increase the SNR in the receiving end of the system. An increase in amplification factor will only achieve this if it is accompanied by a similar decrease in amplifier equivalent input noise level.

2.3. Amplifier requirements

In many cases of the design of amplifiers for piezoelectric sensors, the target is not only to amplify the received signal but also to achieve an impedance matching to the connected cable. As the intention with the presented design is future integration of all electronics onto one chip, the cable matching is irrelevant. Instead the amplified signal shall be presented to an A/D converter or other signal processing electronics. The amplifier must then be designed for a dynamic range higher than the subsequent signal processing electronics if it is not to limit the performance of the system. Apart from noise and bandwidth requirements, the amplifier should be optimized and designed for rapid start up as it will only be used intermittently as discussed in Section 2.2 above.

Amplifier design for ultrasound systems is well covered in the literature [4,5,26]. The included amplifier is optimized as a building block for use in the current system. A summary of the amplifier design goals are found in Table 1. Applications under development within the department concern density and flow measurement, which require a dynamic range of 10–12 bits.

Table 1
Amplifier design goals and measured results

Parameter	Target	Measured
Bandwidth (MHz)	10	10.5
Gain (dB)	20	19.5
Startup time (μs)	10	3
Supply current (mA)	5	2.1
Equivalent input noise (μV_{RMS})	<17	45
Output load	5 pF, 10 MΩ	n.a.

Thus, the noise target was set to achieve 12 bits of output dynamic range for ±1.2 V output swing. The bandwidth is sufficient to handle a signal from a 4 MHz transducer. The current consumption target is set based on the discussion in Section 2.2. On-chip bias generation was included in the design to achieve autonomous operation of the complete system. The closed loop gain was set to 20 dB, which was deemed a reasonable target based on the desired bandwidth and previously published amplifier performance in a similar process [27].

2.4. Simulation and design environment

An ultrasound sensor system incorporates mechanical as well as electrical components. The behavior of the transducer and the ultrasound propagation is one factor that sets the requirements on the electronics and decides the overall system performance, e.g. power consumption. In the design of electronics for the system it is thus advantageous if the behavior of these parts can be included in the simulations. To achieve this system level simulation, SPICE models of the ultrasound system have been used within the design tool for integrated circuits. The model uses an electrical equivalent circuit to model the piezoelectric transducer [28–31]. A schematic of the model is shown in Fig. 2. The voltages at the mechanical ports represent the acoustic pressure, and the currents represent the particle velocity at the transducer surfaces.

The electrical port is equivalent to the connections to the electrodes at the transducer surfaces. The piezoelectric effect is modelled by current controlled current sources, while the static capacitance of the transducer is modelled by capacitor C_0. If a propagation medium is to be added to the circuit, it is modelled as a second transmission line connected to either of the mechanical ports. A medium against which only a reflection is of interest, such as backing, can be modelled by a single resistor instead of a transmission line.

Analog and mixed signal design and simulation has been performed within the Cadence IC4.46 framework, using the Spectre and SpectreVerilog simulators. The digital control block was written in Verilog and synthesized with Synopsis, whereafter Silicon Ensamble was used for place and route.

3. Circuit design

The design has been performed in a 0.8 μm, 50 V CMOS technology provided by austriamicrosystems (AMS) [32]. The

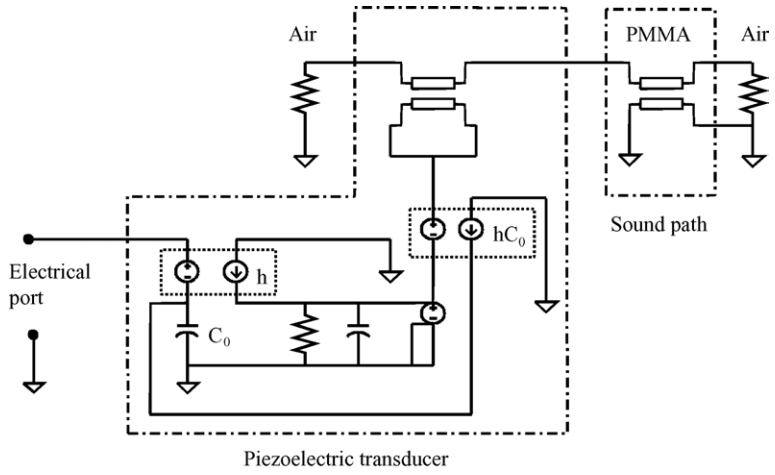

Fig. 2. Schematic model of the ultrasound system including air backed piezoelectric transducer and sound path.

process features double metal and double poly as well as high resistive poly options. A wide variety of various high voltage transistors are available. To avoid the necessity to generate gate voltages that are higher than the battery voltage, the use of thin gate oxide high voltage NMOS transistors has been preferred in the design. This limits the maximum drain–source voltage to 30 V (40 V for short time operation), but also provides transistors with shorter minimum gate length than for the mid- and thick oxide variants.

The design is based on four main blocks as shown in Fig. 3:

- *Control Block*. Controls the full functionality of the chip. Parameters are set via digital input pads.
- *Boost converter*. Used to generate high voltage on the piezoelectric transducer prior to excitation.
- *Discharge unit*. The excitation of an ultrasound pulse is generated by a rapid discharge of the transducer.
- *Amplifier*. Used to amplify the received echo in a pulse–echo system.

The operation of the chip is exemplified by the behavior of the voltage on the transducer as shown in Fig. 4. The main phases are:

- *Charge*. The transducer is charged to high voltage with the boost converter. The charging is done with several *Pump* cycles.
- *Hold*. The transducer is held at the high voltage level to let eventual echoes generated by the charging dissipate.
- *Discharge*. The transducer is rapidly discharged to generate an ultrasound pulse.
- *Wait*. Wait state to let the ultrasound pulse travel in the media.
- *Amplify*. The amplifier is powered up and amplifies the received echo.
- *Off*. System is turned off until next pulse generation.

The following subsections give more detailed descriptions of the functionality of the blocks. The general idea followed in the design of the chip has been to keep each block as simple as possible while maintaining the desired functionality. Rather than to suboptimize a single block for 10% extra performance, the effort has been to optimize on system level and to get the design "first-time-right", i.e. functional after the first manufacturing run.

3.1. Control block

The control of the functionality of the chip is handled by a finite state machine (FSM). The FSM relates all switching

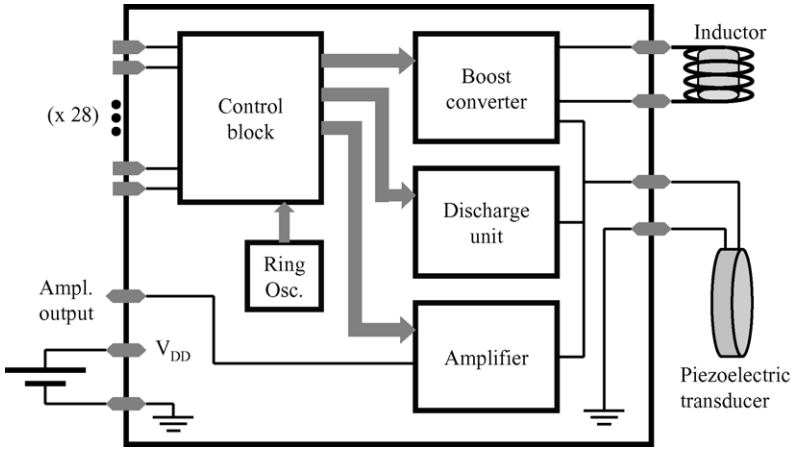

Fig. 3. Block schematic of the complete chip outlining the main blocks and external connections. Control signal inputs can be bonded directly on the chip.

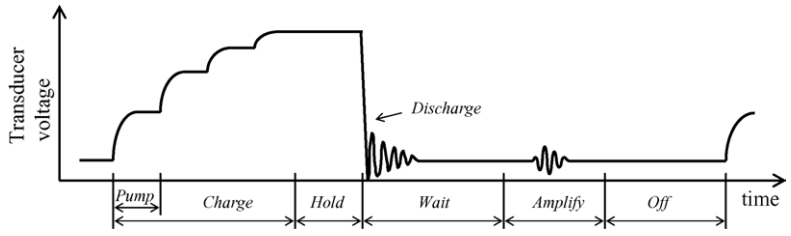

Fig. 4. Chip functionality illustrated by the behavior of the voltage on the transducer.

Table 2
Times controlled by the FSM

Parameter	Range ($\times T_{clk}$)	No. of steps
T_{pump}	1–8	4
T_{charge}	1–513	8
T_{hold}	1–4097	4
T_{wait}	1–513	8
$T_{amplify}$	9–1025	4
T_{off}	17–16385	4

activity to its input clock signal with a frequency $f_{clk} = 1/T_{clk}$. The core of the FSM is a 20-bit counter. The output signals of the FSM controls the complete operation cycle of the chip. A wide range of settings was desired to be able to test the chip with a variety of load and operating conditions. The times controlled by the FSM are indicated in Fig. 4, with the range of settings shown in Table 2.

The settings of the parameters are made through parallel digital input pads. The layout of the chip is performed to allow the settings to be made with on-chip bond wires to power supply or ground provided as bond pads. Pads with internal pull up and pull down have been used to achieve a default state of operation for the FSM without the need for bonding, to facilitate ease of testing. The chip can also be set in manual mode whereafter the control signals are set externally. The parallel digital input pads will be omitted for future generations of the chip, and replaced with a serial programming interface.

The input clock signal to the FSM is delivered by the on-chip ring oscillator, which uses a selectable number of three or nine slow inverters to generate the clock signal. The nominal frequency for the oscillator is $f_{clk} = 1.19$ MHz in the high frequency setting. The clock signal can also be provided from an external generator through a digital input pad for test purposes.

The FSM was synthesized using standard cell libraries available in the used process. To save power a dedicated low power library with weaker drive capacity in the gates was used. This presents no problem as the clock frequency of the FSM is relatively low.

3.2. Inductive boost converter

A simplified schematic of the inductive converter together with possible off-chip connections are shown in Fig. 5. Pumping is performed with the high voltage transistor M9. During the pumping sequence transistor M7 is on and transistor M8 is off. When the pumping cycle is complete, *charge_n* is pulled high so that M8 grounds the supply side of the inductor. This is necessary as a current would otherwise be built up in the inductor during the discharge of the piezoelectric transducer connected to the output of the pump. M7 and M8 are driven with unbalanced inverter chains to ensure that they are never carrying a short circuit current during switching.

The pump is intended to be used together with an external SMD inductor. With the target capacitance C_0^K in the range of 0.2–10 nF a design target for the inductor was set to 100 μH. This gives a resonance frequency of $L_{pump}C_0^K$ ranging from 0.16 MHz to 1.1 MHz. The transfer of energy from the inductor to the capacitive load is performed during a quarter of a period, i.e. within times ranging from 0.23 to 1.6 μs. This corresponds well to the available settings for T_{pump} discussed in the previous section. The chosen inductor has a series resistance R_L of 10 Ω. The self resonance frequency is 10 MHz, corresponding to a parallel capacitance C_L of 2.5 pF.

A large part of the energy loss in the pump is due to the on-resistances in transistors M7 and M9. Wider transistors give lower on-resistance and lower loss. At the same time, the

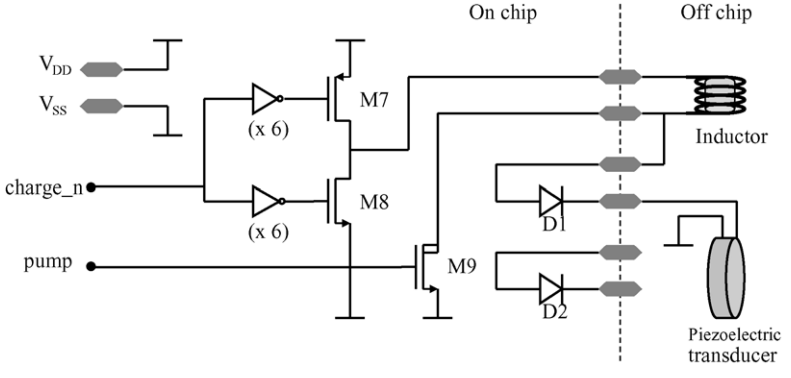

Fig. 5. Simplified schematic of the inductive boost converter. External connections to inductor and transducer are indicated in the figure.

consumed chip area and capacitive loss during switching increases. Both transistors are here scaled to have an on-resistance in the order of 2 Ω, to keep the total transistor on-resistance below the value of the series resistance in the inductor.

One diode is needed to achieve the desired functionality. Although not available as standard components in the libraries, two on-chip diodes were implemented in an effort to minimize the number of external components. One uses the parasitic diode formed between drain and substrate in a high voltage NMOS transistor, while the other is custom made using n and p-doped areas (DNTUP, PTUB). Connections to the diodes are done off-chip to enable the use of an external diode if necessary.

3.3. Discharge unit

The fall time of the discharging of the crystal is important to get maximum amplitude from the ultrasound pulse. The choice of a large discharge transistor can decrease the time and give a higher output amplitude. On the other hand, this consumes chip area and increases the load on the preceding transistor stage as well as on the crystal [9]. Simulations of a piezoelectric transducer driven by a pulse source showed that a fall time t_{dis} of 1/10 of the crystal resonance frequency period time T_{osc} gives maximum pulse amplitude from the crystal while avoiding to use faster transitions than necessary. The relation:

$$C_0^S U_{dis} = W I_{sat/\mu m} t_{dis} \quad (6)$$

can be used get a first estimate of resulting fall time or required transistor width for a given crystal. Here, U_{dis} is the discharge voltage, $I_{sat/\mu m}$ the saturation current per μm of the discharge transistor and W is its width in μm. The use of the clamped capacitance of the transducer is motivated by the fact that the frequency content of the discharge pulse has a high content of harmonics above the resonance frequency of the crystal. After the discharge, the discharge transistor has to be turned off immediately to let the crystal oscillate freely at its resonance frequency.

The discharge unit is divided into five equivalent blocks, one of which is shown in Fig. 6. The division into blocks makes it possible to adjust the used discharge transistor size to the connected load. The main component in the block is the 12000/3 μm discharge transistor M1. The used type is the NMOSTH, which is a high voltage thin oxide n-channel transistor. At a gate voltage of 3.6 V, the transistor achieves a peak current of about 1 A. The gate capacitance presented by M1 is large, and care has been taken to use appropriate transistor scaling to drive the gate. Care has also been taken during the layout process to ensure that the maximum allowed current densities in all layers of the chip are not exceeded during the discharge of the transducer.

A discharge is initiated by a high level on the *pulse* input, which propagates through the AND gate A1 to the buffers and to the discharge transistor M1 which starts to discharge the node *out*. The task of the discharge control is to turn the discharge transistor M1 off immediately when the *out* node has been discharged, to avoid holding the transducer clamped to ground level. A key component to achieve this is the controllable level shifter M2/M3 which transforms the high voltage on the *out* node to a level appropriate for the low voltage CMOS logic. The gate node of the inverter M4/M5 will hold a value of $V_{DD} - V_{GSM3}$ as long as the *out* node remains over approximately $V_{DD} - V_{GSM3} + V_{DS,satM3}$. To avoid discharge of the *out* node during charge and hold, the level shifter is turned on only when a discharge is initiated.

When the out node has been discharged to a level approaching $V_{DD} - V_{GSM3}$, the gate node of M4/M5 starts to drop as it is pulled down by M2 when M3 turns off. The inverter M4/M5 switches and pulls the clock input of the D flip-flop high. This turns off the discharge transistor through the AND gate A1, as well as the sense circuit through AND gate A2. Before a new discharge cycle can be performed the D flip-flop has to be reset through *reset*.

The control block as well as the buffer inverters for M1 has been designed with low voltage transistors and logic, except for the transistor M3. This is subject to a high voltage at the

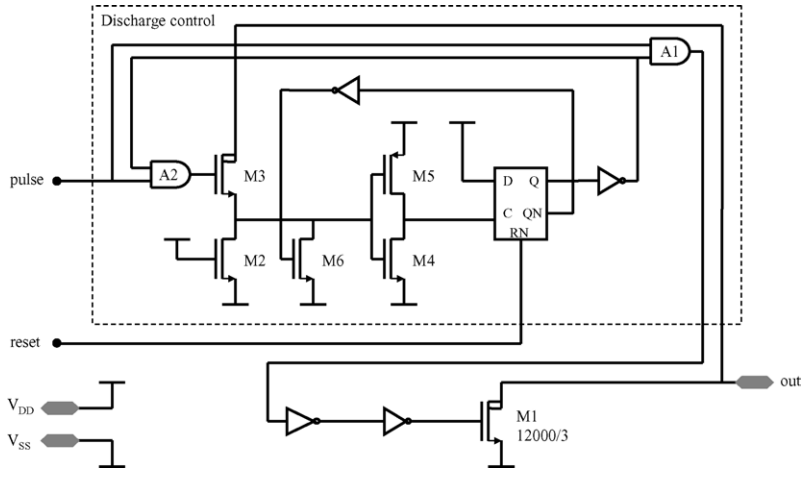

Fig. 6. Simplified schematic of one discharge block.

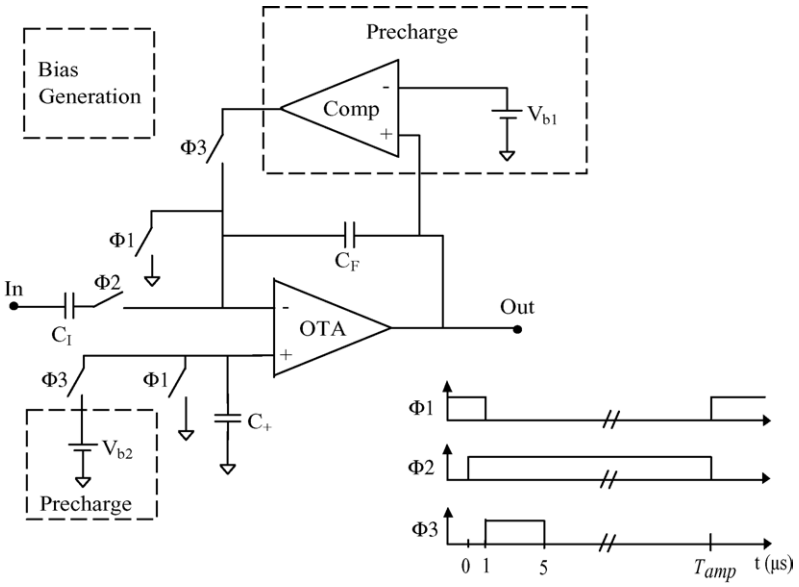

Fig. 7. Block schematic of the amplifier. Switch timing is indicated in the diagram.

drain which is connected to the transducer, thus a high voltage transistor has been used.

3.4. Amplifier

This section gives a block level description of the amplifier. Detailed circuit solutions can be found in [33]. The amplifier is based on three blocks as shown in Fig. 7: an operational transconductance amplifier (OTA), bias generation, and precharge generation.

The amplifier is centered around the OTA, which is a standard two stage CMOS Miller design [34] with transisitor/capacitor pole-zero compensation between the stages. Switch transistors are inserted in series with the current sources in the structure to allow the OTA to be turned on and off as desired. The OTA will always be used in a fixed feedback configuration within the amplifier, thus there is no requirement for unity gain stability. During the design of the OTA, it was noted that the cost in terms of power consumption to meet the design target for noise would be high. The decision was then taken to stay with a fairly low power consumption instead of trying to optimize the noise level.

As the amplifier is used intermittently and built around capacitive feedback, all operating points need to be set at each start up. This is achieved by the precharge block, which is based on a comparator that is connected in the feedback loop during the start up phase of the amplifier. The precharge block also contains two voltage bias points. V_{b1} sets the reference of the comparator to approximately half the supply voltage, yielding an output voltage of the amplifier at the same value after complete start up cycle. The comparator feedback also compensates eventual input related offset in the OTA. V_{b2} is used to set the positive input of the OTA to a suitable bias point during the start up phase. Bias current for the OTA and the startup block is provided by the bias generation block. This is also a standard design [35], which has been extended with a switch transistor to enable power off. The reference current generated is 20 μA, which is scaled in the target blocks.

The switching sequence for the amplifier is indicated by the diagram in Fig. 7. Main phases are the following:

- $t < 0$ μs: *Off*. Used while the piezoelectric transducer is excited and the echo is travelling in the media. Both amplifier inputs are grounded through switches Φ1. At the same time the high voltage switch Φ2 is open. This protects the negative OTA input from high voltage transients on the input, which all the time is connected to the piezoelectric transducer. Switches Φ3 are open, disconnecting the startup block.
- $0 < t < 1$ μs: *Bias*. The bias generation block is activated and switch Φ2 is closed to connect the input capacitor C_I to the negative input of the OTA, which remains grounded.
- $1 < t < 5$ μs: *Startup*. Switches Φ1 are opened and switches Φ3 are closed. The OTA and the comparator are turned on to initiate the precharging of all nodes to the desired bias point.
- $5 < t < T_{amp}$ μs: *Active*. Switches Φ3 are opened and the precharge phase discontinued. The amplifier is operational.
- $t > T_{amp}$ μs: *Off*. Switch Φ2 is opened and switches Φ3 are closed to ground the inputs of the OTA. Bias generation, OTA and comparator are turned off.

All parts in the amplifier except switch Φ2 and the input and feedback capacitors have been designed with low voltage transistors. The input capacitor and switch Φ2 have to be able to withstand the high voltage generated on the transducer. The feedback capacitor C_F is not subject to high voltage and could be designed with standard components, but it was elected to use the same type of capacitor as for C_I to achieve reasonable matching.

4. Results and discussion

A chip photograph outlining the main blocks is shown in Fig. 8. The chip area is 3.3 mm × 3.6 mm, with a major part

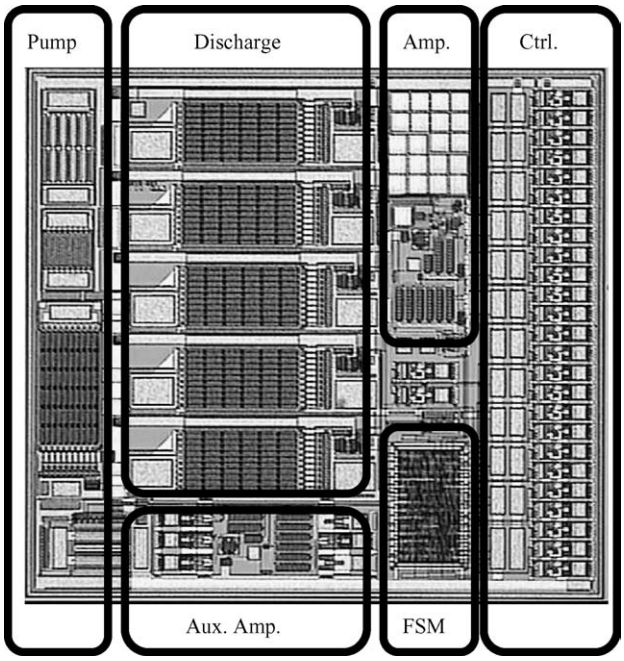

Fig. 8. Photograph of the manufactured chip. The main blocks are outlined in the figure.

occupied by the transducer discharge transistors. The following subsections describe the measurement setup and the various measurements performed on the chip.

4.1. Measurement setup

The following measurements were performed to verify the functionality of the chip:

- *Functional verification*. Recording of a complete operation cycle including pumping, discharging and amplification.
- *Amplifier performance*. The performance of the amplifier was measured and set in relation to design target.
- *Pump efficiency*. The efficiency of the charge pump was measured. A capacitor was used as a load for these measurements to get a value of the pump efficiency without the electromechanical coupling in a piezoelectric transducer.
- *System power consumption and efficiency*. The total system power consumption was measured for both capacitive and piezoelectric loads.

Measurements were performed with the chip bonded directly to a test circuit board. Power was supplied by a Keithley 2400 series Sourcemeter set at 3.6 V. Tests were made using both a capacitor and piezoelectric transducers as the target for the system. The capacitor was used as it allows a more precise judgement of the system power consumption related to the capacitive load than the piezoelectric transducer does. When a piezoelectric transducer was used this was connected to the board using 20 cm long micro coaxial cabling. This allowed the transducer to be mounted on a plexiglas (PMMA) backing and immersed in water to achieve a pulse–echo system. The front side of the transducer together with electrical connections was covered with one layer of PC-52 protective lacquer to allow immersion in water.

The voltage at the transducer and the amplified received echo were measured with a Tektronix TDS7254 oscilloscope, using a low load active probe ($C_p < 2$ pF, $R_p = 1$ MΩ) for the measurement at the amplifier output. The power consumption of the pump cycle and the amplifier were measured differentially with active probes over a 1.2 Ω resistor in series with the power supply, while the mean power consumption was measured directly with the Sourcemeter.

The Keithley 2400 Sourcemeter measures current and voltage with accuracies of about 10 nA and 2 mV respectively. The measurement error for mean power consumption is thus estimated to less than 0.1%. The standard deviation in the measurements is low (<0.3%) for the measurements performed with high pulse repetition frequency, but noticeably higher (∼6%) for 10 measurements at 70 Hz repetition rate. The power consumption for the pump and amplifier as measured over the reference resistor include larger uncertainties. The resistor value has an accuracy of 1%. With offset errors calibrated, a gain error of 2% and the uncertainty due to limited resolution (8 bits) remain in the oscilloscope. The measured voltage amplitudes are low level (mV), and overlaid on a non stable dc base. The unstable environment yields a standard deviation which has been estimated to less than 4% for 10 measurements.

Measurements were performed using capacitors of 1.0 and 4.6 nF, and with 4 MHz piezoelectric transducers with diameters 6.5, 10 and 12 mm. Although, several parameters are possible to vary in the system, most of them have been kept constant in these measurements. The amplifier on time T_{amp} which is one of the decisive factors for the power consumption has been set to 120 μs throughout the measurements. The loads and setting used for the measurements presented below are but a few of the many possible in the system. It should thus be expected to see efficiencies and power consumption for various parts of the system vary when different settings are used. The complete interdependence between settings of the FSM, load values, and efficiency is subject for further investigation.

4.2. A complete cycle

A complete transmit and receive cycle is shown in Fig. 9, where the voltage at the transducer and the amplifier output are plotted to the same scale. The amplifier is active to amplify the second incoming echo in a pulse–echo system. Expanded views of the excitation and the amplified echo are shown in Figs. 10 and 11, respectively. Even though the transducer was covered with protective lacquer, leakage was observed for high voltages when it was immersed in water. This will not be present for a complete sensor where the transducer is cast in surrounding material.

In Fig. 10 it is seen that the transducer is properly released as the voltage approaches zero, whereafter it oscillates at its resonance frequency of about 4 MHz. It is also seen that the transducer produces oscillations at a frequency more than 1 decade lower than 4 MHz. These are caused by radial and flexural modes in the transducer that are excited simultaneously as the wanted

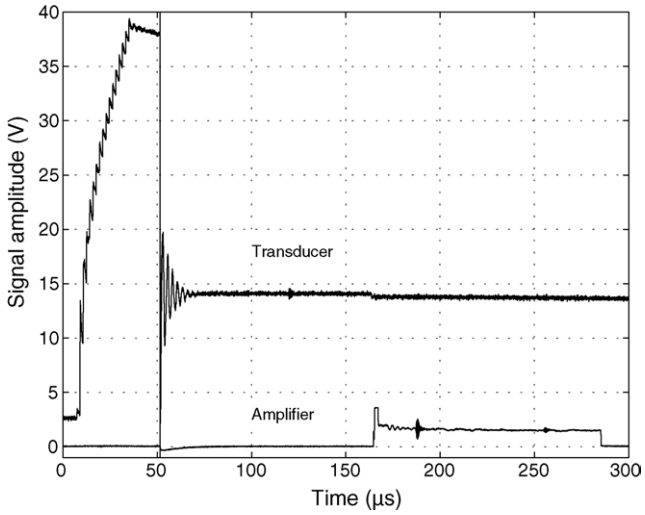

Fig. 9. Measured transducer and amplifier output voltages for a complete transmit and receive cycle.

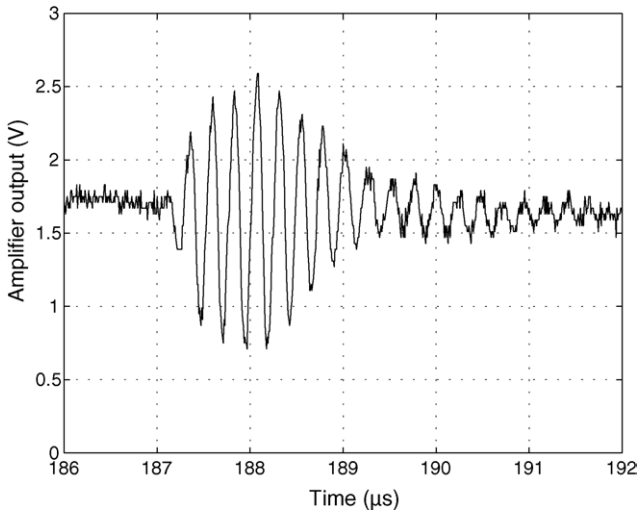

Fig. 11. Close up of the measured received echo signal after amplification.

longitudinal mode [12]. With the transducer integrated in a complete sensor with correct backing and matching layers these modes would be reduced. Another source for non-wanted oscillations in the received signal are the acoustic output produced during pumping. To reduce this, the wait time before excitation need to be increased in an application.

Another phenomenon is the reminiscent voltage of about 14 V at the transducer when the ringing has settled. This is equivalent to a remaining electrical energy of about 14% compared to the initial energy at a voltage of 38 V. A possible cause of this behavior can be found in the coupling between mechanical and electrical properties for the piezoelectric material [36]. Although a complete solution would require the solution of the differential equations that describe the momentary behavior of the system, a phenomenological explanation can be given.

The electrical displacement D in the material is coupled to both the applied electrical field E and to the strain S through the relation:

$$D = \varepsilon^{S} E + eS. \tag{7}$$

Here, $\varepsilon^{S} = \varepsilon_0 K^{S}$ is the permittivity for the free transducer, and e is the piezoelectric coupling constant. Further, as the piezoelectric material does not contain free charges, the displacement is directly linked to the surface charge density σ_s, i.e.:

$$D = \sigma_s. \tag{8}$$

As the discharge is initiated, charge is removed from the surface of the piezoelectric transducer, thus lowering the electrical field. Simultaneously, both mechanical stress and strain are developed in the transducer. When the electrical field reaches zero, this is a combined effect of reduced D and mechanical influence. Thus, when the crystal is electrically released, there may well be a remaining D field in the material, even though $E = 0$. Thus, there is charge "trapped" on the surfaces of the transducer, and when the mechanical ringing has settled this manifests itself as a reminiscent E field.

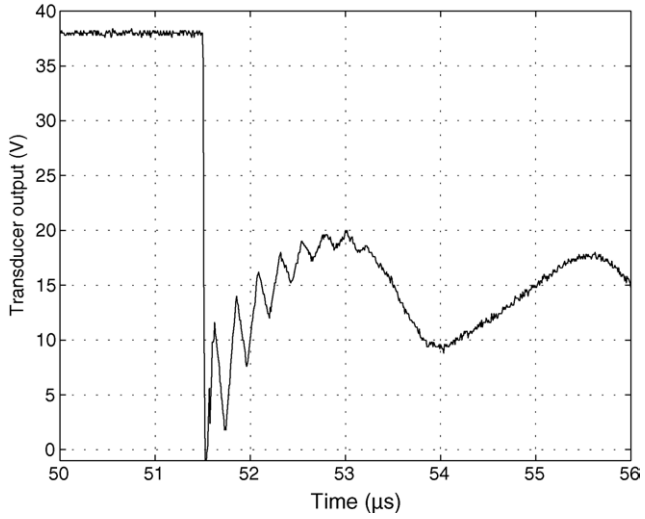

Fig. 10. Close up of the measured transducer voltage during excitation.

4.3. Amplifier performance

Measured performance of the amplifier are presented in Table 1 together with the design targets. The amplifier meets the design targets except for the input equivalent noise, as discussed in Section 3.4.

4.4. Pump efficiency

Initial measurements of the pump efficiency gave very disappointing results in the order of 10%. The cause was traced to the use of the on-chip parasitic diodes. When conducting in forward direction, these form parasitic bipolar transistors to the substrate of the circuit, which shunt the charge current away from the load capacitance. Thus, for the remainder of the measurements an external 1N4148 switch diode was used to overcome this problem.

Table 3
Power consumption of the system for various repetition rates and load conditions

$\varnothing_{\text{transducer}}$ (mm)	6.5	10	12
C_0^S (nF)	0.55	1.30	1.88
U_{exc} (V)	40.5	35.8	31.4
f_{rep} (Hz)	70, 1385, 3430	69, 1335, 3130	69, 1335, 3130
P_{meas} (mW)	0.21, 2.48, 6.06	0.27, 3.56, 8.44	0.29, 3.67, 8.46
P_{min} (mW)	0.063, 1.25, 3.10	0.12, 2.23, 5.23	0.13, 2.47, 5.80

With the external diode, the pump efficiency was measured to 80% for a 1 nF load capacitor charged to 36 V, and to 75% for a 4.6 nF load capacitor charged to 33 V.

4.5. System power consumption

The power consumption for the system excluding digital input pads was measured for three repetition rates and three different piezoelectric transducers, as shown in Table 3. The transducers all have a center frequency of 4 MHz.

The power consumption of a clamped piezoelectric transducer that is excited at a repetition frequency f_{rep} with single shot excitation pulses from a fixed voltage source can be calculated as

$$P_{\text{min}} = f_{\text{rep}} C_0^S U_{\text{exc}}^2, \tag{9}$$

where U_{exc} is the excitation voltage. The use of the clamped capacitance value C_0^S shows that the calculation only takes into consideration the pure electrical capacitance of the transducer [13]. As soon as the transducer is free to move, electrical energy will be converted to mechanical and the effective capacitance value as well as the power consumption will increase. The value of P_{min} can thus be used as a benchmark for the minimum achievable power consumption of an ultrasound system using single pulse excitation. Calculated values of P_{min} are included in the table for the different transducers and excitation frequencies.

The measured power consumption P_{meas} includes the system with digital logic and clock generator, boost pump, excitation, and amplifier operation. It can be seen that P_{meas} comes within a factor of 2 from the minimum achievable for the transducers in all cases at the high repetition frequencies. A reduction in repetition frequency increases the impact of the power consumption of the digital logic and clock generator, which was measured to $P_{\text{digital}} = 90\,\mu\text{W}$. Future generations of the chip will use processes with smaller feature sizes, making it possible to further reduce this number and further reduce the power consumption for low repetition rates.

5. Conclusions and further work

This paper has presented the design of a complete autonomous transmit and receive ASIC for pulse–echo piezoelectric sensors. The on-chip boost converter together with the on-chip amplifier provides the possibility to achieve a high dynamic range, e.g. increased penetration depth, in a battery operated ultrasound measurement system. The excitation voltage can be adjusted to the requirements in the system, i.e. in a low loss system a lower excitation voltage can be used to decrease the power consumption. Intermittent operation of the included amplifier further decreases the power consumption.

Measurements have been performed on the individual parts as well as on the complete system. The efficiency of the boost pump reaches 80% when a discrete switch diode is used. The total power consumption including excitation, amplification and operation of the digital logic has been measured for various pulse repetition frequencies.

The results show that it is possible to reach a power consumption within a factor of 2 from the minimum power required to charge the transducer alone from a fixed voltage source. This clearly shows that the presented design strategy can be applied to reach extremely low power consumption in a battery operated pulse–echo ultrasound sensor. The power consumption at a repetition frequency of 70 Hz reaches 210 μW, which enables an operating time of several years from one single lithium battery.

This work is part of an ongoing research towards a complete thumb size ultrasound measurement system with wireless communication. The next generation of the chip will include a wider range of signal conditioning, such as A/D converter, time-of flight measurement, and pulse energy estimation.

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Jonny Johansson received the MSc in electrical engineering from Chalmers University of Technology in 1992. He thereafter joined Asea Brown Boveri in Ludvika, Sweden, where he worked with development of high voltage measurement systems. In 1999, he joined EISLAB at Luleå University of Technology where he was awarded his PhD degree in 2004. He is currently working as researcher at EISLAB with his major research interest beeing low power mixed mode design for sensor systems.

Martin Gustafsson received the MSc degree in electrical engineering from Chalmers University of Technology in 2003. He is currently enrolled as a PhD student at Luleå University of Technology. His research interest is in the field of mixed mode circuits for sensor front-ends.

Jerker Delsing received the MSc in engineering physics at Lund Institute of Technology, Sweden in 1982. In 1985, he received the degree of Licentiate in Technology and in 1988 the PhD degree, both in electrical measurement at the Lund Institute of Technology. During 1985–1988, he also worked half time at Alfa-Laval, SattControl with development of sensors and measurement technology. Over the years 1989–1995, he was at the Department of Heat and Power Engineering at the Lund Institute of Technology where he got the docent degree in 1994. In 1995, he was appointed professor in Industrial Electronics at Luleå University of Technology where he currently is working as head of EISLAB division and dean of engineering faculty. Major research interest is measurement technology, electronics and EMC targeting embedded internet sensors