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Ultra low-resistance palladium silicide Ohmic contacts to lightly doped n-InGaAs

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The formation of shallow, ultra-low resistance, Pd/Si solid-phase regrowth (SPR) ohmic contacts to n − $In_{0.53}Ga_{0.47}As$ epilayers of $N_D = 1 \times 10^{17}$ cm^{-3} and $N_D = 3 \times 10^{19}$ cm^{-3} is demonstrated. The resulting specific contact resistances of 9×10^{-8} $\Omega\,cm^2$ and 1.8×10^{-8} $\Omega\,cm^2$, respectively, are the lowest demonstrated for SPR contacts to n-InGaAs. An optimum Pd/Si atomic ratio of 1.5 is found to be essential to achieving low specific contact resistance. A low-temperature, two-step, rapid thermal annealing process has been employed to activate the InGaAs regrowth process and consistently achieve shallow contacts with minimal lateral diffusion. Transmission electron microscopy is used to substantiate the SPR mechanism of contact formation. For lightly doped epilayers, I-V-T measurements from 77–300 K show that the ohmic behavior is a direct result of the SPR process due to the introduction of excess Si dopant greater than 10^{19} cm^{-3} at the regrown InGaAs interface. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4748178]

I. INTRODUCTION

Ohmic contacts are an important building block of electronic devices such as heterojunction bipular and high electron mobility transistors. High quality ohmic contacts serve to both reduce parasitic resistance in the device and improve its frequency response characteristics. As feature sizes are slated to reach the 10-nm barrier by the middle of this decade, ohmic contacts with ultra-low specific contact resistance are required to compensate for shrinking contact area.[1] Because high mobility III–V semiconductors such as InGaAs and InAs are of increasing interest for the development of high-speed devices, improving and studying ohmic contacts to these materials is of great necessity.[2]

Ohmic contacts to III–V materials are often formed by heavily doping the semiconductor to allow for current transport by field emission. However, these semiconductors often not doped to the required extent as grown. To alleviate this, further dopants may be introduced by interactions with the metallization. Solid phase regrowth (SPR) contacts have been demonstrated as effective alternatives to liquid phase regrowth contacts. SPR contacts were first demonstrated by Marshall and expanded upon by Sands, Wang, and Lau, among others.[3–8] In these contacts, the contacting metal layer (usually Ni or Pd) reacts deeply with the underlying semiconductor at a fairly low temperature, forming a ternary or quaternary phase, depending on the semiconductor. At a higher temperature, this phase becomes unstable and decomposes. Palladium or nickel, some originating from the decomposing ternary or quaternary, reacts with an adjacent group IV material (usually Si or Ge) to form a stable alloy in contact with the semiconductor.[6,9] This consumption of the reacting metal causes the regrowth of semiconductor. During this regrowth, excess germanium or silicon can act as n-type dopant to heavily dope the semiconductor. For germanide contacts on gallium arsenide, a very thin epitaxial elemental germanium layer also forms. This process is shown graphically on InGaAs in Figure 1. SPR contacts have a significantly more uniform interface morphology compared to alloyed contacts. Kim *et al*. have performed some of the most recent work on SPR contacts, demonstrating specific contact resistance values as low as 1.1×10^{-6} $\Omega\,cm^2$ for a Pd/Ge SPR contact, and 3.7×10^{-7} $\Omega\,cm^2$ using a Pd/Si contact assumed to form through the SPR mechanism, both on 10^{19} cm^{-3}-doped Si : $In_{0.5}Ga_{0.5}As$.[10,11]

Significant work on non-SPR contacts to heavily doped n-InGaAs has already been performed with very good results.[12–14] However, one of the key advantages of the SPR process is its ability to incorporate dopants into an otherwise lightly or undoped layer. For example, high electron mobility structures often have undoped barrier layers that must be etched through or reacted with to form a good ohmic contact,[9] or current must be transported through the barrier. Thus, it is important that SPR ohmic contacts be developed that provide very low specific contact resistance with low levels of as-grown doping. The latest study on the Pd/Si/InGaAs system by Kim states that the SPR mechanism is expected,[11] but no study has verified this claim. Furthermore, the reported resistance was still too high for optimized device performance. In this paper, we show a significantly reduced specific contact resistance compared with all earlier studies on lightly doped InGaAs, while maintaining smooth surface morphology and minimizing voids at the metal-semiconductor contact interface, both of which are important for scaled devices. To our best knowledge, the minimum specific contact resistance presented is a new record for SPR-based contacts on any substrate.[15] We also corroborate the SPR mechanism for palladium silicide contacts on

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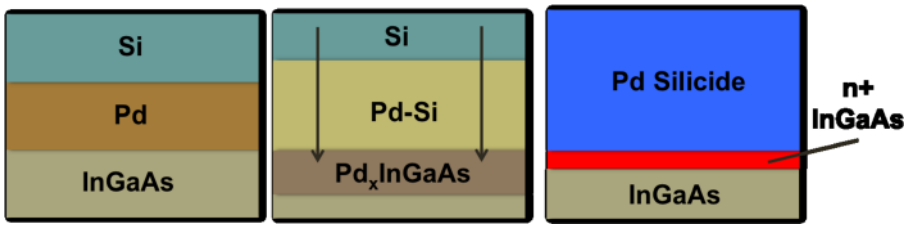

FIG. 1. Schematic of the SPR process on InGaAs.

n-InGaAs using transmission electron microscopy and electrical characterization and estimate the concentration of dopants introduced.

II. EXPERIMENTAL

Epilayers of lightly doped (1×10^{17} cm^{-3}) and heavily doped (3×10^{19} cm^{-3}) Si : $In_{0.53}Ga_{0.47}$ As epilayers with thicknesses of 250 nm and 50 nm, respectively, grown on semi-insulating InP, were used for this study. Both of these epilayers were grown using metal-organic vapor phase epitaxy. The sheet resistance extracted from contact resistance measurements for the lightly doped samples was 336 ± 19 $\Omega/\square$ and for heavily doped samples was 27.2 ± 0.3 $\Omega/\square$. I-V measurements were performed on both types of samples. Lightly doped samples were defined with circular transfer length method (CTLM) patterns, with nominal gap spacings of 0.5–20 μm. Alternatively, heavily doped samples were defined with refined TLM method (RTLM) patterns, with nominal gap spacings of 0.6–10 μm. These structures are shown graphically in Figure 2.

For our contacts, the sheet resistance of the gold layer, in which the majority of current flows, is 0.27 $\Omega/\square$, on the order of 1% of the heavily doped semiconductor sheet resistance. This resistance could introduce noticeable error and must be controlled for. The standard TLM model treats the ohmic contacts as isopotentials, which is valid for high sheet resistance underlying semiconductor but not for a low sheet resistance epilayer. RTLM structures, as used by Dormaier, are employed in this paper to reduce these errors. [14]

Current probes are placed far away from the gap and associated voltage probes to allow for parallel isopotentials across the contact gap. The design of the RTLM test structure ensures that the extracted specific contact resistance measured is not below the actual value due to an artifact from the metal sheet resistance, although due to the small resistive contribution of the metal between the contact front and the voltage probe extension pads (placed for convenience) the measured value may be slightly higher than the real value.

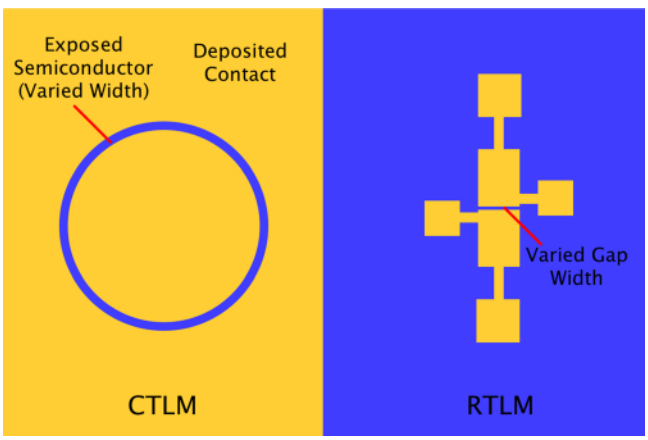

FIG. 2. Comparison of CTLM and RTLM structures.

The substrates were degreased in acetone, isopropanol, and deionized (DI) water in an ultrasonicator for 1 min each and dried with compressed nitrogen. Immediately before photolithography, all samples were dehydration baked for at least 1 min at a temperature exceeding 100 °C. CTLM and RTLM structures were defined using a standard dual-layer NANO SF9/SPR3012 resist stack followed by optical exposure in a GCA 8000 i-Line Stepper, and development with CD-26 (tetramethylammoniumhydroxide/TMAH), deep UV flood exposure, and second stage development using PMGI 101 A developer.

After lithographic definition, all samples were surface treated using UV ozone with a 80% nitrogen/20% oxygen mixture for 10 min at 0.9 SLPM to remove organic contaminants and grow a uniform oxide layer on the surface of the substrate.[16] After UV ozone treatment, the oxide was etched in a 10:1 buffered oxide etch (BOE) solution for 2 min and immediately loaded into an electron beam deposition chamber. A base pressure below 3×10^{-7} Torr was reached before beginning metal deposition. A titanium getter was performed to reduce oxygen content in the chamber even further. The ohmic contact stack (Pd/Si/Pd/Ti/Au) was then deposited with thicknesses and deposition rates listed in Tables I and II. After contact deposition and liftoff, RLTM mesas were defined and the surrounding InGaAs was wet etched using a solution of lactic, phosphoric, and citric acid with hydrogen peroxide (6 ml:1ml:1g:1 ml).

Samples were then annealed in an AG Associates Heatpulse 610 rapid thermal annealing furnace in argon atmosphere to form the ohmic contact. All samples, except those fabricated to study the first annealing step only, were annealed using two distinct steps. All samples were annealed with a silicon cover wafer to maintain an overpressure of arsenic to prevent vapor loss of arsenic from the semiconductor.

TABLE I. Deposited metal layers and deposition conditions.

Metal type (first to last)	Deposition rate (Å/s)
Palladium	1
Silicon	1.5
Palladium	1
Titanium	2
Gold	1.3

TABLE II. Contact structure thicknesses, atomic ratios between Pd and Si layers, and notes.

Metal thicknesses (nm)	Pd/Si ratio	Notes
15,27.5,15,40,90	1.49	Optimized ratio, minimized thicknesses
30,45–70,30,40,90	1.17–1.82	Various Pd thicknesses to find best ratio
30,70,30,30,90	1.17	Un-optimized ratio, thin diffusion barrier (failed)

After annealing, electrical characterization was carried out using a Keithley 238 four point microprobe station, sweeping current and measuring voltage. Absolute resistance values for each CTLM/RTLM gap are calculated from the unweighted mean of measured resistances from −0.6 mA to +0.6 mA. For each sample, four or more distinct sets of RTLM or CTLM patterns were measured. All figures in this paper show error bars equal to the standard deviation of the measurements between these four sets. No outlier data were discarded for the purposes of calculating these error bars. Gap spacing (CTLM and RTLM) and mesa widths (RTLM) were measured using SEM. All measurements were calibrated at the same working distance using an MRS-3 magnification reference standard from Geller Microanalytical Laboratories.

The TLM model assumes the sheet resistance under the contact is equal to the sheet resistance between the contacts. While this assumption is not strictly true when considering SPR contacts, Wang *et al*. have previously explored the use of multiple tests structures for extracting electrical properties from SPR contacts to GaAs.[17] His findings indicated that for specific contact resistances slightly higher than those reported in this paper, the extracted values of sheet resistance under the contact between the TLM structure and end resistance measurements were negligibly different. Thus, the TLM model is employed with such assumptions in this report.

After electrical characterization was completed, selected samples were examined by cross-sectional transmission electron microscopy. All samples were first sputter-coated with a 100 nm protective layer of tantalum. An FEI Quanta 200 3D dual beam focused ion beam was used to deposit additional protective layers of platinum and to lift-out and thin cross-sections from specific sites located adjacent to gap/metal-semiconductor contact edges. Transmission electron microscopy was primarily performed on a JEOL 2010 F field emission microscope, with additional images taken on JEOL 2010 LaB_6 and Philips EM420T microscopes. Bright field (BF) and high angle annular dark field (HAADF) STEM images were taken as needed. Additionally, selected area electron diffraction (SAED) and fast Fourier transform (FFT) images were acquired to provide phase information, and electron dispersive spectroscopy (EDS) was performed to assess elemental composition.

I-V-T measurements were performed using a Lakeshore (cryogenic) probe station from 77 K to 300 K. These measurements were used to determine the estimated level of doping introduced by SPR and the current transport mechanism.

III. RESULTS AND DISCUSSION

The variation of specific contact resistance as a function of annealing times and temperatures is shown in Figures 3 and 4. Second step annealing times were varied between 15 and 50 s, and second step annealing temperatures were varied between 360 and 400 °C. The first-step annealing time and temperature were kept constant at 30 s and 200 °C. The final two-step annealing parameters chosen for further study were 30 s at 200 °C, and 40 s between 380 and 400 °C. Finally, an increased layer thickness of Ti of 40 nm was chosen due to slight diffusion barrier failure at the smaller thickness.

As-deposited contacts were non-ohmic, possibly in part due to a thick semiconducting silicon layer in the contact, as shown in the XTEM image in Figure 5. After the first-step anneal, as shown in the XTEM images in Figure 6, specific

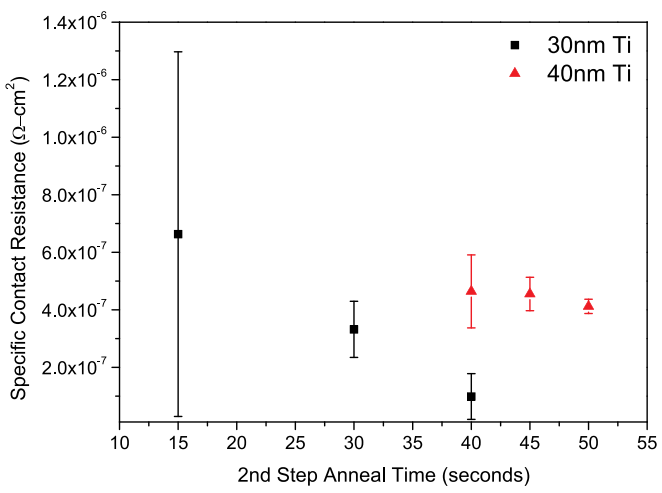

FIG. 3. Specific contact resistance data with varying second step annealing times (380 °C) and diffusion barrier thicknesses.

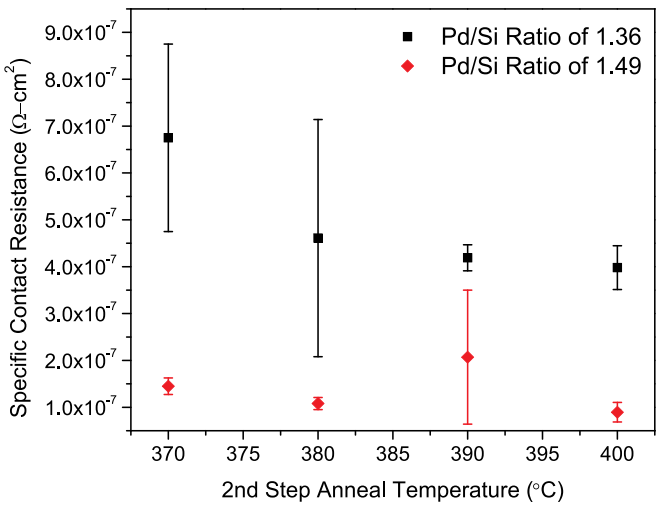

FIG. 4. Specific contact resistance data for varying second step annealing temperatures (40 s time) and Pd/Si ratios.

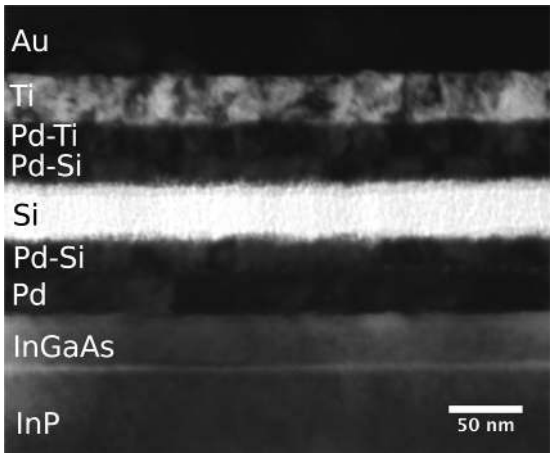

FIG. 5. Bright field XTEM of as-deposited contact.

contact resistance was still high, on the order of 10^{-4} Ω-cm^2 even on heavily doped epilayers. This finding is consistent with the SPR process, as regrowth does not readily occur at such low temperatures as in the first step anneal. Additionally, the existence of an amorphous Si layer is still present, as confirmed by the SAED pattern (inset in Figure 6(a)). As expected after the first-step anneal in the SPR process, Figure 6 also confirms the formation of a thick interface layer that has reacted to an approximate depth of 23 nm into the InGaAs. This layer is formed due to the low-temperature reaction of Pd and InGaAs, and it is attributed to being the hexagonal $Pd_4In_{0.53}Ga_{0.47}As$ quaternary phase, as identified by Ressel.[18] Additionally, small Kirkendall voids can be observed in the Pd above the reacted quartenary layer in Figure 6(b) due to the rapid diffusion of the Pd into the InGaAs at this temperature.

After the second-step anneals at 370 °C, 380 °C, or 400 °C, the thick quaternary phase has decomposed and the formation of Pd_2Si (with calculated lattice constants of $a \approx 6.55$ Å and $c \approx 3.42$ Å) in the adjacent contact layer is confirmed via TEM analysis. Representative XTEM images for the second-step anneals are shown for the 380 °C case in Figure 7. The resultant Pd_2Si layer is quite dense. The HAADF STEM image from Figure 7(b) at the metal-semiconductor gap edge makes it clear to see that the Pd_2Si protrudes shallowly into the final epilayer, only up to 7 nm, with no observable lateral reaction occurring. This feature makes the Pd/Si SPR contact suitable for very densely packed, thin body devices.

Additional XTEM images for the second-step anneals at 370 °C (not shown) and 400 °C (Figure 8) substantiate the final step of the SPR process and the formation of low-resistance ohmic contacts. XTEM from all three second-step anneal temperatures indicate the formation of a thick but shallowly penetrating Pd_2Si layer adjacent to the InGaAs interface and a regrown region of InGaAs approximately 5–15 nm thick directly beneath the layer. EDS data show that the regrown region did not change detectably upon regrowth. This regrown region appears to have increased interface roughness, as can be seen in the higher temperature 400 °C anneal in Figure 8. The regrown region is expected to correspond closely to the approximate thickness of the reacted quaternary phase from the intermediate annealing step,[8] but the XTEM shows that the regrown InGaAs thickness is slightly thinner, possibly due to shorter annealing times than in the previous studies or increased solubility of As in the adjacent Pd_2Si layer at higher temperatures, which was observed by EDS in both the 380 °C and 370 °C annealed samples.

Figures 6 and 7 also indicate that the thick amorphous Si layer is no longer present and instead there is a crystalline Si-rich-Pd layer. The quaternary phase has reacted with the excess Si to form the doped, regrown InGaAs region. The changes in the XTEM images from the first to second-step anneals corroborate the regrowth mechanism and the subsequent decrease in contact resistance. The lowest ohmic contact resistance was found for the second-step anneal at 400 °C. Figure 8 shows that this contact seemed to have the most interfacial roughness compared with the lower second-step anneal temperatures. The increased roughness may in fact be contributing to the slightly lower contact resistance because of an increase in active surface area.[19]

After the annealing parameters were fixed, Pd/Si ratios were explored. Previously, a report by Hao *et al.* on Pd/Ge contacts to n-GaAs concluded that specific contact resistance varied widely as the layer thickness ratio was changed.[20] In

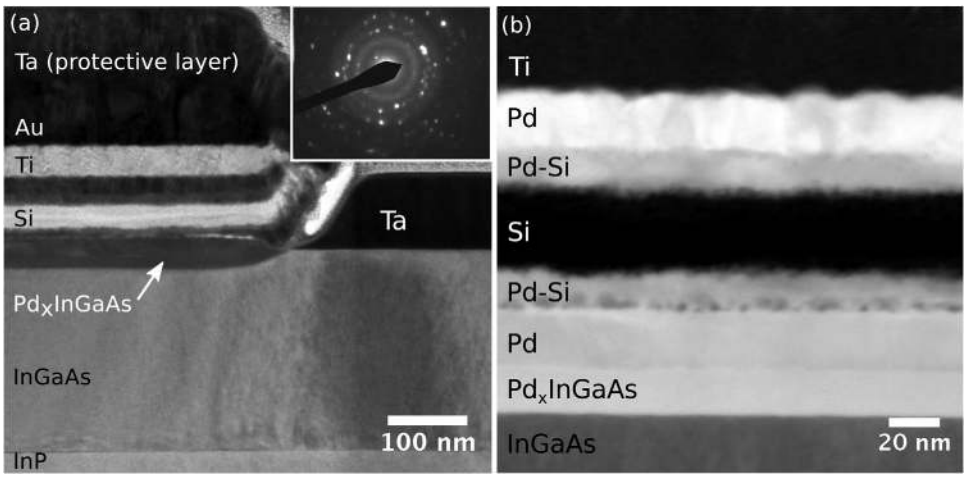

FIG. 6. (a) Bright field XTEM showing first-step anneal of contact structure (inset: SAD pattern of silicon (bright) layer); (b) HAADF STEM image.

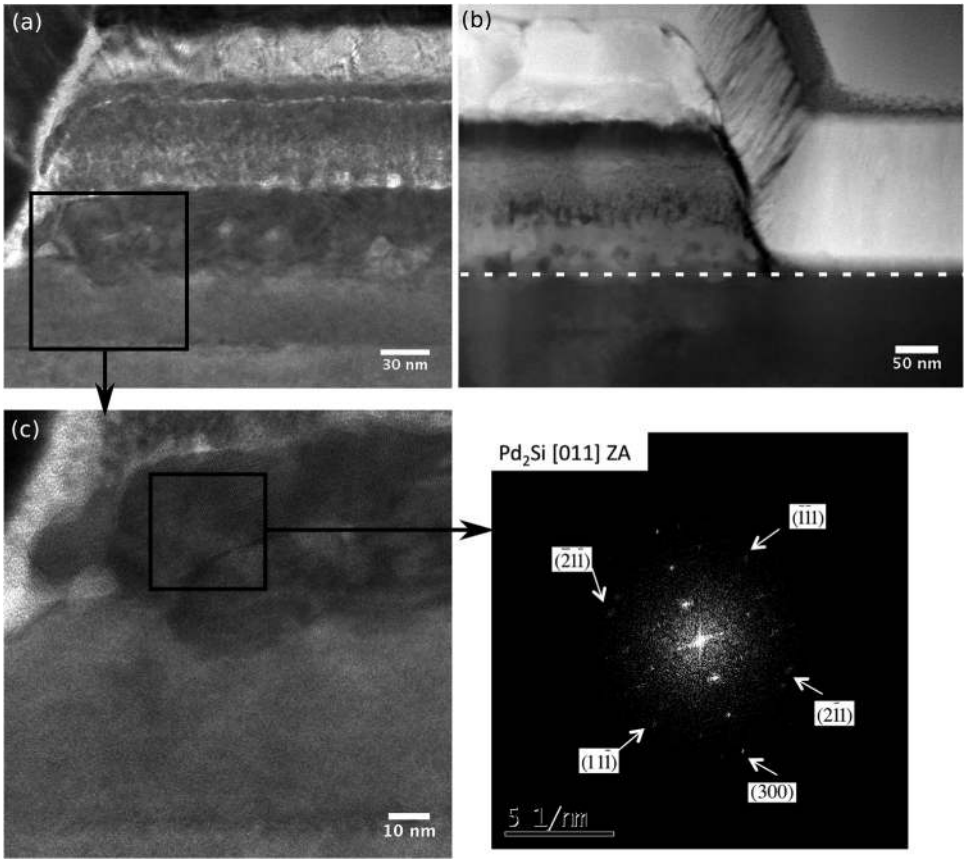

FIG. 7. (a) Bright field XTEM and (b) HAADF STEM images after 380 °C second-step anneal showing that the silicide remaining only reacts approximately 5–7 nm into the semiconductor epilayer at some points (dashed line shows original interface); (c) Pd_2Si contacting layer and FFT image.

our study, however, the ratio refers to the absolute atomic ratio between the total palladium in both the top and bottom layers with respect to the silicon layer in between. Earlier work has varied the Pd/Si ratios to some degree, but only on GaAs and not to the detailed extent presented in this study.[8]

Indeed, the Pd/Si ratio was of great importance to achieving a minimum resistivity, as shown in Figure 9. The results after second-step anneals at temperatures of 380 °C and 400 °C were similar, corresponding to an optimum Pd/Si ratio of about 1.5 for both sets. This trend compares well with the report by Hao *et al.*, in that similar optimum ratios of Pd/Ge on GaAs were observed for multiple annealing conditions (0.31–0.62 after annealing at 175 °C for 1 h and 0.44–1.03 after annealing at 340 °C for 30 min). The stable binary germanide for the Pd/Ge system on GaAs is PdGe,[5,21] as opposed to Pd_2Si for all reasonable annealing temperatures (below 800 °C),[22,23] which may explain the lower ratio observed compared to our Pd/Si contact on InGaAs. Afer optimization of the Pd/Si ratio, a minimum mean specific contact resistance of 9×10^{-8} $\Omega\,cm^2$ was achieved on the lightly doped epilayers, with a contact resistance value of 0.054 Ω mm and sheet resistance of 332 $\Omega/\square$.

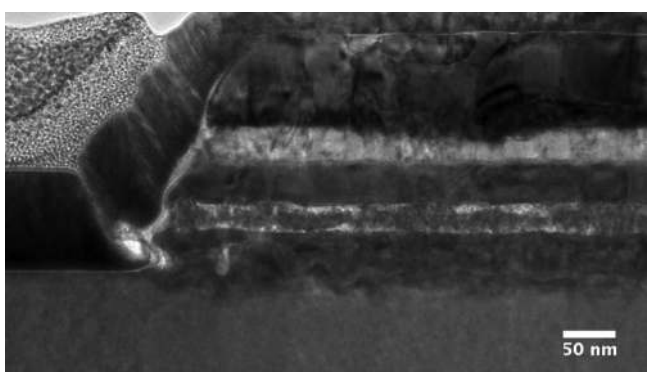

FIG. 8. XTEM of 400 °C second step anneal.

It is important to note that the exact ratio of available reactants (Pd and Si) is more difficult to define in our contact structure compared to Hao's structure, due to the inclusion of a titanium diffusion barrier. Titanium is known to react with palladium at the annealing temperatures employed in our study; for example, some Ti-Pd reaction was seen in the second-step anneal, as shown in Figure 7(b), and confirmed by EDS. For very thin metallizations, this reaction may affect the optimum ratio required to achieve low contact resistance. The Ti and Au layers in our contact stack are merely for convenience during electrical characterization, however, and might not be present in devices. In the absence of a cap material that reacts with Pd, it is expected that the optimum ratio will be slightly lower than reported for this stack. For Pd/Si ratios that were too high, the increase in specific contact resistance could reasonably be due to a lack of excess Si available to be left in the uppermost portion of the InGaAs layer upon the silicide formation.

For Pd/Si ratios that were too low, the mechanism is less clear. Interestingly, for heavily doped samples the contact resistance was insensitive to the reactant ratio. The specific contact resistance remained nominally the same between the optimized and un-optimized contacts, ranging from 1.8×10^{-8} to 2.7×10^{-8} $\Omega\,cm^2$ with standard deviations between 1.6×10^{-9} and 3.2×10^{-9} $\Omega\,cm^2$. This

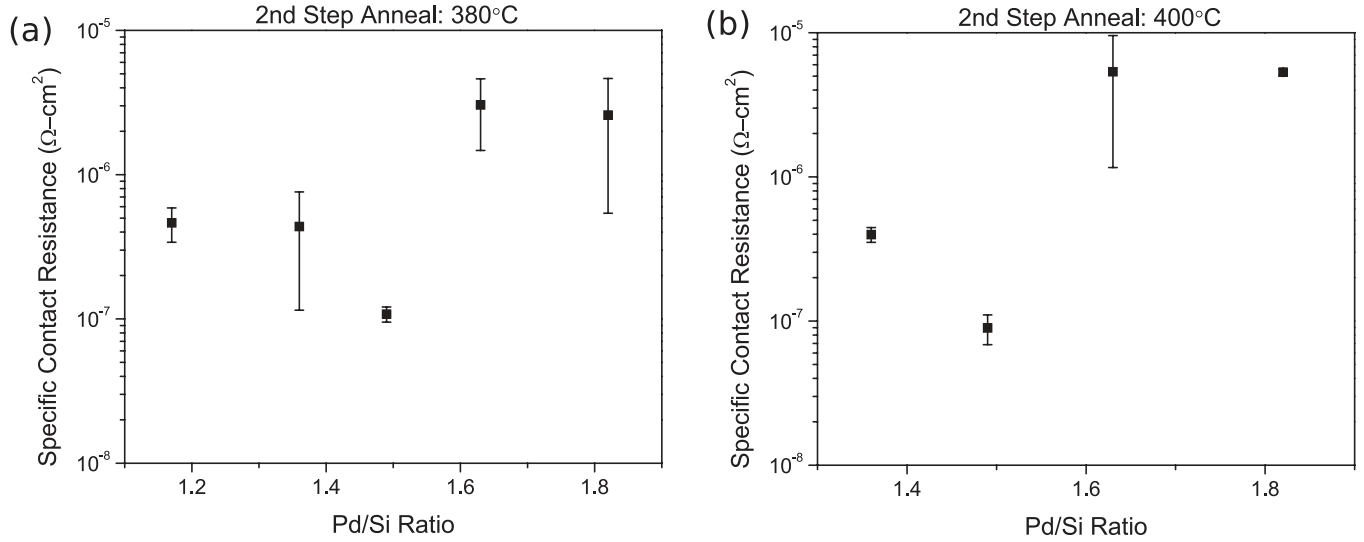

FIG. 9. Specific contact resistance data for varying Pd/Si ratios at (a) 380 °C and (b) 400 °C second step annealing temperatures for 40 s.

insensitivity is likely due to the very small difference between the observed doping introduced by SPR, as will be discussed later in the paper, and the in-grown doping already present in the heavily doped semiconductor. This insensitivity at high doping also indicates that the increase in specific contact resistance from high Pd/Si ratios on lightly doped samples is due to a change in the doping introduced rather than resistance introduced in the contact stack itself.

To investigate the presence of excess Si dopant in the regrown InGaAs, I-V-T measurements were made on lightly doped contacts with a Pd/Si ratio of 1.5 annealed at 200 °C/30 s and 380 °C/40 s. I-V-T measurements from 77–300 K resulted in a constant specific contact resistance averaging $1.2 \times 10^{-7}\ \Omega\,\mathrm{cm}^2$, which did not change significantly with temperature, indicating current transport by field emission. The field emission model for metal-semiconductor current transport[24] for a degenerately doped semiconductor was employed, as described by Eqs. (1)–(6),

$$E_{00} = \frac{hq}{4\pi}\left(\frac{N_D}{m^*\varepsilon_s}\right)^{1/2}, \tag{1}$$

$$J = J_{0F}\exp(qV/E_{00}), \tag{2}$$

$$J_{OF} = \frac{\pi A^* T}{kC_1\sin(\pi kTC_1)}\exp(-q\phi_b/E_{00}), \tag{3}$$

$$C_1 = (2E_{00})^{-1}\ln[-4(\phi_b - V)/\xi], \tag{4}$$

$$N = \frac{2}{\sqrt{\pi}}N_c(kT)^{-3/2}\frac{2}{3}(E_C - E_F)^{3/2}, \tag{5}$$

$$\rho_c = \left(\frac{A^*T\pi q}{k\sin(\pi C_1 kT)}\exp(-q\phi_b/E_{00}) - \frac{A^* q}{C_1 k^2}\exp[(-q\phi_b/E_{00}) + C_1 q\xi]\right)^{-1}, \tag{6}$$

where E_{00} is the characteristic tunneling parameter, J is the current density, $\xi = E_C - E_F$, N is the carrier concentration as defined by the Fermi-Dirac integral, and ρ_c is the specific contact resistance for $E_{00} \gg kT$.

Theoretical specific contact resistance values were calculated for degenerately doped n-$In_{0.53}Ga_{0.47}As$, with $m^* = 0.074$, $A^* = 8.88 \times 10^4\ \mathrm{A/(m^2K^2)}$, with respect to Schottky barrier heights (SBH) ($\phi_b = 0.1 - 0.5$ eV) and dopant concentrations ($N_D = 4 \times 10^{18} - 3 \times 10^{19}\ \mathrm{cm}^{-3}$) over a range of temperatures from 77 to 300 K. For a given SBH, the experimentally measured specific contact resistance values were matched with the doping density required to obtain this value.

An example using $\phi_b = 0.2$ eV with the measured specific contact resistance of $1.1 \times 10^{-7}\ \Omega\,\mathrm{cm}^2$ for a lightly doped sample is shown in Figure 10. The required N_D concentrations were plotted versus a range of SBHs in Figures 11(a) and 11(b) for a heavily doped and lightly doped sample with measured specific contact resistances of $1.8 \times 10^{-8}\ \Omega\,\mathrm{cm}^2$ and $1.1 \times 10^{-7}\ \Omega\,\mathrm{cm}^2$, respectively. As the SBH is increased, the N_D needed to obtain each specific contact resistances value

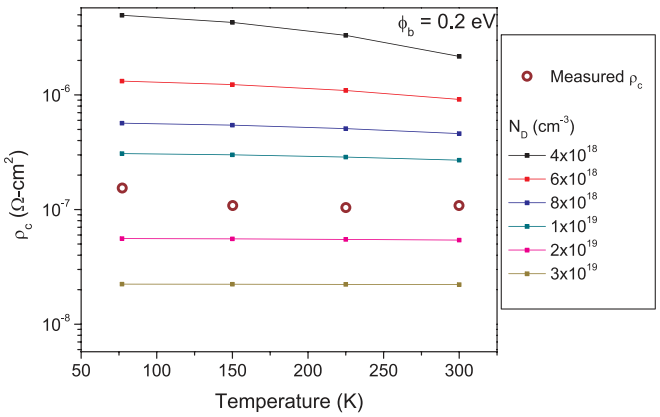

FIG. 10. Specific contact resistances plotted over a range of temperatures and dopant concentrations for a specific SBH. Measured $\rho_c = 1.1 \times 10^{-7}\ \Omega\,\mathrm{cm}^2$ for lightly doped SPR contact with ratio 1.5 and annealed at 200 °C for 30 s and 380 °C for 40 s is also plotted.

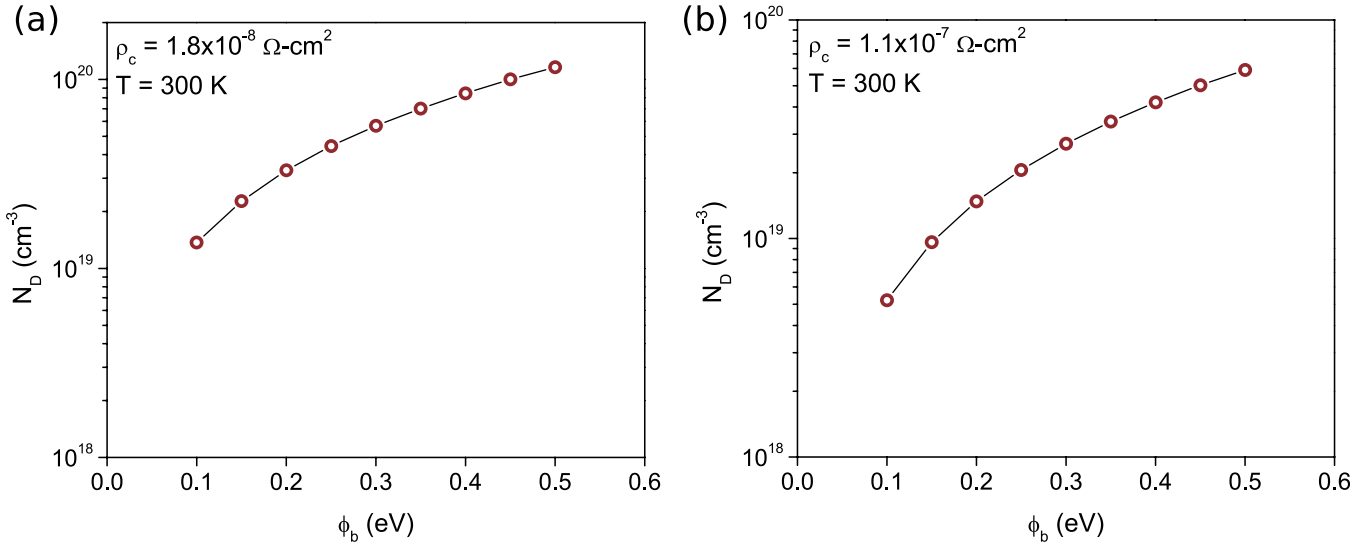

FIG. 11. Required doping density vs. SBH at T = 300 K to obtain the average measured (a) $\rho_c = 1.8 \times 10^{-8}$ Ω cm^2 for the heavily doped SPR contact and (b) $\rho_c = 1.1 \times 10^{-7}$ Ω cm^2 for the lightly doped SPR contact. For $N_D = 3.0 \times 10^{19}$ cm^{-3}, the $\phi_b = 0.19$ eV. Using $\phi_b = 0.19$ eV, the doping density required to obtain measured $\rho_c = 1.1 \times 10^{-7}$ Ω cm^2 is $N_D = 1.3 \times 10^{19}$ cm^{-3}.

ranges from 1.4×10^{19} to 1.6×10^{20} cm^{-3} and 5.2×10^{18} to 5.9×10^{19} cm^{-3}.

Given the original doping concentration of 3.0×10^{19} cm^{-3}, the SBH is then extracted to be 0.19 eV in Figure 11(a). This extracted value closely agrees with the conventional SBH value of 0.2 eV for n-InGaAs.[25–27] Using the extracted barrier height of 0.19 eV, the required N_D needed to achieve the measured specific contact resistance value for the lightly doped case mentioned above can thus be extracted to be 1.3×10^{19} cm^{-3} in Figure 11(b). Recalling the original doping concentration of 1×10^{17} cm^{-3} in the n-InGaAs epilayer, the extracted value is two orders of magnitude higher. The value represents the dopant concentration present in the InGaAs at the contact interface after the final annealing step.

For the heavily doped epilayers, the insensitivity of the Pd/Si ratio, and thus the SPR process, on the specific contact resistance may be due to insignificant increase in doping concentration. Pd/Ti/Au (control) and Pd/Si/Pd/Ti Au (SPR) contacts were deposited on 3.0×10^{19} cm^{-3} doped Si:In $_{0.53}Ga_{0.47}$ As epilayers. Specific contact resistances measured for these contacts were statistically identical, indicating that no additional dopant was introduced by the SPR process on the heavily doped layers.

Recall that the final dopant concentration of the lightly doped samples was extracted to be $N_D = 1.3 \times 10^{19}$ Ω cm^{-3}, which is less than the dopant concentration present in the heavily doped sample. This comparison combined with the lack of contact resistivity reduction in the heavily doped SPR sample versus its control indicate that the insensitivity of the Pd/Si ratio in heavily doped samples is due to the lack of additional dopant incorporation.

Minimum specific contact resistance values of 9×10^{-8} Ω cm^2 and 1.8×10^{-8} Ω cm^2 were achieved for lightly and heavily doped epilayer samples, respectively. These values are a record low, significantly lower than previous SPR-based contacts reported in the literature. Reasons for this include the change from a 1-step rapid thermal anneal process used in recent literature[10,11] to a 2-step rapid thermal anneal process and the exploration of Pd/Si ratios in the contact structure. The formation of the Pd-rich quaternary phase is a low activation energy process due to its observed formation as deposited, with the Pd diffusion activation energy in GaAs of only 0.35 eV calculated by Yeh *et al.*[28] Pd_2Si formation is a higher activation energy process, calculated as 0.9 eV by Cheung *et al.*[29] Because of this situation, the 2-step anneal process should promote each step in series rather than in parallel as with a 1-step anneal process. While previous work has estimated introduced N_D in GaAs to be near 2.0×10^{19} cm^{-3},[8,30] reports on InGaAs that extract levels of doping are not widely available to compare to our results.

IV. CONCLUSIONS

We have shown in this paper a minimum mean specific contact resistance value of 1.8×10^{-8} Ω cm^2 on 3×10^{19} cm^{-3} doped Si : $In_{0.53}Ga_{0.47}As$ and 9×10^{-8} Ω cm^2 for 1×10^{17} cm^{-3} doped Si : $In_{0.53}Ga_{0.47}As$, which are significantly lower values than previously demonstrated solid phase regrowth contacts. Reasons we have been able to achieve low specific contact resistance values include the exploration of various Pd/Si ratios in the contact structure and the use of a 2-step annealing treatment.

We also show substantial evidence that solid phase regrowth is the dominant mechanism for the creation of this ohmic contact. XTEM and SAED show deep reaction at lower annealing temperatures followed by reaction front retreat at higher temperatures, as well as the expected Pd_2Si phase after annealing, and the strong dependence of specific contact resistance on the Pd/Si raztio. I-V-T measurements show evidence of enhanced Si dopant concentration introduced by SPR process.

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