Ultra-low-voltage CMOS Crystal Oscillators

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***Abstract*—In this paper, 32 kHz crystal oscillators operating with only 60 mV supply are presented. Two implementations based on a Schmitt trigger circuit for two different crystals were designed and experimentally characterized. The circuits require 45 µm x 74 µm and 78 µm x 83 µm, respectively, within a 130 nm CMOS process. The power consumptions of the oscillators are 2.26 nW and 15 nW and the temperature stabilities attained are 62 ppm (25-62°C) and 50 ppm (5-62°C), respectively. The dependence on the supply voltage of the current consumption, fractional frequency, start-up time and oscillation amplitude were measured. The Allan deviation is 30 ppb for both oscillators.**

***Index Terms*—ultra-low-voltage, crystal oscillator, Schmitt trigger, Pierce oscillator, subthreshold, 32 kHz XO.**

I. Introduction

WIRELESS sensor nodes require very tight power budgets to operate from either a small battery or some energy harvesting mechanism, or both [1].

In many cases, thermal or electrochemical harvesting devices provide very low voltages of the order of 100 mV or even lower [2]–[4]. CMOS electronics is possible at such low supply voltages [5], [6], which are well below the supply that minimizes the energy per operation, typically in the range of 200 to 350 mV. The minimum energy per operation point may be the ideal condition for the active operation of a circuit [7], but this is not the case for circuits with long standby times. In effect for such circuits the power spent can be minimized by setting the supply voltage to its lowest possible value in the standby mode [6]. Due to the positive feedback, the Schmitt trigger provides a significant gain for voltages below $4kT/q$, approximately 100 mV at room temperature. This feature could enable CMOS electronics operating from such voltage levels. Practical ultra low voltage levels would be $4kT/q$ for digital circuits [8] and $5kT/q$ for analog RF circuits [9]. Additionally, for circuits operating from low voltage energy harvesters, reducing the minimum supply voltage required by the electronics simplifies the design of the voltage step-up converters.

Time-keeping functionality is required in IoT systems and the time-keeping module must be on at all times. Also, synchronization between nodes in a wireless sensor network is vital in order to keep the exchange of coordination messages to the minimum [1].

Crystal oscillators have proven to be useful for low power time-keeping applications, and in this context supply voltage lowering is a convenient strategy [10]–[12].

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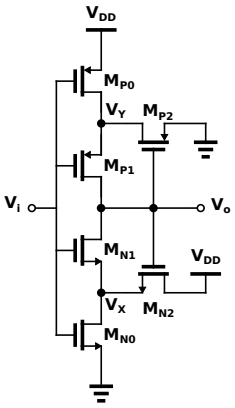


Fig. 1. Six transistor Schmitt trigger circuit schematic.

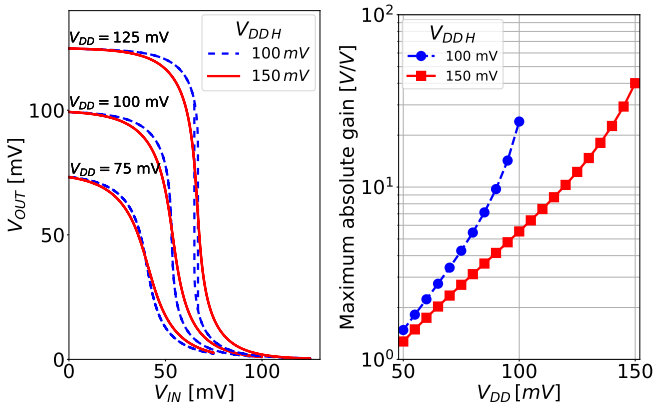
In this paper, two circuit implementations of 32 kHz crystal oscillators are presented. They operate from a 60 mV supply using a Schmitt trigger circuit as the inverting amplifier to compensate for the crystal losses. One oscillator is built with a crystal suitable for smaller external capacitors while in the other a crystal with a larger quality factor is used, providing more frequency stability over temperature but with a larger power consumption. The design of a Schmitt trigger working as an amplifier is detailed in Section II. The basics of the Pierce oscillator design are summarized in Appendix A. Section III brings all of the pieces together to present the design of the two oscillators. Here the losses in the Pierce oscillator are taken into consideration to properly design the transconductance, G_m, and output conductance, G_o, of the Schmitt trigger to compensate for these losses in the ultra low voltage context. Simulation and measurement results are reported, discussed and compared with theoretical results in Sections IV and V. Lastly, some conclusions are drawn in Section VI.

II. Schmitt trigger as an amplifier

For ultra-low-voltage operation, we previously designed a Schmitt trigger circuit operating as an amplifier for the Pierce oscillator [13]. The Schmitt trigger topology is shown in Fig. 1.

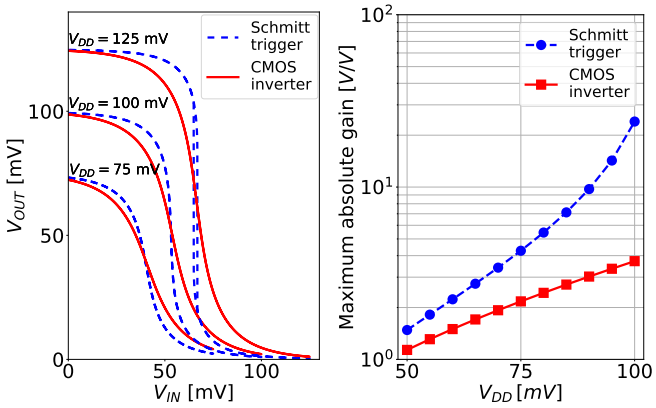
In ultra-low-voltage operation, both nMOS and pMOS are in the weak inversion (WI) region. The MOS transistor drain current in WI is given by [11] and [14]. Thus, the nMOS drain current is

$$I_{D\,N} = I_N\, e^{\frac{V_{GB}}{n_N \phi_t}} \left(e^{-\frac{V_{SB}}{\phi_t}} - e^{-\frac{V_{DB}}{\phi_t}} \right), \qquad (1)$$



(a) (b)

Fig. 2. (a) Voltage transfer characteristic of two Schmitt triggers designed to exhibit hysteresis at different supply voltages, V_{DDH}, and (b) their maximum absolute gain as a function of the supply voltage V_{DD}.



(a) (b)

Fig. 3. (a) Voltage transfer characteristic of a Schmitt trigger with V_{DDH} = 100 mV and of a CMOS inverter and (b) their maximum absolute gain as a function of the supply voltage V_{DD}.

where the current scaling factor I_N, which represent the transistor strength, is given by

$$I_N = \mu_N . n_N . C'_{ox} . \phi_t^2 . \frac{W}{L} . e^{-\frac{|V_{T0N}|}{n_N \phi_t}+1}. \quad (2)$$

W/L is the aspect ratio, μ_N is the mobility, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage, V_{T0N} is the threshold voltage and n_N is the slope factor.

G, S, D and B are the gate, source, drain, and bulk nodes, respectively. The expression for the pMOS current is obtained from (1) changing V_{SB} by V_{BS}, V_{DB} by V_{BD} and V_{GB} by V_{GB}.The expression for the current strength of the pMOS transistor is the same as (2), using the pMOS parameters.

All transistors of the Schmitt trigger are such that every pMOS has the same current strength as its symmetric nMOS, that is, $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$ and $n_N = n_P = n$.

As shown in [15], the minimum supply voltage to obtain hysteresis in a Schmitt trigger with balanced pMOS and nMOS subcircuits is given by

$$V_{DDH} \approx 2\phi_t \, ln \left[n \left(1 + \frac{I_0}{I_2} \right) \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0} \right) - \frac{I_1}{I_0} \right]. \quad (3)$$

Figures 2a and 2b show the voltage transfer characteristic and the maximum absolute gain, respectively, of two Schmitt triggers, one with V_{DDH} = 100 mV and the other with V_{DDH} = 150 mV.

Note that the maximum absolute gain increases until hysteresis appears at a certain level, herein V_{DDH}. It can be seen that, for the same supply voltage V_{DD}, the Schmitt trigger that exhibits hysteresis at a lower voltage consistently has a higher maximum absolute gain. The value of V_{DDH} depends on the values of I_0, I_1 and I_2, and thus is chosen during the design. I_0 = 70 nA, I_1 = 2.8 nA and I_2 = 25 nA give V_{DDH} = 100 mV, while I_0 = 46 nA, I_1 = 7.4 nA and I_2 = 4.6 nA give V_{DDH} = 150 mV.

On the other hand, Figures 3a and 3b let us compare the gain of a CMOS inverter to the gain of a Schmitt trigger, as a function of V_{DD}. The Schmitt trigger exhibits a much higher maximum absolute gain. Thus, for a given supply voltage it is possible to design a Schmitt trigger with maximum absolute gain much higher than that of a CMOS inverter.

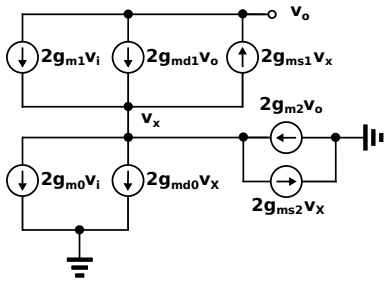


Fig. 4. Six transistor Schmitt trigger circuit low-frequency small-signal equivalent model for $V_I = V_O = V_{DD}/2$.

The equivalent small-signal model of the Schmitt trigger in Fig. 4, looks like the nMOS network small-signal model, but all transconductance values are doubled. The numbers in the subscripts of the transconductances refer to the number of the transistor indicated in Fig. 1. This small signal model holds, provided that the supply voltage is lower than V_{DDH}, preventing the hysteresis from appearing. Later in Section V, the results will show that the performance of the oscillator is degraded for supply voltages above V_{DDH}.

The Schmitt trigger can be represented by an equivalent transconductance G_m and an equivalent output conductance G_o. These two parameters are expressed in terms of g_{mg}, g_{ms} and g_{md} in Appendix B.

Lastly, the Schmitt trigger voltage gain is expressed as

$$A = \left. \frac{v_o}{v_i} \right|_{V_I = V_O = V_{DD}/2} = -\frac{G_m}{G_o}. \quad (4)$$

The voltage gain is a function of the supply voltage V_{DD}, the ratios I_1/I_0 and I_2/I_0, and the slope factor of nMOS and pMOS devices n_N and n_P (considered equal for the sake of simplicity, without loss of generality, thus: $n = n_N = n_P$). The absolute voltage gain increases with the transconductance

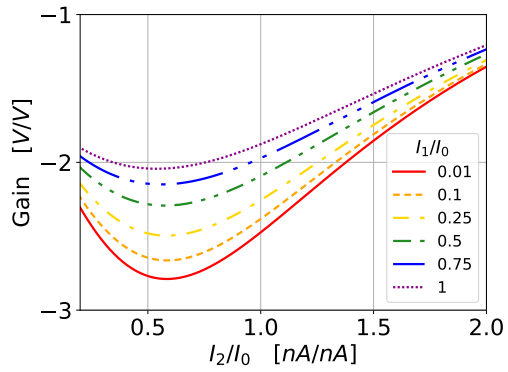


Fig. 5. Voltage gain as a function of I_1/I_0 and I_2/I_0 given by (4), with $n = 1.3$ and $V_{DD} = 60\,mV$, based on [13].

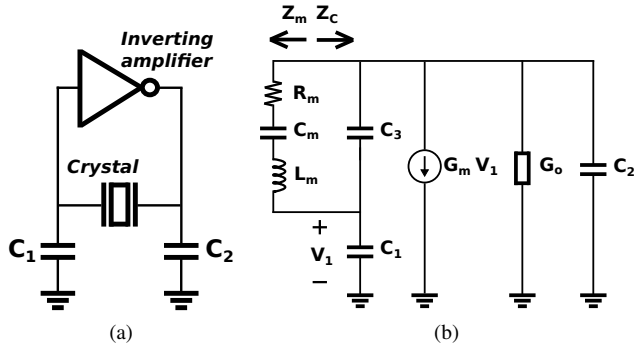


Fig. 6. Pierce crystal oscillator (a) circuit schematic and (b) impedance equivalent model.

G_m, and the latter should be sufficient to compensate for all losses to enable oscillation.

Figure 5 shows the dependence of the voltage gain on I_2/I_0, for constant values of I_1/I_0 and supply voltage $V_{DD} = 60$ mV. We have chosen this ultra-low-voltage to explore the frontier of the design space. A practical ultra-low-voltage complex circuit should operate with a minimum supply of 100 mV as explained in the introduction. For values of I_2/I_0 close to 0.5, independently of the ratio I_1/I_0, the maximum absolute gain is reached. Therefore, $I_2/I_0 = 0.5$ is chosen. On the other hand, the lower the ratio I_1/I_0, the larger the magnitude of the voltage gain. $I_1/I_0 = 0.25$ is chosen for the sake of layout simplicity. In this case, the voltage gain is $A = -2.48$ V/V.

As a consequence, after V_{DD}, I_1/I_0 and I_2/I_0 have been selected and n is given by the process chosen, G_m and G_o can be expressed only in terms of the current strength I_0.

III. Design of Crystal Oscillators Based on Schmitt Trigger

A schematic of a Pierce oscillator [11], consisting of a quartz crystal connected to an amplifier and two functional capacitors C_1 and C_2, can be seen in Fig. 6a.

Fig. 6b shows the equivalent impedance model of the circuit in Fig. 6a. On the left side, the series association of R_m, C_m and L_m represent the crystal motional impedance. On the right side, Z_C represents the small signal model of the rest of the circuit connected in parallel to the crystal and also the crystal parallel capacitance C_3. G_m and G_o are the transconductance and the output conductance of the inverting amplifier, respectively.

The key auxiliary parameters and equations of this circuit, based on [11], are summarized in Appendix A.

Two oscillators, A and B, were designed. Oscillator A includes a crystal suitable for smaller external capacitors. On the other hand oscillator B uses a crystal with a lower motional resistance, R_m, providing a larger quality factor Q.

Table I summarizes all parameters related to the two crystals, that is, resonance frequency f, motional capacitance C_m, motional inductor L_m, motional resistance R_m, quality factor Q, the load capacitance C_L (C_1 in series with C_2) and the parallel capacitance C_3. Here, $C_1 = C_2 = 2 \times C_L$ for simplicity. A feedback resistor R_F is connected in parallel to the crystal for biasing purposes.

TABLE I
Crystals and Other Discrete Components of the Oscillators.

Parameter	Oscillator A	Oscillator B
Crystal part number	ABS07W-32.768kHz-D1	AB38T-32.768kHz-12.5pF-E-7
$f\,[kHz]$	32.768	32.768
$C_m\,[fF]$	4.68	3.5
$L_m\,[H]$	5 048.571	6 740.193
$R_m\,[k\Omega]$	38.194	15.419
Q	27 214	90 000
$C_L\,[pF]$	3	12.5
$C_1 = C_2\,[pF]$	6	25
$C_3\,[pF]$	1.15	1.60
$R_F\,[G\Omega]$	5	5

A Schmitt trigger is used as the inverting amplifier of the Pierce oscillator. As a rule of thumb [16], the transconductance G_m is designed to be $3\times G_{mcrit}$, with G_{mcrit} the critical value of the transoconductance to enable oscillation. In addition, the transconductance G_m is further increased to compensate losses in G_o. With $C_1 = C_2$, $\Delta G_m = G_o$ as shown in Appendix A. Thus,

$$G_m = 3 \times G_{mcrit} + G_o. \tag{5}$$

From (4) and (5),

$$G_m = \frac{3 \times G_{mcrit}}{1 + 1/A}. \tag{6}$$

On the other hand, G_m can be expressed only in terms of the design parameters I_0, I_1, I_2 and V_{DD}, according to (15) found in Appendix B. Figure 7 shows the dependence of I_0 on the transconductance G_m, for $I_1/I_0 = 0.25$ and $I_2/I_0 = 0.5$ according to the design in Section II. As a consequence, I_0 is determined for each oscillator, with $G_{m\,A} = 561$ nS and $G_{m\,B} = 2\,612$ nS according to the values in Table I.

Table II summarizes all parameters related to both Schmitt trigger circuits, that is, the supply voltage V_{DD}, current strengths I_0, I_1 and I_2, current consumption I_{DD}, voltage gain A, transconductance G_m, output conductance G_o and dimensions of all the transistors involved.

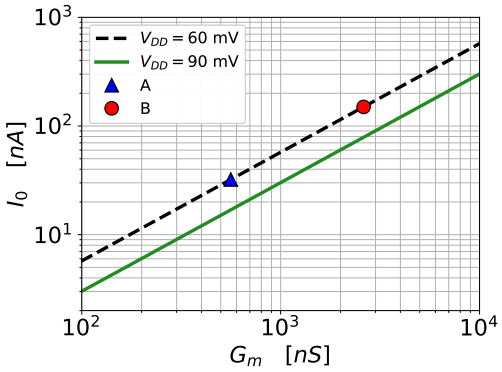


Fig. 7. The required current strength parameter I_0 as a function of the transconductance G_m in (15), for supply voltages 60 mV and 90 mV. G_m also fulfills (6) for each oscillator, A or B, with $G_{m\,A} = 561$ nS (blue triangle) and $G_{m\,B} = 2\,612$ nS (red circle).

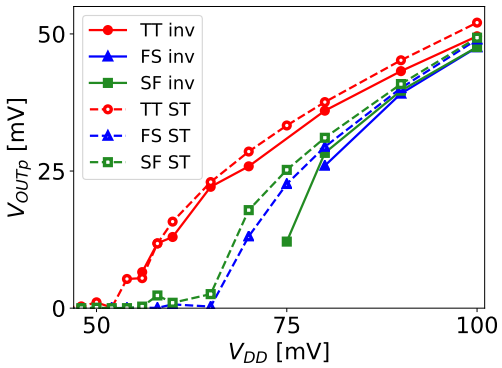


Fig. 8. Simulation results of the output peak amplitude of an oscillator based on a CMOS inverter and an oscillator based on a Schmitt trigger, versus the supply voltage.

TABLE II
OPERATING POINT AND TRANSISTOR DIMENSIONS OF BOTH SCHMITT TRIGGER CIRCUITS.

	Parameter	A	B
Design parameters	$V_{DD}\,[mV]$	60	60
	$I_0\,[nA]$	32.2	150
	$I_1\,[nA]$	8.05	37.5
	$I_2\,[nA]$	16.1	74.9
Performance parameters	$I_{DD}\,[nA]$	27.7	129
	$G_m\,[nS]$	561	2 612
	$G_o\,[nS]$	226	1 053
	$A\,[V/V]$	-2.48	-2.48
Transistor dimensions	$L_{N,\,P}\,[\mu m]$	1.08	1.08
	$W_{N0}\,[\mu m]$	8×5.1	16×11
	$W_{P0}\,[\mu m]$	8×53	16×120
	$W_{N1}\,[\mu m]$	2×5.1	4×11
	$W_{P1}\,[\mu m]$	2×53	4×120
	$W_{N2}\,[\mu m]$	4×5.1	8×11
	$W_{P2}\,[\mu m]$	4×53	8×120

Lastly, a couple of assumptions remain to be verified. Equation (9), with $C_1 = C_2$, becomes $2\omega R_m C_3(1+2C_3/C_1) \ll 1$, which holds for oscillators A and B, given that $0.035 \ll 1$ and $0.011 \ll 1$, respectively. Also, in Appendix A it is stated that even though G_m is 3 times the critical value, it would still be well below G_{mopt} in (10). Since $G_{mopt\,A} = 8\,915$ nS and $G_{mopt\,B} = 90\,719$ nS, it holds that $G_m \ll G_{mopt}$.

To complete the understanding on the advantages of using a Schmitt trigger instead of a CMOS inverter, an oscillator based on a CMOS inverter and using the crystal in oscillator A, was designed. For comparison purposes the same unitary transistors are used and $V_{DD} = 60$ mV. Figure 8 shows the simulation results of output voltage amplitude of the oscillators based on a CMOS inverter and based on a Schmitt trigger. The results in the FS and SF corners show that the CMOS inverter has a lot more variability than the Schmitt trigger. In fact, the oscillator based on a CMOS inverter in the FS corner does not start with less than 80 mV supply and in the SF corner with less than 75 mV supply. Furthermore, the simulation results also show that the standard deviation of the oscillation frequency is 0.16 Hz and 0.53 Hz in the case of the Schmitt trigger and the CMOS inverter, respectively.

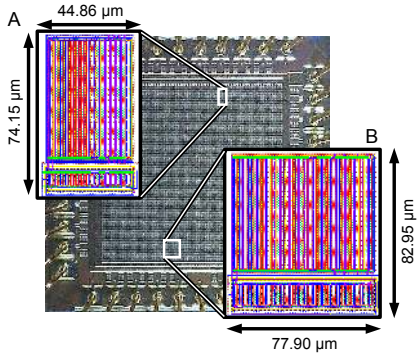


Fig. 9. Microphotograph of the fabricated IC, showing circuits A and B, which are the two Schmitt trigger circuits refered to in this paper.

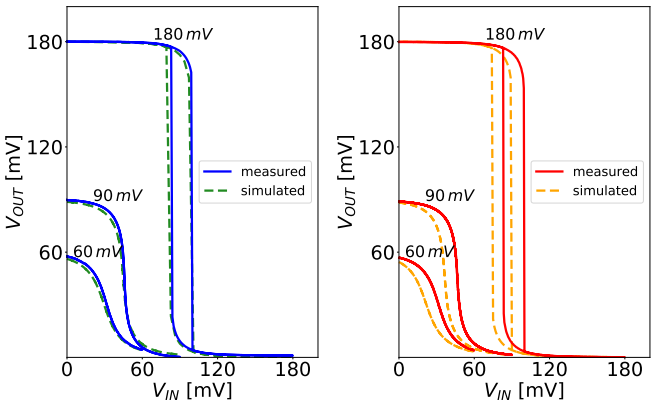
The fact that the oscillators in the FS and SF corners do not start, together with the higher standard deviation of the oscillation frequency, make the oscillator based on a CMOS inverter unsuitable at supply voltages as low as 60 mV.

IV. MEASUREMENT RESULTS FOR THE SCHMITT TRIGGER AS AN AMPLIFIER

A test chip including circuits A and B was designed and fabricated in a 130 nm technology. A microphotograph of one die is shown in Fig. 9. The actual position of these circuits in the die and their dimensions were drawn and superimposed. The layout of each circuit is also depicted. The area occupied by circuit A is 44.86 µm × 74.15 µm. Circuit B occupies a larger area (77.90 µm × 82.95 µm), which is related to the need for a higher current drive.

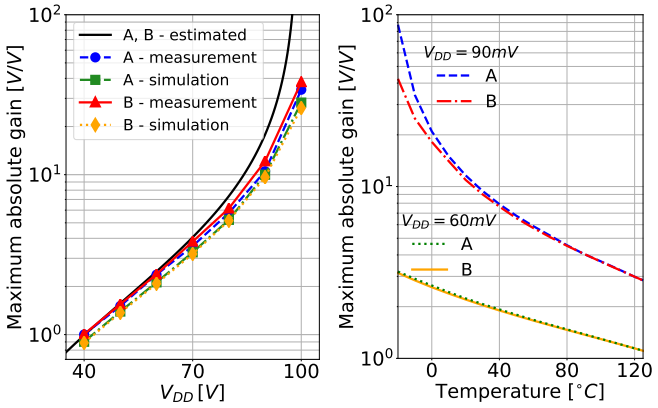
The voltage transfer characteristic of the Schmitt trigger was measured as a function of the supply voltage by means of a semiconductor parameter analyzer (HP4156). Figs. 10a and 10b, show the voltage transfer characteristic of circuits A and B, respectively, and the simulation results are also shown.

The maximum absolute gains for circuits A and B were extracted from the voltage transfer characteristic measurements and simulations, as shown in Fig. 11a. The estimated



(a) (b)

Fig. 10. Simulation and measurement results for the Schmitt trigger voltage transfer characteristic. Results for different supply voltages are displayed for both circuits, (a) A and (b) B.



(a) (b)

Fig. 11. Maximum absolute gain of the Schmitt trigger for circuits A and B, showing their dependence on (a) the supply voltage (simulations and measurements) and (b) the temperature (simulations only). For $V_{DD} \geq 100$ mV hysteresis appears, and the circuits no longer work as amplifiers.

curve was calculated using (4), which is why the results are expected to be the same for circuits A and B, since they were designed to achieve the same gain. Accordingly, the simulation results for the two circuits are exactly the same. In the case of the measurements, the results are acceptably close. Note that the predicted gain for $V_{DD} = 40$ mV is unity, thus for $V_{DD} < 40$ mV the maximum absolute voltage gain is less than 1, disabling regeneration. The values for $V_{DD} \geq 100$ mV are not included since hysteresis appears, and these circuits are meant to work as the amplifier of a Pierce oscillator exhibiting no hysteresis.

Figure 11b shows the simulation results for the maximum absolute gain over temperature. Since the gain decreases with increasing temperature to well below 2 V/V for a 60 mV supply, the measurement of the frequency of the oscillators as a function of the temperature was taken using a 90 mV supply, in order to arrive at insightful conclusions. These simulations predicted a slightly higher maximum absolute gain for circuit A compared with circuit B, in agreement with the simulation results reported in Fig. 11a. This effect becomes more relevant for low temperatures and $V_{DD} = 90$ mV.

V. Measurement Results for the Crystal Oscillators

Two PCBs were built in order to fully test both oscillators, one of which is based on circuit A and the other on circuit B. The values for the parameters of the crystals, the external capacitances and the feedback resistors, are reported in Table I.

A buffering stage is also included in the PCB and connected at the output using a TL072 operational amplifier, which has a very low input capacitance, to avoid excessively loading the oscillator. The actual capacitors connected to the crystal, the parasitic capacitances and the buffering stage input capacitances must add up to the design values of C_1 and C_2, in order to properly tune the oscillation frequency. Unfortunately, the parasitic capacitances within oscillator A are too large, exceeding the total capacitance needed. As a consequence, the frequency of oscillator A was lower than the nominal

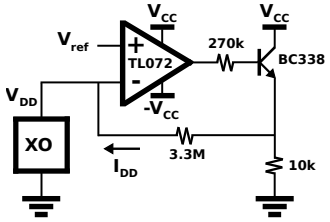


Fig. 12. Schematic of the auxiliary circuit used for current measurements.

resonance frequency of the crystal, which implies a poorer frequency stability. This and other consequences are fully explained in the rest of the paper and their impact on the performance parameters is quantified. In the case of oscillator B, the oscillation frequency was finely trimmed to the nominal frequency.

The measurement setup includes two DC voltage sources (HP 3245A, Tektronix PS280) to supply the oscillator and the buffering stage, respectively, an oscilloscope (Tektronix 1001B), a multimeter (Fluke 8846A). Also, another multimeter (Fluke 289) was used to measure temperature.

The current delivered to each of the oscillators was measured using a simple auxiliary current-to-voltage converter circuit [17] shown in Fig. 12. The results for oscillators A and B are given in Figs. 13a and 13b, respectively. It can be seen that the current and power consumption increase exponentially with the supply voltage, as expected for WI operation. However, the results for oscillator B deserve further inspection, since the measurement results are not very well predicted by the simulations. To this aim, Monte Carlo simulation results for the current consumption are shown in Figs. 14a and 14b for both oscillators with 60 mV and 90 mV supplies, respectively. It is seen that oscillator B measured current falls far from the distribution mean value, in agreement with the results presented in Fig. 13b. Consistently with results shown in Fig. 13a, oscillator A exhibits a measured current closer to the mean value of the distribution.

The variations of the drain currents of the transistors over

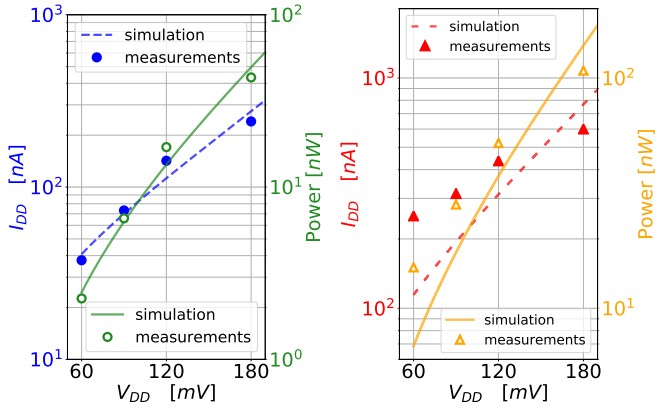


Fig. 13. Simulation and measurement results for the oscillators (a) A and (b) B, DC current and power consumption versus the supply voltage.

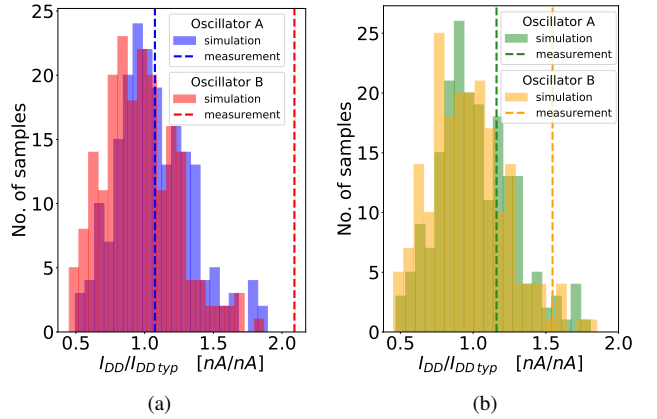


Fig. 14. Monte Carlo simulation and measurement results for the normalized current consumption of oscillators A and B for (a) 60 mV and (b) 90 mV supplies. The Monte Carlo simulations were run for 200 samples to obtain data for both the mismatch and the process variation.

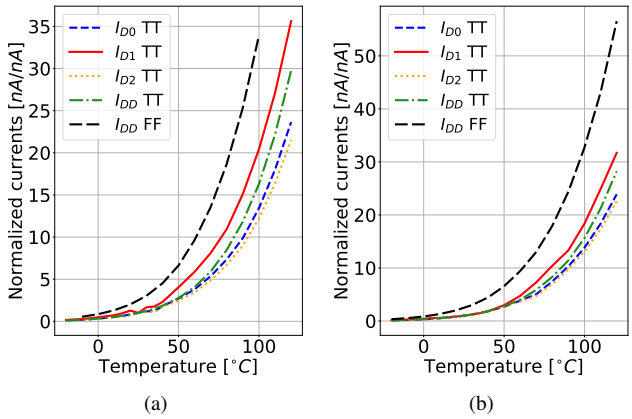


Fig. 15. Simulation results for the oscillators (a) A and (b) B, DC currents in steady state over temperature. I_{D0}, I_{D1} and I_{D2} are the drain current of transistors M_{N0}, M_{N1} and M_{N2}, respectively, normalized to the value at 25°C and 60 mV supply. I_{DD} is the current consumption of the oscillator in the TT and the FF corners, normalized to the value at 25°C and 60 mV supply in the TT corner

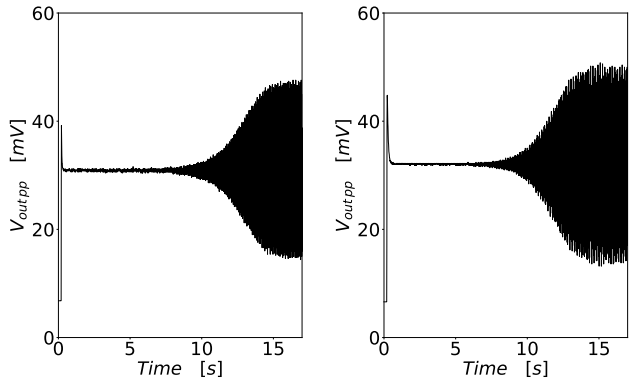


Fig. 16. Start-up of oscillators (a) A and (b) B, with 60 mV supply.

temperature, as well as the total current consumption over temperature, were simulated. The results are shown in Figs. 15a and 15b, for oscillators A and B, respectively. All the currents are normalized to their typical value at 25°C. The results for the total current consumption I_{DD} in the worst case corner, FF, are also shown. In this corner, oscillator A starts-up only in the range from -10 to 100°C, while oscillator B starts-up in the whole considered temperature range.

A. *Oscillator start-up*

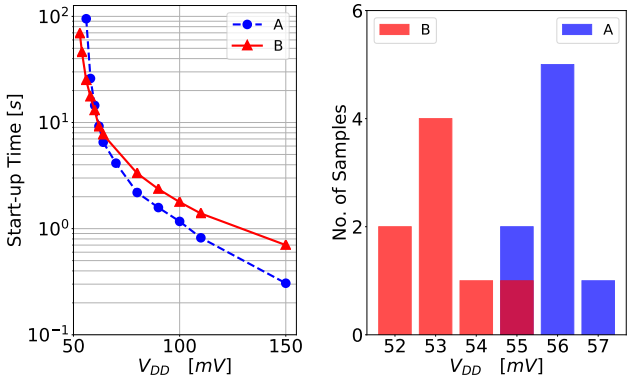
Figures 16a and 16b show the start-up transient measurements for oscillators A and B, respectively, for a supply voltage of 60 mV. The start-up time was measured for both oscillators with different values of the supply voltage V_{DD}, and the results are shown in Fig. 17a.

In order to determine the minimum supply voltage for which the oscillator starts up, measurements for eight samples were taken and the results are plotted in Fig. 17. It can be seen that all oscillators start up and that this occurs for supply voltages below 60 mV. Oscillator B starts-up at a lower supply voltage than oscillator A, which is consistent with the fact that circuit B exhibits a higher maximum absolute gain than circuit A, according to the results shown in Fig. 11a.

The minimum supply voltage varies over temperature, giving a minimum supply to start of 80 mV and 75 mV for oscillators A and B, respectively, at the upper limit of the temperature range measured (62°C).

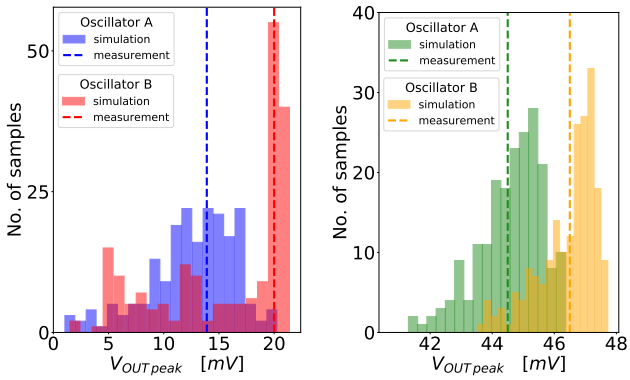
B. *Oscillator output voltage amplitude*

The output voltage amplitude of oscillators A and B at resonance frequency was simulated through Monte Carlo simulations of the mismatch and process variation. The results are presented in Figs. 18a and 18b for supply voltages of 60 mV and 90 mV, respectively. Oscillation takes place with a yield of 100%, even though for a 60 mV supply the output signal could attain a peak to peak amplitude as small as 3 mV in some cases. Statistically, there is 5% probability that a sample of oscillator A exhibits a peak to peak output voltage smaller than 10 mV and in the case of oscillator B the probability is 9%. As seen in Fig. 18b, this effect decreases for a larger



(a) (b)

Fig. 17. Measurement results for oscillators A and B: (a) start-up time versus supply voltage and (b) minimum supply voltage for starting up. The start-up time was measured from the instant the DC output voltage reached 90 % of its final value until the instant when the amplitude of the oscillating signal was 90 % of its value at steady state.



(a) (b)

Fig. 18. Monte Carlo simulation and measurement results for the amplitude of the output voltage of oscillators A and B for (a) 60 mV and (b) 90 mV supplies. The Monte Carlo simulations were run for 200 samples to obtain data on both the mismatch and the process variation.

supply voltage, where all oscillator A samples attain at least a 39 mV peak and oscillator B samples at least a 36 mV peak.

Figure 19 shows the waveforms for the two oscillators with different supply voltages. The blue discontinuous line corresponds to oscillator A and the red continuous line, to oscillator B. For $V_{DD} = 120$ mV and 180 mV the output waveform is visibly no longer sinusoidal. Furthermore, the harmonic components increase with the supply voltage. It should be noted that for $V_{DD} = 110$ mV and above the Schmitt trigger exhibits hysteresis and loses the purely amplifying characteristic.

C. Oscillator frequency

The frequency of the oscillators was measured, by means of a frequency counter (Agilent 53230A) linked to a time source (Symmetricom 5071A primary cesium frequency standard). The measurement results for the two oscillators are shown in Fig. 20a. The fractional frequency was normalized to the frequency obtained with a 60 mV supply. For oscillators A

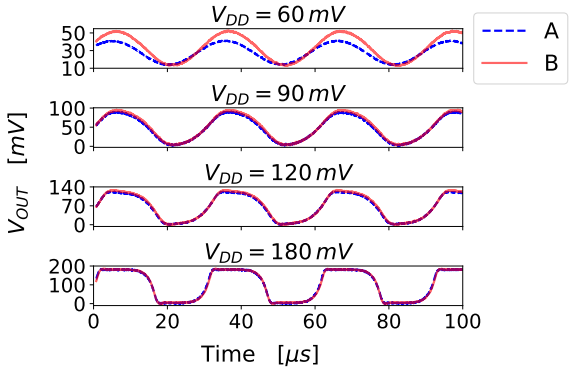
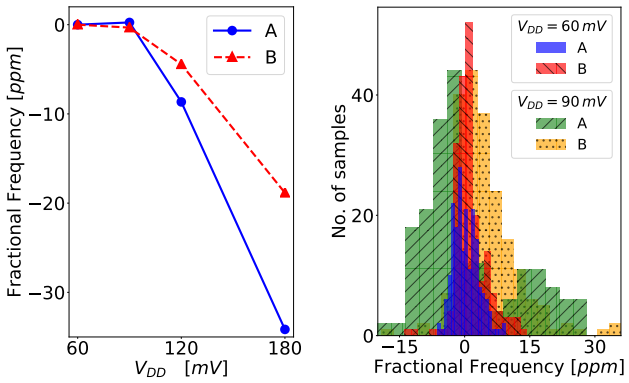


Fig. 19. Measurement results for the output voltage with different supply voltages, V_{DD}, for oscillators A and B.



(a) (b)

Fig. 20. (a) Measurement results for the fractional frequency normalized to that obtained with a 60 mV supply for oscillators A and B, and its dependence on the supply voltage. (b) Monte Carlo simulation results for the normalized fractional frequency for oscillators A and B, with either 60 mV or 90 mV supply. Simulations were run for 200 samples to obtain both mismatch and process variation.

and B, the fractional frequency varies only 0.251 ppm and 0.328 ppm, within the range from 60 mV to 90 mV supply, respectively. As a consequence, the fractional frequency has little dependence on the supply voltage within the range of interest where there is no hysteresis. As the hysteresis appears the frequency drops.

For reference purposes, the Monte Carlo simulation results are shown in Fig. 20b, where the normalized fractional frequency can be observed for both oscillators for supply voltages of 60 mV and 90 mV.

Fig. 21 shows the measurement results for the frequency stability for both oscillators operating with a 90 mV supply. Even though the temperature setup used allows for accurate temperature setting and measurement, the heating capability is limited to 62°C. Thus, the temperature was ramped from ambient temperature to 62°C within 4 h and back to ambient temperature over another 4 h, and the frequency was measured at a rate of once per second, obtaining as a result the shaded area in which the actual frequency stability falls. The same procedure was carried out to obtain measurements below ambient temperature. The curves for the typical values of the intrinsic instability of the used crystal resonators are super-

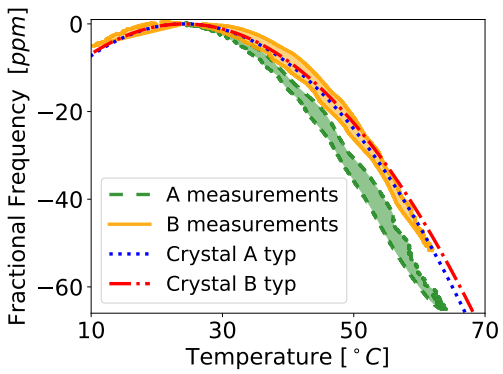
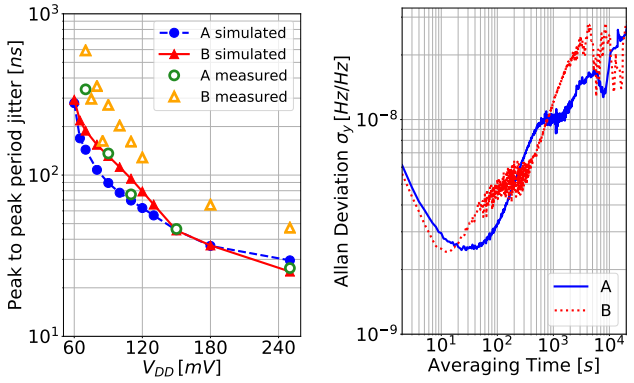


Fig. 21. Measurement results for the fractional frequency normalized to that obtained at 26°C for circuits A and B with 90 mV supply, and its dependence on temperature compared to typical values of the intrinsic instability of the used crystal resonators (provided in the datasheets).



(a) (b)

Fig. 22. Results for the oscillator performance: (a) simulation and measurement results for time jitter versus supply voltage, and (b) Allan deviation measurements with a supply voltage $V_{DD} = 60$ mV.

imposed for reference. The frequency stability of oscillator B falls within the crystal specifications, indicating that the stability is not altered by the presence of circuit B. In the range of 5-62°C, a stability of 50 ppm is attained. On the other hand, oscillator A exhibits less frequency stability, as expected, due to the poor frequency trimming. In this case, the stability is 62 ppm within the range of 25-62°C.

Time jitter was measured using a digital oscilloscope (Tektronix MSO5204). Peak to peak jitter measurements of oscillators A and B are shown next to simulation results in Fig. 22a. As the supply voltage increases the jitter decreases, as expected.

Measurement results of the Allan deviation for both oscillators are shown in Fig. 22. The measurements were taken with an averaging time of 1 s over 10 h, with a maximum temperature variation of 0.5°C. It can be seen that the Allan deviation is below 30 ppb for both oscillators.

D. Comparison to other works

Table III summarizes the details for state-of-the-art ultra-low-voltage crystal oscillators of frequency 32 kHz and compares these to the results of this study.

To the best of the authors knowledge, the oscillators presented herein are the crystal oscillators for 32 kHz with the lowest operating voltage, working with only 60 mV. The closest prior works in terms of low supply voltage are [21] and [18]. [21] reports a minimum supply voltage of 100 mV in part of oscillator circuit, but requires also a second, higher, supply voltage, from 400 mV on. [18] operates down to 150 mV with a supply voltage drift well above all other reported values, remarkable power consumption, temperature stability and Allan deviation. The power consumption reduction is traded-off with a modification in the oscillator output waveform, which might degrade the frequency spectrum. Furthermore, it needs a conventional crystal oscillator to start-up, requiring more area.

The power consumption of oscillator A is very well suited for ultra-low-power applications and in line with other state-of-the-art oscillators. Prior works with comparable ultra-low-power consumption are [24], [19], [18] and [21]. The drawbacks of [18] and [21] have already been discussed. In [24], a power consumption of 0.55 nW is achieved by means of downconverting the signal to DC, amplifying in DC and then upconverting the signal to the frequency of the crystal. An excellent phase synchronization is achieved providing excellent frequency stability over temperature and over time. The output waveform is the result of switching DC levels to obtain a four level switched signal, which will have important harmonic content. The output harmonic content would be filtered by the high quality factor of the crystal. Nevertheless, this might be an issue if spectral purity is needed. [19] reaches a minimum supply voltage of 300 mV while decreasing consumption by means of a sophisticated duty-cycling mechanism. However, a large silicon area is required and the Allan deviation is much larger than that attained in the present work. In order to further reduce the power consumption of a Schmitt trigger-based crystal oscillator, the parasitic capacitances should be lowered using smaller packaging rather than DIP40. Furthermore, a crystal specified for a lower load capacitance would reduce the power consumption. Reduction in packaging capacitances also allows a better tuning of the oscillator frequency in the case of oscillator A.

The approach described herein is also notable for the extremely small silicon area budget, using standard CMOS transistors within a widely used and inexpensive technology. This small area is due to the use of a standalone amplifier, with no calibration or auxiliary circuits needed to improve the power consumption or frequency stability. Other designs shown in Table III are several times bigger, even those in more advanced technology nodes.

Performance aspects, where other designs in Table III are better than this work, are start-up time ([21], [23]) and Allan deviation ([18], [21], which drawbacks were previously discussed). Regarding start-up time, [21] and [23] require much higher minimum operating voltage. Furthermore, the start-up time and the Allan deviation in the designs here presented are still within the range achieved or better than other state-of-the art works, as visible in Table III.

Summing up, the designs shown in this work, provide record low operating voltage and a very compact implementation

TABLE III
COMPARISON TO PRIOR WORK

	[10]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	This work	
									A	B
Technology	2 µm	28 nm	0.13 µm	0.18 µm	55 nm	40 nm	0.18 µm	65 nm	0.13 µm	0.13 µm
Area (mm^2)	N/A	0.03	0.0625	0.027	0.16	0.07	0.035	0.027	0.0033	0.0065
Frequency (kHz)	32.8	32.768	32.768	32.768	32.768	32.76	32.768	32	32.763	32.768
Crystal total load capacitance (pF)	8.2	N/A	3	N/A	N/A	N/A	2.23	7.5	3	12.5
Supply voltage (V)	0.71 - 1.7	0.15 - 0.5	0.3 - 0.9	0.25 - 0.5	0.1 - 0.5 0.4 - 0.8	0.5	0.4 - 5.5	0.5	0.06 - 0.1	0.06 - 0.1
Supply voltage drift (ppm/V)	N/A	∼83	7	N/A	6.7	1	2.1	13	8.4	11
Power consumption (nW)	23	1.89	1.5	2.89	1.7	47	10 nW@1V	0.55	2.26	15.0
Amplitude of oscillation (mV)	130	150	230	250	100	N/A	90	500	27.5	40
Start-up time	N/A	N/A	31 s	N/A	8 ms	N/A	1 ms	0.2 s	14.5 s	13.0 s
Temperature stability	N/A	48.8 ppm -20∼80°C	-150 ppm 0∼80°C	N/A	109.1 ppm -20∼80°C	0.25 ppm/°C @room temp	120 ppm -40∼85°C	80 ppm -20∼80°C	-62 ppm 25∼62°C	-50 ppm 5∼62°C
Allan deviation	N/A	∼2 ppb	90 ppb	N/A	2.5 ppb	N/A	N/A	14 ppb	30 ppb	30 ppb

The crystal oscillator in [21] is PLL-assisted and requires two different supply voltages. The two operating ranges are reported.
Crystal total load capacitance is the series of C_1 and C_2, including parasitic capacitances.
Amplitude of oscillation is peak to peak.
Amplitude of oscillation and power consumption are reported at the lowest operating supply voltage.
Unless stated otherwise, results are reported at room temperature.

with competitive consumption and precision specifications (temperature stability, long term stability, supply voltage drift).

VI. CONCLUSION

The design, simulation and measurement results for two crystal oscillators are presented herein. They are based on the application of a Schmitt trigger as an amplifier. Guidelines for designing this block to be the amplifier of a crystal oscillator are provided. The amplifiers A and B were experimentally characterized, providing a gain of 2.48 V/V with a 60 mV power supply. The oscillators operate with the lowest reported supply voltage of only 60 mV while providing temperature and long-term stability competitive with respect to state-of-the-art ultra-low-voltage crystal oscillators. Oscillator A exhibits a power consumption in line with the best state-of-the-art oscillators previously reported.

APPENDIX A
PIERCE CRYSTAL OSCILLATOR OPERATION

The impedance Z_C shown in Fig. 6b can be expressed as [11]

$$Z_C = \frac{Z_1Z_3 + Z_2Z_3 + G_mZ_1Z_2Z_3}{Z_1 + Z_2 + Z_3 + G_mZ_1Z_2}, \tag{7}$$

where Z_1, Z_2 and Z_3 are the impedances of capacitors C_1, C_2 and C_3, respectively. The imaginary part of Z_C is negative, since it is a purely capacitive impedance. The real part of Z_C is negative, provided that G_m has positive values, and is equal to $-R_m$ when the critical condition for oscillation is reached at G_{mcrit}

$$G_{mcrit} = \omega^2 C_1C_2R_m\left(1 + \frac{C_3}{C_1} + \frac{C_3}{C_2}\right)^2. \tag{8}$$

Equation (8) is valid as long as [11]

$$2\omega R_mC_3(1 + C_3/C_1 + C_3/C_2) \ll 1. \tag{9}$$

It will be verified that the design complies with this condition.

On the other hand, G_{mopt} is the transconductance value required to achieve the maximum negative resistance possible, and is given by

$$G_{mopt} = \omega\left(C_1 + C_2 + \frac{C_1C_2}{C_3}\right). \tag{10}$$

It will be verified that even though $G_m = 3 \times G_{mcrit}$, it is smaller than G_{mopt}. The determination of G_m must also compensate the losses in the inverting amplifier. These losses are not negligible at low supply voltages.

The real part of Z_C, R_C, increases by the amount ΔR_C due to the losses in G_o

$$\Delta R_C = \frac{G_o}{(\omega C_2)^2\left(1 + \frac{C_3}{C_1} + \frac{C_3}{C_2}\right)^2}. \tag{11}$$

Assuming small losses, $G_o \ll \omega C_2$, and based on (8) and (11), the increase in G_{mcrit} needed to compensate G_o is

$$\Delta G_m = \frac{C_1}{C_2}\,G_o. \tag{12}$$

APPENDIX B
TRANSCONDUCTANCES OF THE SCHMITT TRIGGER

The expressions for the equivalent transconductance and the output conductance of the Schmitt trigger are [13]

$$G_m = \left.\frac{i_o}{v_i}\right|_{V_I=V_O=V_{DD}/2} = -2 \times \frac{g_{m1}(g_{ms2}+g_{md0}) + g_{ms1}g_{m0}}{g_{ms1}+g_{ms2}+g_{md0}}, \quad (13)$$

and

$$G_o = \left.\frac{i_o}{v_o}\right|_{V_I=V_O=V_{DD}/2} = -2 \times \frac{g_{md1}(g_{ms2}+g_{md0}) - g_{ms1}g_{m2}}{g_{ms1}+g_{ms2}+g_{md0}}. \quad (14)$$

where the transconductances are given in Table I of [15] and the subscript number correspond to the transistor number in Fig. 1.

The equivalent transconductance G_m can be rewritten in terms of the supply voltage, V_{DD}, and the current strengths, I_0, I_1 and I_2, as follows

$$G_m = \frac{2\,I_1/n}{e^{-V_{DD}/2n\phi_t}} \left[\frac{(I_0+I_2)e^{-V_{DD}/2\phi_t} - I_2 e^{-V_{X0}/\phi_t}}{I_0\, e^{(V_{X0}-V_{DD})/\phi_t} + I_1 + I_2} \right], \quad (15)$$

where

$$e^{-V_{X0}/\phi_t} = \frac{I_0 + I_1 e^{-V_{DD}/2\phi_t} + I_2 e^{-V_{DD}/\phi_t}}{I_0+I_1+I_2}. \quad (16)$$

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