Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits

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2004

Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits

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Abstract—This paper presents several architectures and designs of low-power 4-2 and 5-2 compressors capable of operating at ultra low supply voltages. These compressor architectures are anatomized into their constituent modules and different static logic styles based on the same deep submicrometer CMOS process model are used to realize them. Different configurations of each architecture, which include a number of novel 4-2 and 5-2 compressor designs, are prototyped and simulated to evaluate their performance in speed, power dissipation and power-delay product. The newly developed circuits are based on various configurations of the novel 5-2 compressor architecture with the new carry generator circuit, or existing architectures configured with the proposed circuit for the exclusive OR (XOR) and exclusive NOR (XNOR) [XOR–XNOR] module. The proposed new circuit for the XOR–XNOR module eliminates the weak logic on the internal nodes of pass transistors with a pair of feedback PMOS–NMOS transistors. Driving capability has been considered in the design as well as in the simulation setup so that these 4-2 and 5-2 compressor cells can operate reliably in any tree structured parallel multiplier at very low supply voltages. Two new simulation environments are created to ensure that the performances reflect the realistic circuit operation in the system to which these cells are integrated. Simulation results show that the 4-2 compressor with the proposed XOR–XNOR module and the new fast 5-2 compressor architecture are able to function at supply voltage as low as 0.6 V, and outperform many other architectures including the classical CMOS logic compressors and variants of compressors constructed with various combinations of recently reported superior low-power logic cells.

Index Terms—4-2 compressors, 5-2 compressors, arithmetic circuits, digital multipliers.

I. INTRODUCTION

THE semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. As the CMOS process technology shrinks, the unity gain cutoff frequency, f_T of the transistors become comparable with that of the GaAs bipolar technology that it is now practical to design sub-1-V radio frequency integrated circuits (RFICs) based solely on the matured low cost, low-power CMOS process [17]. Front-end wireless communication circuitries, traditionally based on analog circuit techniques are

also being transferred into the digital domain to offer alluring power savings and high density integration by direct conversion architecture [4]. It is high time we explore the well-engineered deep sub-micron CMOS technologies to address the challenging criteria of these emerging low-power and high-speed communication digital signal processing chips. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. Microprocessors and digital signal processors rely on the efficient implementation of generic arithmetic logic units and floating point units to execute dedicated algorithms such as convolution and filtering [6],[10],[15], [16]. In most of these applications, multipliers have been the critical and obligatory component dictating the overall circuit performance when constrained by power consumption and computation speed. At the circuit design level, considerable potential for optimizing the power-delay product of the multiplier exists by voltage scaling and through the use of contemporary and new CMOS logic styles for the implementation of its embraced combinational circuits [13]–[15], [19].

A fast array or tree multiplier is typically composed of three subcircuits: a Booth encoder for the generation of a reduced number of partial products; a carry save structured accumulator for a further reduction of the partial products' matrix to only the addition of two operands; and a fast carry propagation adder (CPA) [9] for the computation of the final binary result from its stored carry representation. Among these subcircuits, the second stage of partial product accumulation, often referred to as the carry save adder (CSA) tree [5], [6], [8], [10], [12], [18], occupies a high fraction of silicon area, contributes most to the overall delay, and consumes significant power. Therefore, speeding up the CSA circuit and lowering its power dissipation are crucial to sustain the performance of the multiplier to stay competitive. Early designs of CSA tree used the Dadda's column compression technique [18] with the 3-2 counters, or equivalently the full adders to reduce the partial product matrix. To lower the latency of the partial product accumulation stage, 4-2 and 5-2 compressors have been widely employed nowadays for high speed multipliers. Owing to its regular interconnection, the 4-2 compressor is ideal for the construction of regularly structured Wallace tree with low complexity [12], [18]. Several 4-2 compressor circuits have been proposed for low-power applications [3], [5], [7], [8], [10], [12]. Some of these are able to operate at low supply voltages but require excessive number of transistors due to their complementary CMOS structures, others use smaller number of transistors but fail to function at ultra low voltages, or lack the driving capability to drive the next level of

Fig. 1.   A 4-2 compressor.

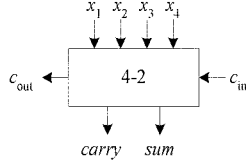Fig. 2.   Conventional 4-2 compressor—4Δ.

Fig. 3.   Logic level optimized CMOS 4-2 compressor.

subcircuits. The insertion of additional buffers for every output ports to provide the output drive increases the switching activities and hence the power dissipation. Higher input compressors have also been studied by researchers [2], [6], [8], [10] and fast 5-2 compressors have been increasingly employed in large word-size multiplier and high precision multiply-accumulators [5], [6], [12]. Most of the research on high-input compressors focuses on the optimization of circuit structure for high speed applications at standard supply voltages. With trends in VLSI toward deep-submicrometer technology, circuits operating reliably at sub-1 V will soon become a reality. This is because the materials used to form the transistors cannot withstand an electric field of unlimited strength, and as transistors get smaller, the field strength increases if the supply voltage is held constant. Since supply voltage has a quadratic contribution to the power dissipation, lowering the supply voltage is also a lucid means of reducing power consumption. However, the major problem with reducing the supply voltage is that the speed of the circuits is also degraded. Therefore, there is a strong impetus to renew the full custom arithmetic cells to achieve high power efficiency for VLSI circuits operating at ultra low supply voltages.

In this paper, we explore new design methodologies for low-power 4-2 and 5-2 compressor circuits that possess sufficient drivability at ultra low voltages based on the advanced CMOS process technology. By investigating the performances of several fast 4-2 and 5-2 compressor architectures and their underlining building modules, a new composite exclusive OR (XOR) and exclusive NOR (XNOR) [XOR–XNOR] cell is proposed. The 4-2 compressors constructed around the proposed XOR–XNOR cell exhibit superior power efficiency comparing to other configurations of the same architecture. A new fast 5-2 compressor architecture is proposed, together with a new circuit for its carry generator module. This new architecture performs well with almost any configuration of logic styles and its overall performance is the best among the known 5-2 compressor architectures under a realistic simulation environment that truly reflects its actual operability in a tree-structured multiplier.

II. THE 4-2 COMPRESSOR

A. 4-2 Compressor Architectures

A 4-2 compressor has five inputs and three outputs, as shown in Fig. 1. The four inputs x_1, x_2, x_3, and x_4, and the output sum have the same weight. The output carry is weighted one binary bit order higher. The 4-2 compressor receives an input c_{in} from the preceding module of one binary bit order lower in significance, and produces an output c_{out} to the next compressor module of higher significance. Different structures of
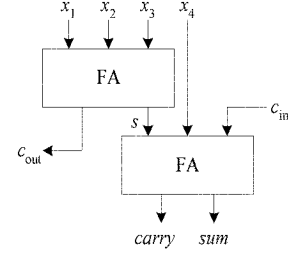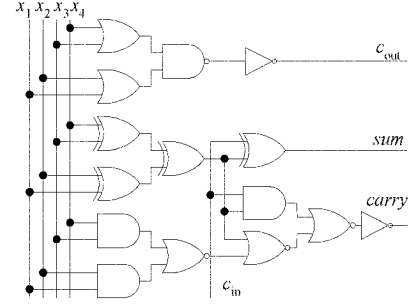
4-2 compressors exist and they all have to abide by the fundamental equation given as follows:

$$x_1 + x_2 + x_3 + x_4 + c_{\text{in}} = \text{sum} + 2 \cdot (\text{carry} + c_{\text{out}}). \quad (1)$$

Besides, to accelerate the carry save summation of the partial products, it is imperative that the output, c_{out} be independent of the input c_{in}.

The conventional implementation of a 4-2 compressor is composed of two serially connected full adders, as shown in Fig. 2. At gate level, high input compressors are anatomized into XOR gates and carry generators normally implemented by multiplexers (MUX). Therefore, different designs can be classified based on the critical path delay in terms of the number of primitive gates. Let Δ_{XOR} denote the delay of an XOR gate and Δ_{CGEN} denote the delay of a carry generator. A compressor is said to have a delay of $(m\Delta_{\text{XOR}} + n\Delta_{\text{CGEN}})$ if its critical path consists of m XOR gates and n carry generators. Since the difference between the delays of widely used XOR gate and carry generator is trivial in an optimized design, the delay of the compressor is more commonly specified as $(m + n)\Delta$. Therefore, the straightforward implementation of a 4-2 compressor of Fig. 2 has a long critical path delay of 4Δ [5]. Additionally, due to the uneven delay profiles of the outputs arriving from different input paths, the CSA tree for the partial product accumulation constructed from such cells tends to generate a lot of glitches.

A 4-2 compressor flattened and optimized at gate level to reduce the critical path delay is shown in Fig. 3 [12]. It uses more than 80 transistors when implemented in conventional or complementary CMOS logic style. As this circuit is capable of functioning below 1 V, it is used as a benchmark for evaluating the performance of other low voltage and low-power 4-2 compressor circuits.
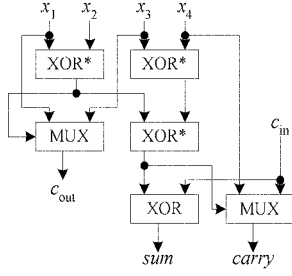
Fig. 4.   Logic decomposition of 4-2 compressor—3Δ.

A recent design of 4-2 compressor [3], [7], [10], [12] is derived from the modified equations for the functions of Fig. 2. The three outputs of the design are described as follows:

$$c_{\text{out}} = (x_1 \oplus x_2) \cdot x_3 + x_1 \cdot x_2 = (x_1 \oplus x_2) \cdot x_3$$
$$+ \overline{(x_1 \oplus x_2)} \cdot x_1 \qquad (2)$$

$$s = x_1 \oplus x_2 \oplus x_3 \qquad (3)$$

$$\text{sum} = s \oplus x_4 \oplus c_{\text{in}} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus c_{\text{in}} \qquad (4)$$

$$\text{carry} = (s \oplus x_4) \cdot c_{\text{in}} + s \cdot x_4$$
$$= (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \cdot c_{\text{in}}$$
$$+ \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4)} \cdot x_4. \qquad (5)$$

The two carry signals carry and c_{out} are generated from both the XOR and XNOR functions of the input signals. The sum output is generated by several two-input XOR circuits, some internal signals of which can be used to generate the two carries. Fig. 4 shows the logic decomposition of this 4-2 compressor architecture. It is mainly composed of six modules, four of which are XOR circuits and the other two are 2-1 MUX. Three special XOR–XNOR modules marked with "XOR^*" generate both the XOR and XNOR signals simultaneously to other modules driven by them. This design has a critical path delay of 3Δ, which is 1Δ delay shorter than the conventional implementation. Besides, its outputs feature balanced signal arrival time from each data inputs (x_1 to x_4), thanks to the special "XOR^*" modules.

B. Circuit Implementations of Building Block Modules

There are several designs [1], [11]–[15] of the XOR^* modules, as shown in Fig. 5, for implementing the 4-2 compressor of Fig. 4. As both the XOR and XNOR functions are required in the carry generation circuits, circuits capable of co-generating these two signals, as depicted in Fig. 5, are beneficial to the implementation of the special XOR^* modules of Fig. 4. Although there is no need for the XOR^* module with inputs of x_3 and x_4 to provide the XNOR output, the same structure as other XOR^* modules is still preferred in order to avoid skewed delay paths. In Fig. 5, the numerical values next to the transistors are the channel widths in μm. Minimum feature size is assumed for the channel lengths of the transistors based on the latest Chartered Semiconductor CSM 0.18-μm CMOS process technology.

The design of Fig. 5(a) has the least number of transistors and consumes very low power [13]–[15]. However, it generates a weak logic "1" at the XNOR node when the primary inputs are both '1's, which prevents it from functioning reliably at low
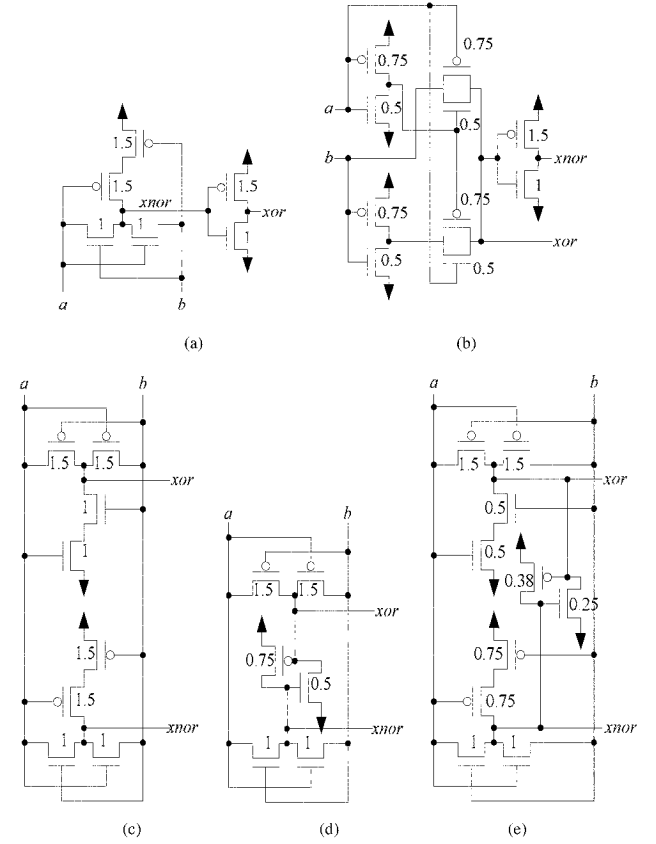

Fig. 5.   Implementations of the XOR^* module.

supply voltage. The design of Fig. 5(b) is able to operate at low voltage, but it is not power efficient [13]–[15]. Both designs [Fig. 5(a) and (b)] use inverter to generate the complementary XOR and XNOR signals, therefore, their outputs skew heavily in time.

The design of Fig. 5(c) consists of two cross-backed XOR and XNOR cells [13]–[15]. It is able to generate the complementary XOR and XNOR outputs simultaneously. However, it performs non full-swing operations for some input patterns causing their corresponding outputs to be degraded by 1 V_{th}. For example, the XNOR output transmits a weak logic "1" when both inputs are "1"s, whereas the XOR output transmits a weak logic "0" when both inputs are "0"s. When the power supply voltage is lower than 1 V, the week logic transmission will slow down the charging and discharging speed of the driven circuits, or worse, unable to turn on or off the driven transistors as desired. Therefore, it is also not a suitable candidate for ultra low-voltage operation.

The combined XOR–XNOR cell of Fig. 5(d) was proposed in [11], [12]. It is a low-power circuit with the least number of transistors that can output XOR and XNOR concurrently. It eliminates the transmission of weak logic for certain input patterns by virtue of the feedback PMOS–NMOS transistors in the midst of the circuit. Nevertheless, it is still not suitable for low-voltage applications for the following reason. When the inputs change from any other pattern to "00" or "11," the feedback transistors that were turned off originally will be turned on by both a weak logic driver and a high impedance driver. This transition takes
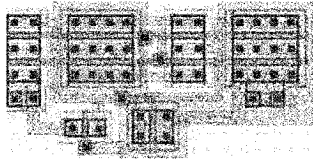
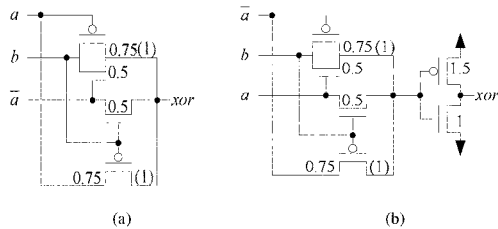Fig. 6.   Layout of the proposed circuit of Fig. 5(e) for the XOR^* module.

Fig. 7.   Implementations of the XOR module.

Fig. 8.   Implementations of the carry generator module using MUX.

a long time at very low voltage slightly above $2\,V_{\mathrm{thp}}$. Meanwhile, the short-circuit current of the following stage increases tremendously, which lead to a rise in the power dissipation.

We proposed a new circuit for the XOR^* module, as shown in Fig. 5(e), which is able to generate the XOR and XNOR outputs simultaneously, too. A pair of feedback PMOS-NMOS transistors is added to the XOR–XNOR circuit of Fig. 5(c). It eliminates the weak logic problem encountered by the former circuit when the input pattern is "00" or "11." It is able to operate at even lower voltage than Fig. 5(d) because the pairs of serially connected PMOS transistors and serially connected NMOS transistors ensure full-swing logic during the input transitions to "00" and "11". Hence, the proposed circuit is rather robust against delay driven voltage scaling. Fig. 6 shows the layout of the proposed new circuit module.

The last XOR module to generate the sum output of Fig. 4 does not need to provide the XNOR output, but it should provide sufficient output current to drive the next stage of 4-2 compressors. Fig. 7 shows two possible XOR gate designs for this simple XOR module [13]–[15]. Fig. 7(a) is a low-power design of XOR function. But the limited drivability prevents it from being used as an output module in a 4-2 compressor. Fig. 7(b) is an XNOR circuit followed by an inverter, which has stronger driving capability than Fig. 7(a). Therefore, Fig. 7(b) is used in our proposed 4-2 compressor to generate the sum signal. As mentioned earlier, the numbers beside the transistors are the optimized channel widths. As some transistors have different optimized sizes for different compressors, the numbers in brackets are the sizes of the transistors optimized for 5-2 compressors, which will be discussed next.

The carry generator modules produce the signals carry and c_{out}, which are usually generated by MUX. Several designs are shown in Fig. 8. Fig. 8(a) is widely used in low-power full adder cells [13]–[15]. However, its driving capability is somewhat limited, which causes signal decay when many stages are to be cascaded. So it is not suitable for use in the 4-2 compressors of the CSA tree. Fig. 8(b) improves the driving capability by adding an output buffer at the expense of increasing its power dissipation [13]–[15]. The output buffer formed by the cascaded inverters is
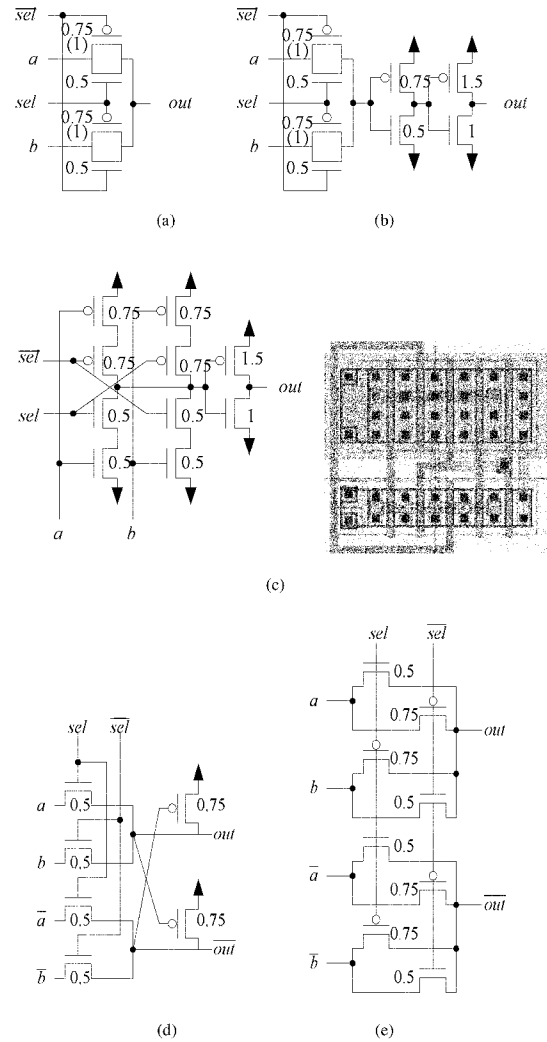
designed such that the first inverter is half the size of the output inverter in order to cut down the power dissipation.

The circuit of Fig. 8(c) is a MUX implemented in standard complementary CMOS logic style [3], [19]. Being a complementary CMOS circuit, it is robust against both voltage scaling and transistor sizing. Despite having one inverter lesser than the design of Fig. 8(b), this circuit still delivers sufficient drive to its succeeding circuits through the output inverter. The total number of transistors of this circuit is ten. Although it is two more than that of Fig. 8(b), the silicon areas occupied by both circuits are almost the same. This is because Fig. 8(b) requires more space to segregate the different diffusion areas, which increases the routing complexity of the interconnecting lines. The regularity of the layout of the circuit of Fig. 8(c) is evident from the diagram on its right. The MUX circuits of Fig. 8(d) and Fig. 8(e) are implemented in complementary pass transistor logic (CPL) and dual pass transistor logic (DPL) styles, respectively [10], [19]. Because they are dual-rail circuits, complementary pairs of primary inputs and outputs need to be generated. Although they can generate full-swing outputs, due to the pass transistor structure, they will not provide adequate drivability if many such circuits are cascaded, particularly at
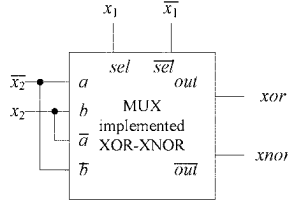
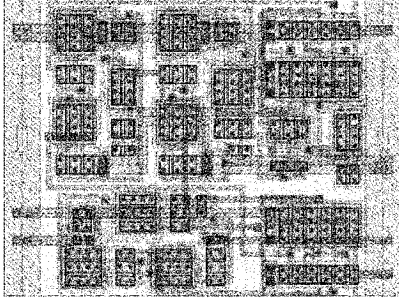Fig. 9. Implementation of the XOR–XNOR module with CPL and DPL MUX.

Fig. 10. Layout of the new 4-2 compressor using the proposed XOR–XNOR cell.
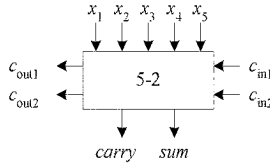

Fig. 11. A 5-2 compressor.

Fig. 12. A 5-2 compressor based on cascaded full adders—6Δ.

Fig. 13. A 5-2 compressor architecture—5Δ.

low supply voltage. Therefore, if these circuits are used at the output ports of the compressor, output buffers are required to strengthen the signals. Fig. 9 shows the use of a dual-rail MUX to construct the XOR–XNOR module, which can be used for the fully multiplexer-based implementation of the compressor [10].

The layout of the proposed new 4-2 compressor based on the novel XOR–XNOR cell of Fig. 5(e) is shown in Fig. 10. It occupies a silicon area of $22\ \mu\mathrm{m} \times 17\ \mu\mathrm{m}$.
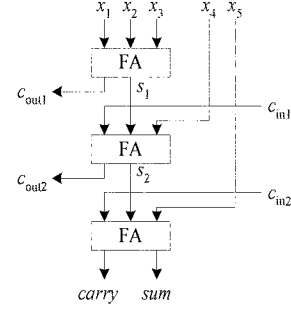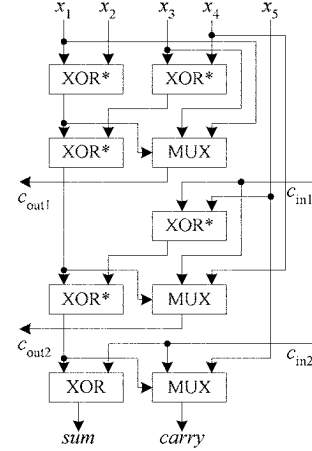
III. 5-2 COMPRESSOR

A. 5-2 Compressor Architectures

The 5-2 compressor is another widely used building block for high precision and high speed multipliers. The block diagram of a 5-2 compressor is shown in Fig. 11, which has seven inputs and four outputs. Five of the inputs are the primary inputs x_1, x_2, x_3, x_4 and x_5, and the other two inputs, c_{in1} and c_{in2} receive their values from the neighboring compressor of one binary bit order lower in significance. All the seven inputs have the same weight. The 5-2 compressor generates an output sum of the same weight as the inputs, and three outputs carry, c_{out1}, and c_{out2} weighted one binary bit order higher. The outputs, c_{out1} and c_{out2} are fed to the neighboring compressor of higher significance. All the 5-2 compressors of different designs abide by (6)

$$x_1 + x_2 + x_3 + x_4 + x_5 + c_{\mathrm{in1}} + c_{\mathrm{in2}}$$
$$= \mathrm{sum} + 2 \cdot (\mathrm{carry} + c_{\mathrm{out1}} + c_{\mathrm{out2}}). \quad (6)$$

Besides, to speed up the carry save summation of the partial products, the output c_{out1} must be independent of the inputs c_{in1}

and c_{in2}, and the output c_{out2} must be independent of the input c_{in2}.

A simple implementation of the 5-2 compressor is to cascade three full adders in a hierarchical structure, as shown in Fig. 12, which has a critical path delay of 6Δ.

Fig. 13 shows a modified architecture of the 5-2 compressor [10], which has a critical path delay of 5Δ. The XOR* modules in the figure generate both the XOR and XNOR signals simultaneously, as described in Section II. The style and structure of the circuit share some common attributes as the recently published structural design of full adders [10], [11], [13]–[15] and 4-2 compressors [3], [10], [12].

In spite of the structural differences between the implementations of Fig. 12 and Fig. 13, the formulas to generate the output signals are essentially derived from the same basic architecture of Fig. 12. Each full adder can be logically expressed as

$$s_{\mathrm{FA}} = a \oplus b \oplus c \quad (7)$$
$$c_{\mathrm{FA}} = (a \oplus b) \cdot c + \overline{(a \oplus b)} \cdot a \quad (8)$$

where a, b, and c are the primary inputs, and s_{FA} and c_{FA} are the primary outputs of the full adder.

It follows that the outputs and the internal nodes of Fig. 12 can be expressed by the following set of equations:

$$s_1 = x_1 \oplus x_2 \oplus x_3 \quad (9)$$
$$c_{\mathrm{out1}} = (x_1 \oplus x_2) \cdot x_3 + \overline{(x_1 \oplus x_2)} \cdot x_1 \quad (10)$$
$$s_2 = s_1 \oplus x_4 \oplus c_{\mathrm{in1}}$$
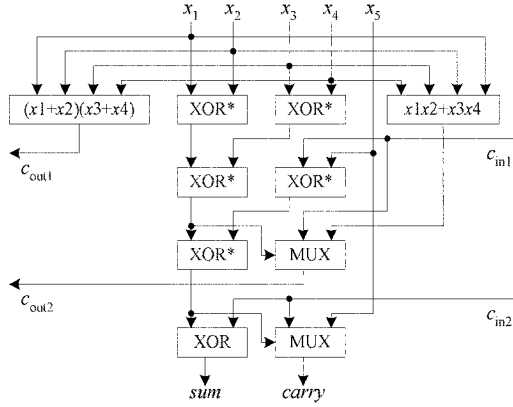$$= x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus c_{\mathrm{in1}} \quad (11)$$

Fig. 14.   A 5-2 compressor architecture—4Δ.

$$c_{out2} = (x_4 \oplus s_1) \cdot c_{in1} + \overline{(x_4 \oplus s_1)} \cdot x_4$$
$$= (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \cdot c_{in1}$$
$$+ \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4)} \cdot x_4 \tag{12}$$
$$\text{sum} = s_2 \oplus x_5 \oplus c_{in2}$$
$$= x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1} \oplus c_{in2} \tag{13}$$
$$\text{carry} = (x_5 \oplus s_2) \cdot c_{in2} + \overline{(x_5 \oplus s_2)} \cdot x_5$$
$$= (x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1}) \cdot c_{in2}$$
$$+ \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1})} \cdot x_5. \tag{14}$$

A faster 5-2 compressor proposed in [6] is shown in Fig. 14. This architecture uses a different method to generate the outputs, c_{out1} and c_{out2}. Although this architecture produces different output bit patterns in c_{out1} and c_{out2} for the same input data, it still abides by (6). It is claimed to have a delay of 4Δ.

Equations (15)–(18) show the output functions

$$\text{sum} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1} \oplus c_{in2} \tag{15}$$
$$c_{out1} = (x_1 + x_2) \cdot (x_3 + x_4) \tag{16}$$
$$c_{out2} = \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4)} \cdot (x_1 \cdot x_2 + x_3 \cdot x_4)$$
$$+ (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \cdot c_{in1} \tag{17}$$
$$\text{carry} = \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1})} \cdot x_5$$
$$+ (x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1}) \cdot c_{in2}. \tag{18}$$

We proposed a new and faster architecture with the same theoretical critical path delay of 4Δ. The structure of our 5-2 compressor is shown in Fig. 15(a). It uses one less module than the 5-2 compressor of Fig. 14. The mechanisms for generating the carry output signals, such as carry, c_{out1}, c_{out2}, are fundamentally different from those of the existing architectures. The carry generator CGEN1 is used to produce the signal c_{out1}. In anticipation that this carry generator is most likely to be situated in the longest delay path in the tree structured multiplier, it is implemented as a complex gate fed only with the primary inputs. Although several more transistors are used, the speed of this carry generator is faster than that controlled by a XOR^* module. The other two carry generators CGEN2 which are used to produce the carry and c_{out2}, are still controlled by the corresponding XOR^* modules. Unlike CGEN1, one of the inputs to CGEN2

(a)

(b)
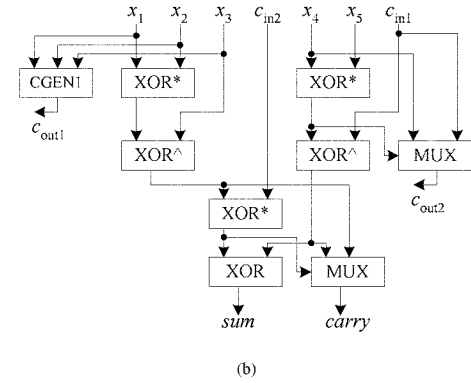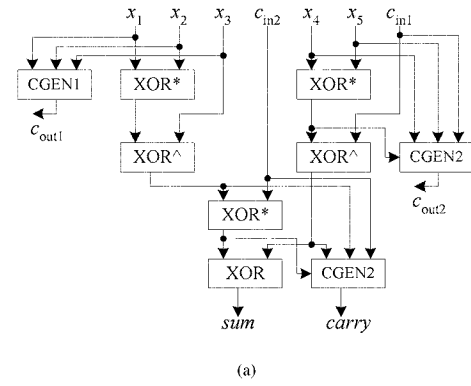
Fig. 15.   Proposed 5-2 compressor architecture—4Δ.

is either c_{in1} or c_{in2}, which comes from an output of the compressor of the preceding stage. Since these signals are often arrived later than the primary inputs, implementing CGEN2 with more costly complex gate as CGEN1 is not necessary as it will not help to reduce the critical path delay of the tree-structured multiplier any way.

The carry generators CGEN2 in Fig. 15(a) can also be implemented by MUX, as shown in Fig. 15(b). CGEN2 of Fig. 15(a) is better implemented in complementary CMOS logic style, which offers low capacitive loading to the driving XOR^* modules while the MUX-based carry generator modules of Fig. 15(b) is more suitable for realization with other logic styles.

The output functions of our proposed architecture in Fig. 15 are described by (19)–(22)

$$\text{sum} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus x_5 \oplus c_{in1} \oplus c_{in2} \tag{19}$$
$$c_{out1} = (x_1 + x_2) \cdot x_3 + x_1 \cdot x_2 \tag{20}$$
$$c_{out2} = (x_4 \oplus x_5) \cdot c_{in1} + x_4 \cdot x_5$$
$$\equiv (x_4 \oplus x_5) \cdot c_{in1} + \overline{(x_4 \oplus x_5)} \cdot x_4 \tag{21}$$
$$\text{carry} = ((x_1 \oplus x_2 \oplus x_3) \oplus (x_4 \oplus x_5 \oplus c_{in1})) \cdot c_{in2}$$
$$+ (x_1 \oplus x_2 \oplus x_3) \cdot (x_4 \oplus x_5 \oplus c_{in1})$$
$$\equiv ((x_1 \oplus x_2 \oplus x_3) \oplus (x_4 \oplus x_5 \oplus c_{in1})) \cdot c_{in2}$$
$$+ \overline{(x_1 \oplus x_2 \oplus x_3) \oplus (x_4 \oplus x_5 \oplus c_{in1})}$$
$$\cdot (x_1 \oplus x_2 \oplus x_3). \tag{22}$$

Based on the above formulas, it is conjectured that lowering the critical path delay of the 5-2 compressor to 3Δ or lower is almost impossible. However, it is very likely to explore different logic styles at transistor level to design significantly improved low-

Fig. 16. Implementations of the CGEN2 module.

Fig. 18. Layout of the proposed 5-2 compressor.

(a) *4-2 compressor simulation environment*

(b) *5-2 compressor simulation environment*

Fig. 19. Simulation environments. (a) 4-2 compressor simulation environment. (b) 5-2 compressor simulation environment.

(a)   (b)

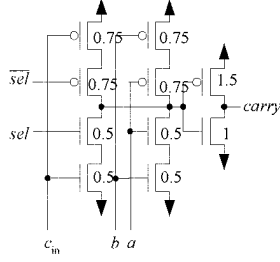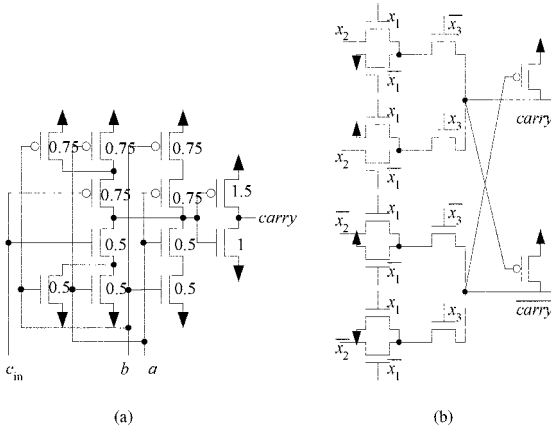Fig. 17. Implementations of the CGEN1 module.

power and high-speed 5-2 compressor cells for instantiation at architectural level. For example, a dual-rail 5-2 compressor [10] is proposed for the architecture of Fig. 4, where the XOR modules are implemented as dual-rail MUX to improve the performance.

B. Circuit Implementations of the Proposed 5-2 Compressor Architectures

The design of Fig. 5(e) is recommended for the implementation of XOR^* modules to allow low-voltage operation. The $XOR^\wedge$ modules do not need strong driving capability for the internal modules driven by them. Therefore, the design of Fig. 7(a) without the output buffer can be used for the $XOR^\wedge$ module. The sum output stage is implemented with the circuit of Fig. 7(b) to assure the drivability.

A new complementary CMOS logic style circuit, as shown in Fig. 16, is suggested for the implementation of the CGEN2 module. It resembles the circuit of Fig. 8(c), except that an additional input c_{in} is introduced and the original input a is rearranged. Comparing with the design of Fig. 8(c), this design lowers the switched capacitance of the preceding XOR^* module due to the reduction of its fanouts from 2 to 1 for both the XOR and XNOR outputs. It is also easier to layout without the cross lines of $\overline{sel}$ and sel.

The c_{out1} output of the CGEN1 module receives the primary inputs of x_1 to x_3 directly. It can be implemented with the carry generator circuit of the full adder in complementary CMOS logic style, which is shown in Fig. 17(a) [9], [19]. This circuit uses two more transistors than the circuit of Fig. 16, but it bypasses the XOR and XNOR signals from the preceding XOR^* module, which has prevented the delay of the c_{out1} generation from being degraded by about 1Δ. Fig. 17(b) shows the circuit for the CGEN1 module implemented in CPL logic style [19].
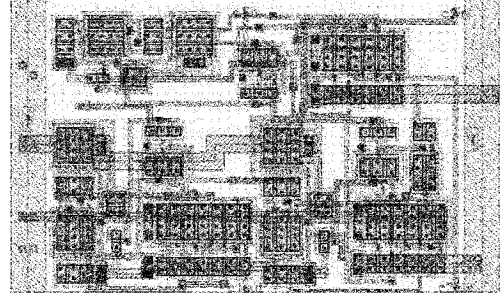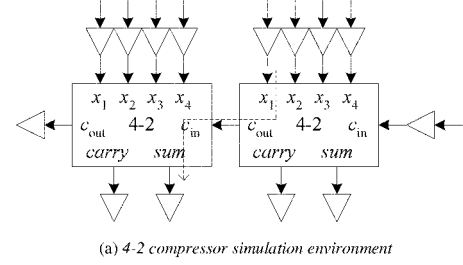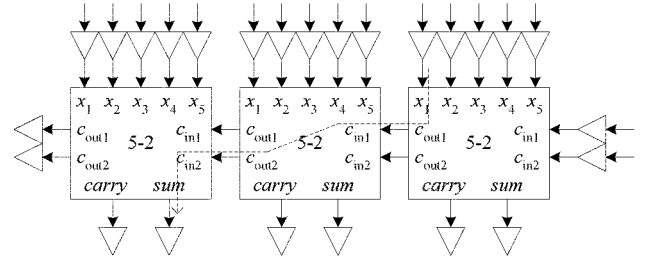
The complete layout of the proposed 5-2 compressor of 4Δ is shown in Fig. 18.

IV. SIMULATION RESULTS

A. Simulation Environment

The simulations are performed by Nassda HSIM 2.0 tool with the option "HSIMSPEED" set to "0." This option gives the slowest simulation time with the highest accuracy giving results compatible to HSPICE simulation. All the circuits and layouts are targeted for CSM 0.18-μm CMOS technology. Therefore, the circuits are designed and optimized based on this process model.

The simulation environments for the 4-2 compressor and 5-2 compressor circuits are shown in Fig. 19. Each input is driven by buffered signals and each output is loaded with buffers, which provide a realistic simulation environment reflecting the compressor operation in actual applications. The simulation environments for the 4-2 compressor and 5-2 compressor consist of two cascaded 4-2 compressors and three cascaded 5-2 compressors, respectively. These compressors are running in parallel to simulate an actual compressor stage in the CSA tree. More than one compressors are used in the simulation because the critical paths of some data patterns may cross adjacent compressors in the same stage of the CSA tree. The dashed lines in Fig. 19

TABLE I
CONFIGURATION OF SIMULATED 4-2 COMPRESSORS

S/N	Design	XOR*	XOR	MUX	Min. V_{DD} (V)
1	4-2_CMOS		3		0.6
2	4-2_a	5(a)	7(b)	8(b)	0.9
3	4-2_b	5(b)	7(b)	8(b)	0.6
4	4-2_c	5(c)	7(b)	8(b)	2.1
5	4-2_d	5(d)	7(b)	8(b)	0.8
6	4-2_e	5(e)	7(b)	8(b)	0.6
7	4-2_hybrid	5(e)	7(b)	8(c)	0.6
8	4-2_CPL	8(d) + 9	8(d) + 9	8(d)	0.6
9	4-2_DPL	8(e) + 9	8(e) + 9	8(e)	0.6

TABLE II
COMPARISON OF DELAY (NANOSECONDS) OF 4-2 COMPRESSORS

Delay(ns)	0.6V	0.7V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V	2.1V	2.5V	3.3V
4-2_CMOS	*6.29*	*3.18*	2.05	1.48	1.16	0.81	0.57	0.46	0.39	0.36	0.31
4-2_a			12.7	5.99	1.91	0.75	0.46	*0.36*	*0.30*	*0.26*
4-2_b	8.03	4.05	2.54	1.80	1.36	0.90	0.59	0.46	0.40	0.36	0.31
4-2_c								1.01	0.75	0.52
4-2_d			34.7	7.04	3.70	1.54	0.79	0.55	0.43	0.35	0.33
4-2_e	6.83	3.43	2.20	1.56	1.19	0.80	0.55	0.46	0.40	0.37	0.33
4-2_hybrid	7.11	3.72	2.43	1.74	1.36	0.93	0.66	0.54	0.47	0.42	0.35
4-2_CPL	*6.28*	*3.04*	*1.91*	*1.38*	*1.07*	*0.74*	*0.53*	*0.44*	0.39	0.35	0.32
4-2_DPL	6.74	3.32	*2.04*	*1.40*	*1.04*	*0.69*	*0.48*	*0.38*	*0.33*	*0.29*	*0.26*

TABLE III
COMPARISON OF POWER (MICROWATTS) OF 4-2 COMPRESSORS

Power(μW)	0.6V	0.7V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V	2.1V	2.5V	3.3V
4-2_CMOS	0.17	0.23	0.32	0.40	0.48	0.76	1.33	2.10	3.23	5.03	9.80
4-2_a				0.33	0.41	0.68	1.33	2.67	5.26	12.7	70.7
4-2_b	0.11	0.16	0.21	0.27	0.33	0.51	0.91	1.50	2.38	3.88	8.23
4-2_c								14.1	28.3	98.4
4-2_d			0.26	0.32	0.37	0.54	0.89	1.33	1.98	3.00	*6.03*
4-2_e	*0.11*	*0.15*	*0.20*	*0.26*	*0.31*	*0.48*	*0.82*	*1.26*	*1.89*	*2.94*	6.02
4-2_hybrid	*0.11*	*0.15*	0.21	0.26	0.32	0.49	0.84	*1.28*	*1.93*	*3.00*	6.14
4-2_CPL	0.13	0.18	0.23	0.29	0.36	0.57	0.96	1.50	2.34	3.62	7.86
4-2_DPL	0.12	0.16	*0.20*	*0.25*	*0.31*	*0.48*	*0.83*	1.30	2.03	3.46	8.41

TABLE IV
COMPARISON OF POWER EFFICIENCY (FEMTOJOULES) OF 4-2 COMPRESSORS

PDP (fJ)	0.6V	0.7V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V	2.1V	2.5V	3.3V
4-2_CMOS	1.05	0.74	0.65	0.60	0.56	0.62	0.76	0.96	1.27	1.81	3.04
4-2_a			4.19	2.45	1.29	0.99	1.22	1.89	3.82	18.4
4-2_b	0.92	0.64	0.54	0.49	0.45	0.46	0.54	0.69	0.95	1.38	2.51
4-2_c								14.2	21.2	51.2
4-2_d			9.06	2.22	1.36	0.84	0.70	0.73	0.86	*1.06*	*1.99*
4-2_e	*0.77*	*0.52*	0.45	0.41	*0.37*	*0.38*	*0.45*	*0.57*	*0.76*	1.08	*1.96*
4-2_hybrid	0.81	0.58	0.50	0.46	0.43	0.46	0.55	0.69	0.91	1.26	2.15
4-2_CPL	*0.79*	0.54	*0.44*	*0.40*	0.38	0.42	0.51	0.66	0.91	1.27	2.52
4-2_DPL	0.80	*0.53*	*0.42*	*0.35*	*0.32*	*0.33*	*0.40*	*0.49*	*0.67*	*1.00*	2.14

indicate the scenario of such potential critical paths. The left-most compressor of both simulation environments is inspected because it is most probable to have the longest delay. The delay is measured from the earliest input signal reaching 50% of the supply voltage to the latest output signal reaching 50% of the supply voltage for each input cycle. The worst case delay is the largest delay among all input data.

For each circuit, 1024 data are randomly generated by MATLAB to feed into the circuits as input stimuli. The circuits under test are simulated at various supply voltages, ranging from 0.6 to 3.3 V. Each supply voltage corresponds with one of two simulation frequencies (the rate at which data patterns are fed): supply voltages greater than 1.0 V operate at 100 MHz, while supply voltages less than or equal to 1.0 V operate at 10 MHz. It should be noted that the simulation frequency is not the maximum operating frequency of the compressors. In fact, the compressors simulated are capable of operating correctly at much higher frequency than the simulation frequency. The average power consumption of the leftmost compressor is measured for every supply voltage, with the power consumed by the additional buffers excluded from the average power consumption calculation.

B. Simulation Results of 4-2 Compressors

Nine different 4-2 compressor designs are simulated. The first circuit is a full complementary CMOS logic style implementation of Fig. 3, which is used as the benchmark for low-voltage operation. The second to the sixth compressors use the same architecture of Fig. 4, with the XOR modules implemented by the circuit of Fig. 7(b) and the MUX modules implemented by the circuit of Fig. 8(b). They differ mainly in the circuit implementation of the XOR^* modules. The XOR^* modules of these five compressors are respectively implemented by the circuits of Fig. 5(a) to Fig. 5(e). The seventh compressor is a hybrid design employing the circuit of Fig. 5(e) for its XOR^* modules, the circuit of Fig. 7(b) for its XOR modules, and the circuit of Fig. 8(c) as its MUX modules. The eighth and ninth compressors are implemented by CPL and DPL logic styles, using the circuits of Figs. 8(d) and 9, and Fig. 8(e) and 9, respectively as their building blocks. The configurations of the nine compressors are listed in Table I. For brevity, only the figure numbers of the circuits, e.g. 5(a) instead of Fig. 5(a), are shown in the table. The last column in Table I shows the lowest operable

voltage for each 4-2 compressor obtained from the simulation, below which the circuit fails to function correctly. The full simulation results for the performance of all the compressors at different supply voltages are tabulated in Tables II–IV. The power efficiency, or the power-delay product (PDP) measured in fJ is defined as the product of the worst-case delay and the average power consumption. This metric provides an indication of the
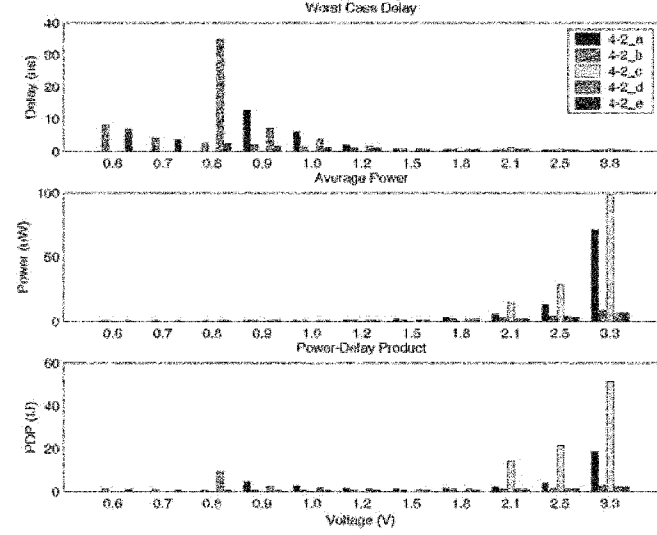
Fig. 20.   Performances of 4-2 compressors (Designs 2–6).

TABLE V
CONFIGURATIONS OF SIMULATED 5-2 COMPRESSORS

S/N	Design	Architecture	XOR*	XOR, XOR^	MUX, CGEN
1	**5del_bbb**	13	5(b)	7(b)	8(b)
2	**5del_ebb**	13	5(e)	7(b)	8(b)
3	**5del_hybrid**	13	5(e)	7(b)	8(c)
4	**5del_cpl**	13	8(d) + 9	8(d) + 9	8(d)
5	**5del_dpl**	13	8(e) + 9	8(e) + 9	8(e)
6	**kwon_bbb**	14	5(b)	7(b)	8(b)
7	**kwon_ebb**	14	5(e)	7(b)	8(b)
8	**kwon_ebc**	14	5(e)	7(b)	8(c)
9	**kwon_cpl**	14	8(d) + 9	8(d) + 9	8(d)
10	**4del_bbb**	15(b)	5(b)	7(b), 7(a)	17(a), 8(b)
11	**4del_ebb**	15(b)	5(e)	7(b), 7(a)	17(a), 8(b)
12	**4del_hybrid**	15(a)	5(e)	7(b), 7(a)	17(a),16
13	**4del_cpl**	15(b)	8(d) + 9	8(d) + 9	17(b), 8(d)

respectively the CMOS, CPL and DPL logic styles have comparatively shorter worst-case delay. However, they and Design 3 dissipate notably higher power than Designs 6 and 7, which use our proposed XOR^* cell of Fig. 5(e). For example, Design 8 (CPL) consumes 12.7% more power at 0.6 V than Design 6 (4-2_e). The average power consumption exacerbates with increasing supply voltages to a surplus of 14.9% at 1.0 V, 19.0% at 1.8 V and 30.5% at 3.3 V. The power efficiency (PDP) of Designs 6 and 7 are comparable to those circuits implemented in CPL and DPL styles. Both CPL and DPL logic styles require the generation of dual-rail signals for each primary input and output, incurring almost twice as many interconnecting lines as the other designs. Taking into account the substantial capacitive load due to the wiring overhead, Design 8 and 9 will not be competitive for the implementation of 4-2 compressors in large parallel multipliers.
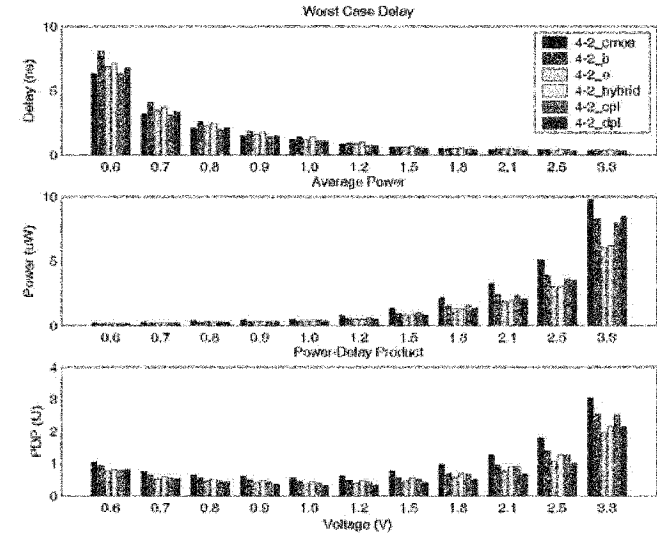

Fig. 21.   Performances of 4-2 compressors (Designs 1, 3, 6–9).

energy expended and the life span of the battery when the circuit is operating at its maximum speed. Two best performances at each supply voltage are highlighted in italic and bold print for ease of comparison.

To investigate the performance variations of the same 4-2 architecture due to different implementations of the XOR^* module, the worst case delay, power dissipation and power-delay product of Designs 2–6 are charted in Fig. 20. It is evident that the worst case delays at low supply voltages of Designs 2 and 5 are much longer than those of the other designs. Designs 2 and 4 consume more power. Consequently, Designs 3 and 6 perform significantly better than the other designs in terms of the power efficiency. In fact, these are the only two designs of Fig. 20 that are able to operate down to 0.6 V. The circuits used to implement the XOR^* modules for Designs 3 and 6 are respectively, Fig. 5(b) and our proposed Fig. 5(e).

The worst case delay, power dissipation and power-delay product of all designs capable of functioning down to the lowest supply voltage of 0.6 V, including our proposed hybrid 4-2 compressor are charted in Fig. 21. Designs 1, 8 and 9 featuring

C. Simulation Results of 5-2 Compressors

Thirteen different 5-2 compressor designs are simulated. These selected designs are all operable from 0.6 V to 3.3 V and their circuit configurations are tabulated in Table V. Each design is named according to its base architecture and a postfix indicating the types of circuits employed for the three constituent modules. For example, the name 5del_ebb of Design 2 implies that it is a 5Δ 5-2 compressor constructed by the circuits of Fig. 5(e), Fig. 7(b) and Fig. 8(b) for its XOR^*, XOR, and MUX modules, respectively. The first five designs are 5-2 compressors of 5Δ based on the architecture of Fig. 13. The four designs that followed are the 5-2 compressors of 4Δ based on the architecture of Fig. 14 proposed by Kwon *et al.* [6]. Designs 6–8 use the optimized complementary CMOS logic style to generate the OR–AND and AND–OR functions while Design 9 (kwon_cpl) generates these two functions with CPL logic style. The last four designs are the 5-2 compressors of 4Δ using the proposed architecture of Fig. 15. Designs 10, 11, and 13 use the circuits of Fig. 15(b) and Fig. 17(a) for the CGEN1 modules, and the circuit of Fig. 8(b) for the MUX modules. Design 12 is based on the architecture of Fig. 15(a), with a hybrid composition of optimally designed circuits of different

TABLE VI
COMPARISON OF DELAY (NANOSECONDS) OF 5-2 COMPRESSORS

Delay (ns)	0.6V	0.7V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V	2.1V	2.5V	3.3V
5del_bbb	11.42	5.72	3.58	2.52	1.91	1.26	0.84	0.68	0.59	0.52	0.45
5del_ebb	11.73	5.76	3.59	2.54	1.94	1.30	0.91	0.75	0.66	0.61	0.57
5del_hybrid	12.15	6.19	3.89	2.75	2.11	1.44	1.00	0.80	0.69	0.61	0.55
5del_cpl	*8.11*	*3.99*	*2.51*	*1.83*	*1.42*	*0.99*	*0.69*	*0.57*	*0.49*	*0.45*	0.41
5del_dpl	8.97	*4.35*	*2.65*	*1.83*	*1.37*	*0.92*	*0.64*	*0.52*	*0.45*	*0.39*	*0.35*
kwon_bbb	10.35	5.32	3.37	2.36	1.78	1.13	0.80	0.66	0.57	0.50	0.41
kwon_ebb	11.57	5.83	3.47	2.47	1.90	1.29	0.91	0.74	0.65	0.60	0.56
kwon_ebc	11.68	5.91	3.66	2.59	1.99	1.35	0.95	0.77	0.67	0.61	0.55
kwon_cpl	*8.92*	4.35	2.75	1.97	1.54	1.09	0.81	0.67	0.59	0.54	0.50
4del_bbb	12.33	6.11	3.78	2.63	2.01	1.34	0.91	0.73	0.62	0.55	0.46
4del_ebb	10.31	5.26	3.41	2.44	1.84	1.18	0.79	0.62	0.53	0.46	*0.39*
4del_hybrid	10.11	5.24	3.36	2.41	1.86	1.27	0.87	0.70	0.59	0.51	0.43
4del_cpl	10.14	4.66	2.92	2.07	1.62	1.11	0.80	0.66	0.57	0.51	0.47

TABLE VII
COMPARISON OF POWER (MICROWATTS) OF 5-2 COMPRESSORS

Power (μW)	0.6V	0.7V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V	2.1V	2.5V	3.3V
5del_bbb	0.22	0.29	0.40	0.51	0.62	0.95	1.71	2.73	4.25	6.93	15.15
5del_ebb	0.21	0.28	0.38	0.48	0.58	0.88	1.50	2.32	3.45	5.41	11.22
5del_hybrid	0.21	0.29	0.38	0.49	0.59	0.92	1.55	2.39	3.54	5.48	11.39
5del_cpl	0.22	0.30	0.39	0.50	0.60	0.93	1.55	2.42	3.64	5.79	12.23
5del_dpl	0.20	0.27	0.34	0.41	0.50	0.78	1.32	2.07	3.19	5.32	12.33
kwon_bbb	0.21	0.29	0.39	0.50	0.60	0.96	1.67	2.71	4.16	6.93	14.88
kwon_ebb	0.21	0.29	0.38	0.49	0.59	0.90	1.52	2.40	3.66	5.83	12.21
kwon_ebc	0.21	0.284	0.38	0.49	0.58	0.91	1.54	2.44	3.65	5.79	12.12
kwon_cpl	0.26	0.37	0.47	0.60	0.72	1.14	1.87	2.92	4.43	7.13	15.00
4del_bbb	0.17	0.23	0.31	0.40	0.49	0.76	1.33	2.13	3.30	5.36	11.33
4del_ebb	*0.15*	*0.21*	*0.28*	*0.36*	*0.43*	*0.68*	*1.14*	*1.78*	*2.70*	*4.35*	*9.02*
4del_hybrid	*0.15*	*0.21*	*0.28*	*0.36*	*0.43*	*0.67*	*1.14*	*1.76*	*2.69*	*4.31*	*9.05*
4del_cpl	0.23	0.32	0.42	0.53	0.66	0.99	1.70	2.68	4.03	6.34	13.67

TABLE VIII
COMPARISON OF POWER EFFICIENCY (FEMTOJOULES) OF 5-2 COMPRESSORS

PDP (fJ)	0.6V	0.7V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V	2.1V	2.5V	3.3V
5del_bbb	2.46	1.69	1.43	1.29	1.18	1.21	1.43	1.86	2.50	3.59	6.82
5del_ebb	2.47	1.64	1.36	1.22	1.12	1.15	1.37	1.73	2.29	3.29	6.37
5del_hybrid	2.59	1.80	1.50	1.36	1.26	1.33	1.54	1.90	2.42	3.32	6.25
5del_cpl	1.76	1.20	0.99	0.91	0.85	0.92	1.07	1.38	1.79	2.61	5.01
5del_dpl	1.75	1.16	0.90	*0.75*	*0.69*	*0.72*	*0.84*	*1.07*	*1.44*	*2.08*	4.32
kwon_bbb	2.18	1.56	1.32	1.19	1.08	1.09	1.33	1.78	2.36	3.45	6.15
kwon_ebb	2.42	1.66	1.32	1.20	1.11	1.17	1.38	1.78	2.38	3.49	6.83
kwon_ebc	2.43	1.68	1.39	1.26	1.16	1.23	1.45	1.87	2.46	3.51	6.70
kwon_cpl	2.35	1.60	1.30	1.19	1.10	1.25	1.52	1.97	2.62	3.88	7.44
4del_bbb	2.08	1.43	1.19	1.06	0.98	1.01	1.21	1.56	2.05	2.95	5.21
4del_ebb	*1.60*	*1.11*	*0.97*	0.88	*0.79*	*0.80*	*0.90*	*1.10*	*1.43*	*2.00*	*3.52*
4del_hybrid	*1.53*	*1.09*	*0.94*	*0.86*	*0.79*	0.85	0.99	1.22	1.59	2.20	*3.85*
4del_cpl	2.29	1.47	1.22	1.09	1.07	1.10	1.36	1.77	2.30	3.23	6.43
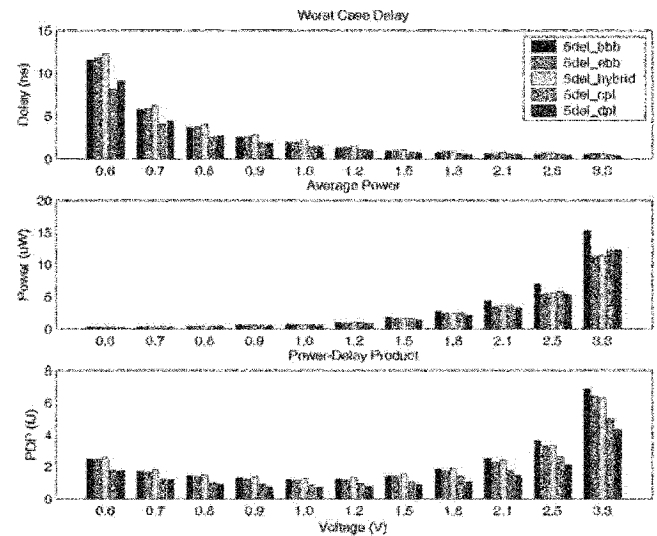
Fig. 22. Performances of 5-2 compressors (Designs 1–5).

logic styles. It uses the proposed XOR^* cell of Fig. 5(e), the pass-transistor style XOR gate of Fig. 7(b), the $XOR^\wedge$ circuit of Fig. 7(a), the complementary CMOS styled CGEN1 circuit of Fig. 17(a), and the CGEN2 circuit of Fig. 16. Design 13 (CPL) is based on the same architecture as Designs 10 and 11, but uses the circuits implemented in CPL logic style for the XOR^*, XOR, $XOR^\wedge$ and MUX modules. Its CGEN1 module is implemented with the CPL circuit of Fig. 17(b).

The simulation results of the delay, power and power efficiency of all the compressors are tabulated in Tables VI–VIII. Two best performances at each supply voltage are printed in bold and italic. The performances of all 5-2 compressors based on the 5Δ architecture are charted in Fig. 22 for comparison. The CPL (5del_cpl) and DPL (5del_dpl) designs have the best

worst case delay and power efficiency. Among the non dual-rail designs, 5del_bbb consumes more power and 5del_hybrid has the longest delay. Design 5del_ebb provides the best trade-off between delay, power and power efficiency among the three non dual-rail compressors. Considering all aspects of the performance, this architecture is best implemented with either CPL or DPL circuits.

Fig. 23 compares the performances of various 4Δ 5-2 compressors built upon the architecture proposed by Kwon et al. [6]. The design implemented with CPL circuits continues to perform well in delay than the non dual-rail designs as in the previous comparison but its overall performance is not necessary better than the others this time. The problem lies in its high power dissipation. Designs kwon_ebb and kwon_ebc consume about 2% to 18% lesser power than the other two designs, but they are slower too. In term of power efficiency, Design kwon_bbb
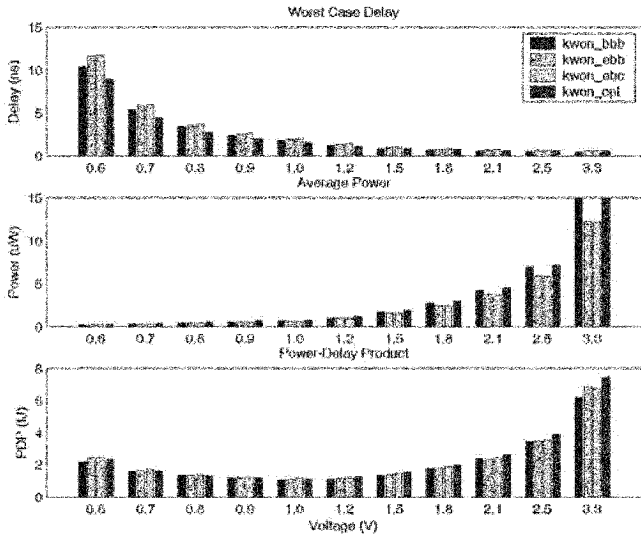
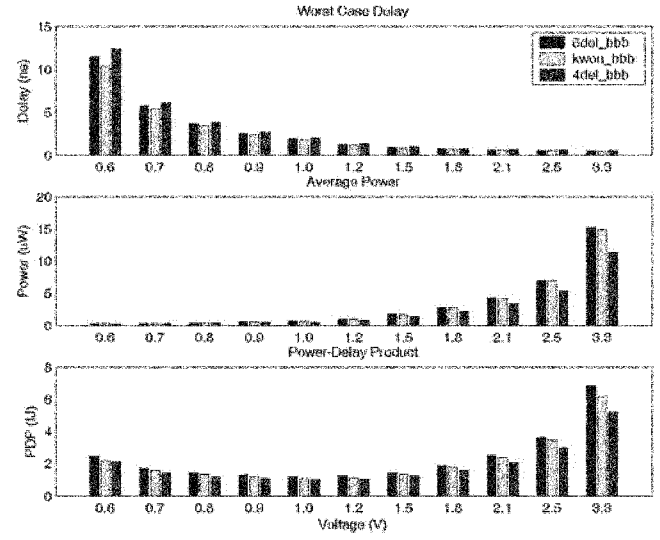Fig. 23.   Performances of 5-2 compressors (Designs 6–9).

Fig. 24.   Performances of 5-2 compressors (Designs 10–13).

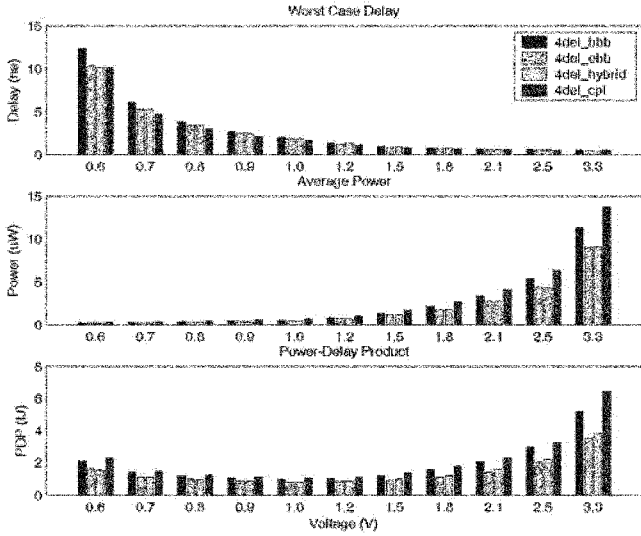Fig. 25.   Performance of different 5-2 compressor architectures with bbb configuration (Designs 1, 6, 10).

Fig. 26.   Performance of different 5-2 compressor architectures with ebb configuration (Designs 2, 7, 11).

outperforms the other two non-CPL designs, which have very similar performance.

Fig. 24 shows the performances of several circuits built around our proposed 4Δ 5-2 compressor architecture. Both 4del_ebb and 4del_hybrid outperform 4del_bbb and 4del_cpl remarkably. Their speeds are comparable to the circuit implemented with CPL logic style. They consume 32% to 35% lesser power than 4del_cpl and 10% to 20% lesser power than 4del_bbb. At voltage higher than 1.0 V, 4del_ebb has a slight edge over 4del_hybrid, whereas at voltage lower than 1.0 V, 4del_hybrid performs slightly better.

Performance differences due to architectural difference are also studied by comparing different compressor architectures using identical configuration for the same anatomized modules. The performances of three 5-2 compressor architectures with configurations of bbb, ebb, hybrid, and CPL are respectively charted in Figs. 25–28. Design 5del_dpl is also added to Fig. 28 for comparison. Our proposed architecture has the best performance among all architectures implemented with non dual-rail
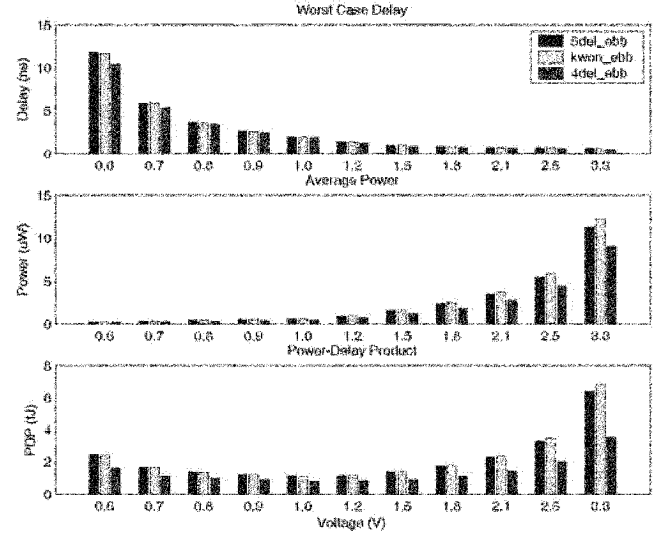
logic styles. For modules implemented with CPL or DPL logic style, the architecture of Fig. 13 is better.

Fig. 25 compares the architectures with bbb configuration. The results show that the average power of our proposed 4Δ architecture is 19% to 24% lesser than Kwon's architecture of Fig. 14, and 20% to 25% lesser than the 5Δ architecture of Fig. 13. Although it is slower, its power-delay product is still far lower than the other architectures.

Fig. 26 shows that, with the configuration ebb, both the average power and worst-case delay of our proposed 4Δ architecture are superior to Kwon's architecture and the 5Δ architecture. As a result, its power efficiency performance is 27% to 48% better than Kwon's and 28% to 45% better than the 5Δ architecture.

Fig. 27 shows that, with the hybrid configuration, our proposed 4Δ architecture consumes 25% to 28% lesser power than Kwon's architecture, and 20% to 29% lesser power than the 5Δ
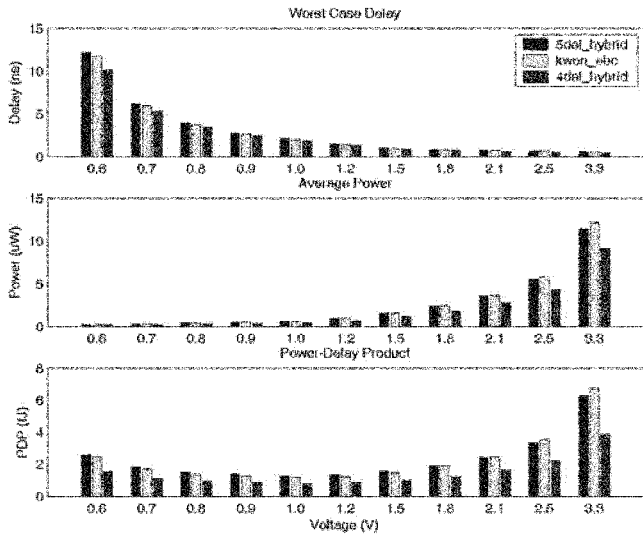
Fig. 27. Performance of different 5-2 compressor architectures with hybrid configuration (Designs 3, 8, 12. Configuration kwon_ebc is equivalent to the Kwon's hybrid architecture.)
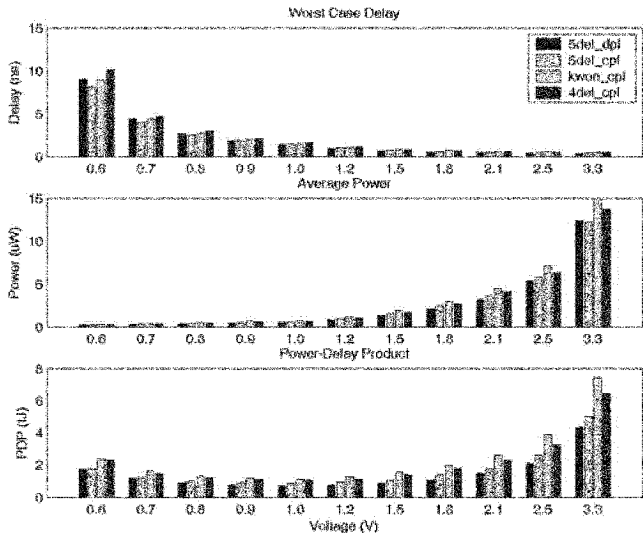

Fig. 28. Performance of different 5-2 compressor architectures of dual-rail logic configuration (Designs 4, 5, 9, 13).

architecture. It is also 6% to 23% faster than Kwon's architecture and 12% to 23% faster than the 5Δ architecture. Therefore, the hybrid configuration is best suited for the proposed architecture.

Fig. 28 shows the comparison of architectures with CPL and DPL configurations. The designs of the 5Δ architectures, 5del_cpl and 5del_dpl, have their performances improved sensibly over the other architectures. Therefore, the CPL and DPL logic styles are more suitable to be implemented on this architecture.

V. CONCLUSION

The architectures of 4-2 and 5-2 compressors are analyzed and different CMOS logic style circuit implementations of their constituent modules are explored. A new low-power circuit with good drivability is proposed for the complex XOR^* logic module which is used to co-generate the XOR–XNOR outputs. A

novel 5-2 compressor architecture of 4Δ delay is also proposed. A new design of the carry generator cell has been spawned as a result of this unique architecture. In order to realistically assess and compare the figures of merits of different configurations of 4-2 and 5-2 compressors at various supply voltages, new simulation environments are established to ensure the measured performances are still sustainable when these cells are integrated in a CSA tree. The simulation results show that the 4-2 and 5-2 compressors constructed with the novel XOR^* cell is able to function down to 0.6 V, and features high speed and low-power characteristics. Our proposed 5-2 compressor architecture outperforms all the other architectures over the range of voltages simulated, particularly when it is configured with the proposed circuits for the XOR^* and the carry generator modules. Better performances against other architectures are also attained almost irrespective of the logic styles used for the circuit implementation of their constituent modules. In summary, a library of excellent power efficiency 4-2 and 5-2 compressor cells based on CMOS process technology has been developed for implementing high speed and low-power multipliers operable at ultra low supply voltages.

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