Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era

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***Abstract*—A 40-nm-gate-length ultrathin-body (UTB) nMOSFET is presented with 20-nm body thickness and 2.4-nm gate oxide. The UTB structure eliminates leakage paths and is an extension of a conventional SOI MOSFET for deep-sub-tenth micron CMOS. Simulation shows that the UTB SOI MOSFET can be scaled down to 18-nm gate length with <5 nm UTB. A raised poly-Si S/D process is employed to reduce the parasitic series resistance.**

***Index Terms*—CMOS, deep-sub-tenth micron, gate work function engineering, MOSFET, raised poly-Si S/D, short-channel effect, SiGe, SOI, ultrathin-body.**

I. Introduction

FULLY depleted silicon-on-insulator (SOI) technology has the advantages of lower junction capacitance and better subthreshold swing [1]. However, the conventional fully depleted SOI MOSFET is known to have worse short-channel effects than bulk MOSFET's and partially depleted SOI MOSFET's [2]. Fig. 1 shows that the UTB SOI device can be scaled down to 18 nm with <5 nm body thickness. The ultrathin-body (UTB) structure eliminates the leakage paths between source and drain [3]. Nearly all the leakage current at $V_g = 0$ in the $T_{si} = 7$ nm flows along the bottom 2 nm of the body, which is least strongly controlled by the gate. Therefore, by eliminating this 2 nm, i.e., making $T_{si} = 5$ nm reduces the leakage by 30 times. The data in Fig. 1 were obtained through device simulation (MEDICI) assuming a low and uniform body doping (10^{15} cm^{-3}) and simple Gaussian S/D doping profiles (peak concentration = 10^{20} cm^{-3}, surface doping concentration under the gate edge = 7.1×10^{16} cm^{-3}). An energy balance model without quantum effect consideration was used. Work function for gate elctrode was assumed to be 4.74 eV. It meets the goals of <3 nA/um $I_{\rm off}$ and >600 uA/um $I_{\rm on}$ for $L_g = 18$ nm with 1.5-nm gate oxide. The good short-channel effects can be seen by comparing the 18 and 30 nm gate curves in Fig. 1 (both having the same T_{si})—ΔV_t is only 45 mV.

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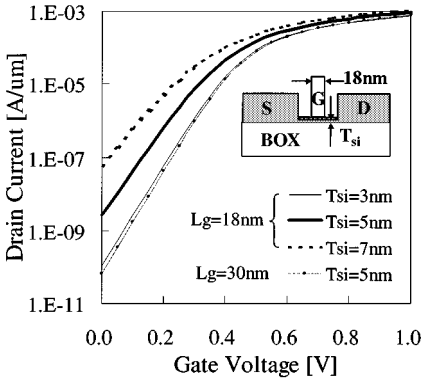

Fig. 1. Impact of body thickness on the I_{ds}–V_{gs} characteristics of UTB SOI device. ($T_{ox} = 1.5$ nm, $N_{sub} = 1e15$ [cm^{-3}], $V_{ds} = 1$ V).

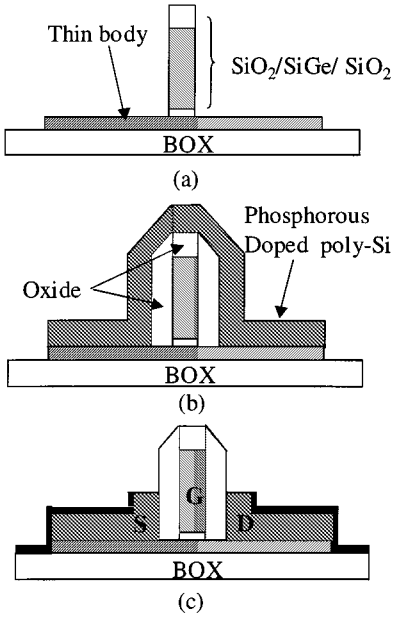

Fig. 2. Process flow of UTB SOI MOSFET (a) after active and gate patterning, (b) after oxide spacer formation and n^+poly-Si deposition, and (c) after cap oxide and n^+poly Si etch-back.

II. Device Fabrication

Our novel UTB device fabrication process is shown in Fig. 2. 100-nm SOI film (BOX = 400 nm) was reduced to 20 nm by thermal oxidation process. Isolation was achieved with a simple silicon etch. The 2.4-nm thin gate oxide was grown at 750 °C in 15 min. For tuning the threshold voltage, boron *in situ* doped

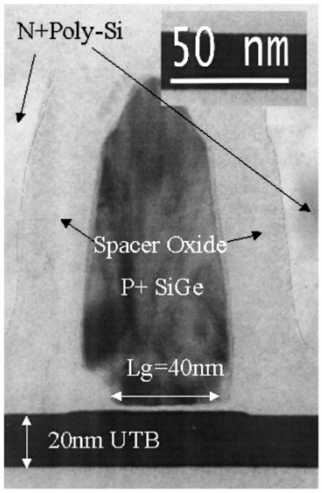

Fig. 3. Cross-sectional TEM picture of 40 nm gate.

poly-SiGe was adopted as a gate material because the work function can be adjusted with the Ge mole fraction [4]. Therefore, the channel can be lightly doped to eliminate the dopant (V_t) fluctuation effect in nano-dimension devices. A high temperature oxide (HTO) hard mask over the gate was employed. All masking steps were done by i-line lithography. The gate pattern was defined first with i-line stepper. The resist pattern was reduced by resist ashing in O_2 plasma and then transferred into the hard-mask oxide. The oxide hard mask pattern was then reduced by HF etching before it was transferred to the poly-SiGe [Fig. 2(a)]. Oxide spacers were then formed. *In situ* doped poly-Si was deposited and patterned with the same active area (thin-body) mask [Fig. 2(b)]. A thin cap oxide was deposited over the poly-Si. A resist-etch back process was used to etch away the top portion of the poly-Si and form the raised poly-Si [Fig. 2(c)], which is self-aligned to the gate to reduce parasitic resistance. Fig. 3 shows the cross-sectional TEM of a device that has 40 nm L_g.

III. Results and Discussion

Typical I_{ds}–V_{ds} characteristics of the 40 nm channel length device are shown in Fig. 4(a), and Fig. 4(b) shows that DIBL is suppressed. The subthreshold swing is 87 mV/dec. Good V_t roll-off characteristics are shown in Fig. 5. The total parasitic series resistance was determined to be 2400 $\Omega\mu$m by plotting V/I versus L_g. It is high because the S/D extension doping process was not optimized in this experiment.

In short, the UTB MOSFET with self-aligned raised poly-Si S/D shows well-behaved current–voltage (*I–V*) characteristics at sub-50 nm devices. The special features of the new device structure are the following.

1) Ultrathin-body eliminates all leakage paths that are far from the gate, thus suppressing the short-channel effects.
2) Self-aligned raised poly-Si S/D reduces the parasitic resistance.
3) Gate is patterned with i-line lithography and reduced from 0.5 to 0.04 μm with resist ashing and oxide trimming.
4) The topography is quite flat and the process is similar to that used in today's planar CMOS technology.

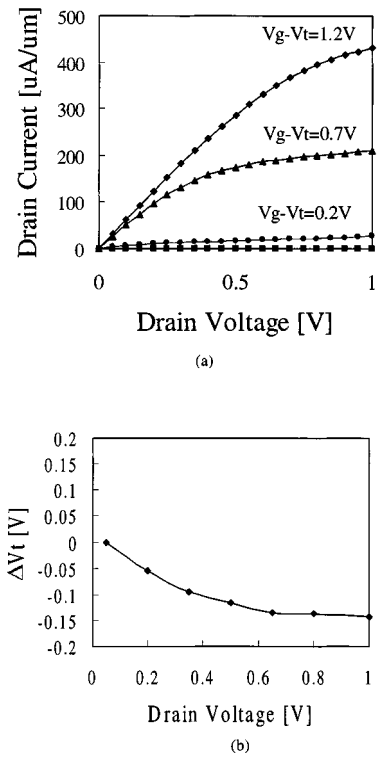

Fig. 4. Measured UTB SOI n-MOSFET: (a) I_{ds}–V_{ds} characteristics and (b) ΔV_t–V_{ds} characteristics of 40-nm effective channel length.

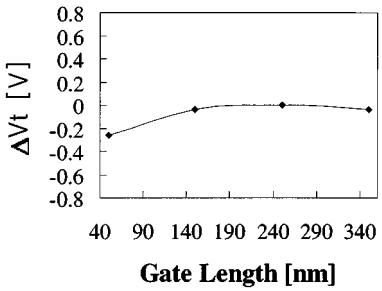

Fig. 5. Measured threshold voltage dependence on the channel length.

IV. Conclusion

An ultrathin-body SOI MOSFET is demonstrated as a promising device structure for deep-sub-tenth micron CMOS technology. 40-nm channel length was achieved with the UTB which suppresses the short-channel effect. 18 nm-gate-length CMOS can be attainable if <5 nm ultrathin-body is used.

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