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Ultrafast Synaptic Events in a Chalcogenide Memristor

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Compact and power-efficient plastic electronic synapses are of fundamental importance to overcoming the bottlenecks of developing a neuromorphic chip. Memristor is a strong contender among the various electronic synapses in existence today. However, the speeds of synaptic events are relatively slow in most attempts at emulating synapses due to the material-related mechanism. Here we revealed the intrinsic memristance of stoichiometric crystalline $Ge_2Sb_2Te_5$ that originates from the charge trapping and releasing by the defects. The device resistance states, representing synaptic weights, were precisely modulated by 30 ns potentiating/depressing electrical pulses. We demonstrated four spike-timing-dependent plasticity (STDP) forms by applying programmed pre- and postsynaptic spiking pulse pairs in different time windows ranging from 50 ms down to 500 ns, the latter of which is 10^5 times faster than the speed of STDP in human brain. This study provides new opportunities for building ultrafast neuromorphic computing systems and surpassing Von Neumann architecture.

Humankind has never stopped his footsteps to pursue a machine that can function like the human brain, which is the most sophisticated organ in existence. The large number of neurons (10^{11}) and synapses (10^{15}) in the brain, along with the network complexity of the nervous system may be the biggest obstacles to creating such a machine. Although their design has benefited greatly from the scaling of complementary metal-oxide semiconductor (CMOS) technology, neuromorphic circuits and chips are still hindered by challenges related to area and power consumption restrictions. Tens of transistors and capacitors are required to build a neuron, a synapse and a learning module[1]. In particular, when considering the high-level connections of neuronal dynamics, a large area on existing neuromorphic chips is dedicated to synapses, whereas neurons occupy only a small portion of a synaptic matrix. To the end, a lack of compact and power-efficient electronic synapses could be a key factor affecting the development of brian scale neuromorphic systems[2].

In recent years, researchers have demonstrated the feasibility of various nanoscale electronic devices that emulate representative neuronal and synaptic functions, such as synaptic modifications, excitatory/inhibitory postsynaptic currents and memory consolidation[3–16]. The resistance or conductance of the electronic synapses in these physical implementations represents the synaptic efficacy (synaptic weight), which is the connection strength between neurons[17]. The Hebbian spike-timing-dependent plasticity (STDP) rule has been a commonly demonstrated biological function in various electronic synapses[3–6,13–16]. This function has been experimentally observed in a wide variety of neural circuits in different species, ranging from locusts to humans, and is regarded as the basis for learning and memory[18–20]. Among currently available devices,chalcogenide device is a competitive candidate for combining data storage and processing in a manner similar to neural cognitive processing[21,22]. In addition to being used as a non-volatile memory because of the reversible switching between chalcogenide's amorphous and crystalline states[23–25], chalcogenide device is also capable of acting as an arithmetic processor[26], as a result of the natural energy accumulation property. Kuzum et al. recently utilized the partial crystallization property of chalcogenide controlled by different RESET and SET pulses to mimic STDP and achieved picojoule-level energy consumption[27]. However, the high precision programming of resistance states, which is crucial for emulating the analog nature of synaptic efficacy, can be perturbed by percolation phenomena. Moreover, most electronic synapses neglect the tuning of the STDP time window, and duplicating the biological window with a time scale on the order of tens of milliseconds is obviously insufficient for creating future ultrafast neuromorphic systems.

We uncovered the intrinsic memristance of stoichiometric crystalline $Ge_2Sb_2Te_5$ (c-GST), a mature chalcogenide material used for non-volatile memory. The memristive characteristics facilitated fine resistance programming through the application of polarity electrical pulses, which were capable of emulating synaptic weight modification. We demonstrated four STDP forms using programmed pre- and postsynaptic spike pairs and tuned the STDP time window from the order of milliseconds down to nanoseconds, addressing the potential for ultrafast synaptic events to occur outside the brain. Note that our approach focused on the use of the crystalline state of GST, which is very different from the methods used by Kuzum et al. and Suri et al.[27,28].

Results

Memristance of crystalline $Ge_2Sb_2Te_5$. We fabricated a typical T-structure GST based memristor using micro/nano fabrication processes (See Methods). The two terminal device is used as the electronic synapse. We built up an electrical characterization system to perform electrical measurements (See Methods and Supplementary Fig. S1). The device switched between the amorphous and crystalline states and displayed good endurance without failure (Supplementary Fig. S2). To study the memristance of c-GST, the device was first set to the crystalline state at several kilo-ohms using a DC voltage sweep. Next, the hysteresis and asymmetry memristive characteristics were observed under the clockwise voltage sweep $0 \rightarrow -1\ V \rightarrow 0 \rightarrow 1\ V \rightarrow 0$ (Fig. 1b) with a current compliance of 100 mA. Our results indicated that the resistance could be modulated within a certain range depending on the voltage polarity. The highest resistance state (HRS) in the c-GST was below 10 kΩ, while the lowest resistance state (LRS) was approximately 500 Ω. The resistance states were all measured at a read current of 1 μA during the electrical measurements.

To further analyze the memristive mechanism, different conduction models were used to fit the nonlinear I–V curve[29]. Thermionic emission ($I \propto V$), Schottky emission ($\ln I \propto \sqrt{V}$), Poole-Frenkel emission ($\ln I/V \propto \sqrt{V}$), and Fowler-Nordheim quantum tunneling ($\ln I/V^2 \propto V^{-1}$) were not good fits for the curve; space charge limited conduction (SCLC) ($I \propto V^2$) was the best model for interpreting the memristance of c-GST and can be described by

$$I = (\varepsilon \mu_0 N_c e^{-E/kT}/N_t d^3)V^2, \quad (1)$$

where ε is the dielectric constant, μ_0 is the carrier mobility, N_c is the density of states in the valence band, E is the effective trapping potential, k is the Boltzmann's constant, T is the temperature, N_t is the number of traps, d is the effective film thickness[30–33]. The slopes of the double-logarithmic plots of negative bias and positive bias were analyzed (Fig. 1c). The low voltage region (<-0.25 V) was dominated by linear Ohmic conduction. At subsequent higher voltages, the I–V relationship agreed with the trap-controlled SCLC, as has been observed in other memristive materials[30,32,34]. Such memristive phenomena could account for the defects in the c-GST. Although GST has a stable hexagonal structure, the fast phase transformation

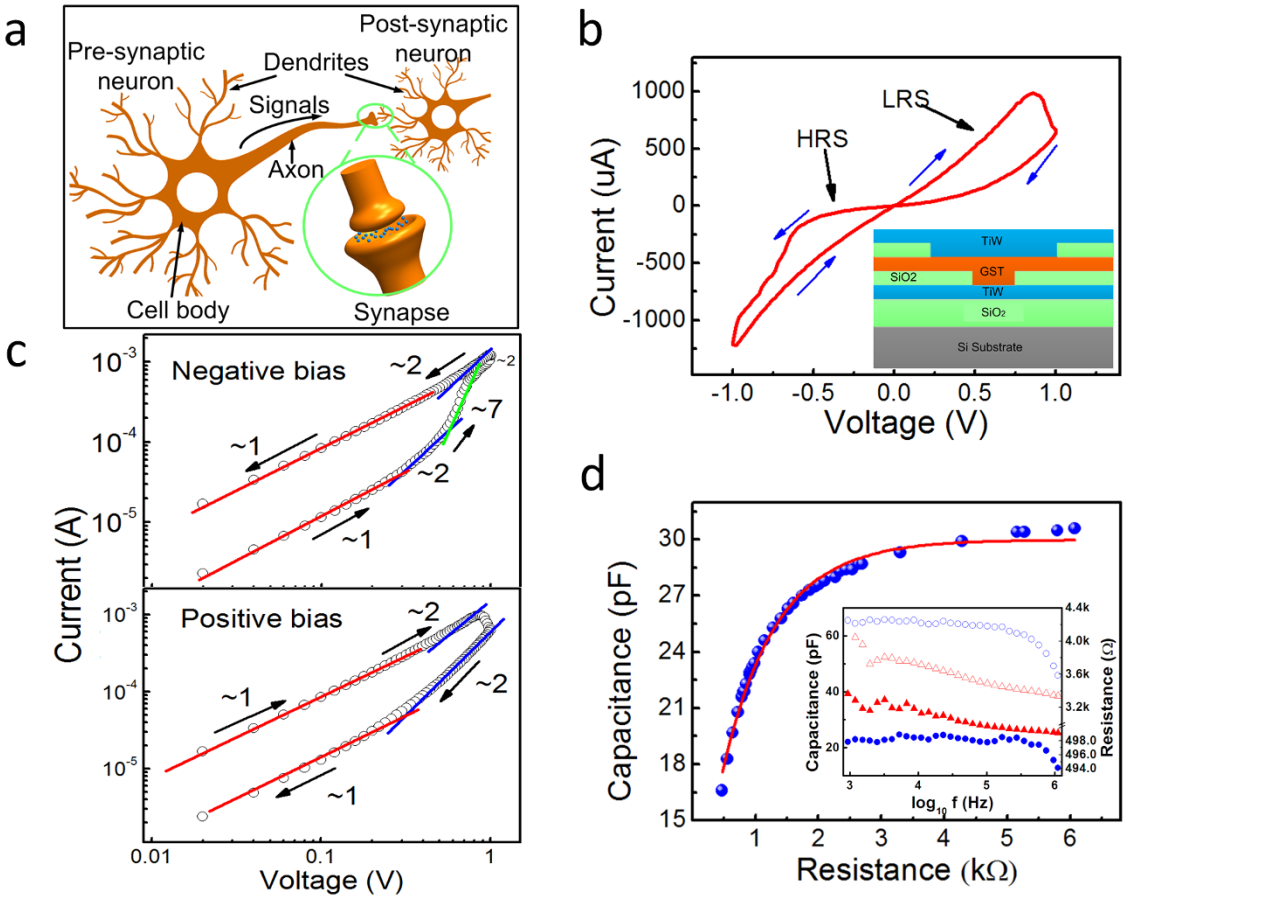

Figure 1 | Intrinsic memristance of a crystalline GST-based synapse. (a) Schematic illustration of a typical biological neuron possessing a cell body (soma), an axon and dendrites. The synapses are the connections between neurons. (b) I-V characteristics measured by DC double sweeping, exhibiting a memristive hysteresis loop. The blue arrows indicate the voltage sweeping directions, and the inset shows the structure of the chalcogenide synapse. (c) Double-logarithmic plot of negative bias (upper) and positive bias (lower) regions exhibiting SCLC behavior. (d) Dependence of capacitance on resistance. The inset shows the frequency dependence of R(ω) (circle symbols) and C(ω) (triangle symbols) at zero bias for HRS (open symbols) and LRS (solid symbols).

proceeds between the amorphous and metastable distorted rocksalt structure with a face-centered-cubic (fcc) lattice, which has been confirmed by high-resolution transmission electron microscopy and X-ray diffraction[35,36]. In the GST fcc structure, Te atoms occupy the anionic sites, while the cationic sites are occupied randomly by Ge and Sb atoms, with 20% vacancies[35–38]. These vacancies and defects at grain boundaries create deep energy levels in the band gap between the conduction and valence bands, and act as charge trap centers. During the application of external negative voltage bias in this experiment, the injection electrons were captured by the vacancies, filling the deep-level traps. The conduction behavior in the positive bias region indicated the transition from trap-filled to trap-unfilled SCLC associated with charge emission. These processes resulted in the variation of resistance, which occured simultaneously with a change in capacitance.

Figure 1d shows that when the resistance varied from 474 Ω to 6.07 kΩ, the capacitance increased from 16.6 to 30.6 pF, suggesting a change in the space-charge distribution. Meanwhile, the inverse relationships between resistance R(ω) or capacitance C(ω) and the frequency also support the model[31,39], as shown in the inset of Fig. 1d. The high frequency disturbed the establishment of the space charge distribution, and the trapped and free carriers could not reach a thermal equilibrium, resulting in the increase in current. Therefore, the R(ω) and C(ω) values at higher ω were less than the respective low-ω values.

Although bipolar resistive switching phenomena have been reported in GST, they are all based on the conductive filament theory[40–42]. The memristive characteristics of c-GST are intrinsic characteristics. Lattice defects, mainly vacancies, and defects at grain boundaries appear as a natural cause of the memristance.

Modification of synaptic efficacy and implementation of ultrafast STDP. The postsynaptic conductance changes as ion channels open or close when they are induced by potentiating or depressing postsynaptic potentials. To emulate this synaptic weight modification, the conductance of a chalcogenide memristor was used to represent the synaptic weight, and positive and negative pulses were applied to modulate the conductance. The shortest pulses that we used are presented in Fig. 2. First, the device was set to an initial crystalline state of approximately 2.6 kΩ using a SET pulse (2 V, 100 ns). The negative pulses led to the increase in conductance that represented potentiating spikes, while the positive pulses represented depressing spikes. The pulse widths and rise and fall times were fixed at 30, 10 and 10 ns, respectively. The amplitudes of 20 consecutive potentiating spikes increased from −0.6 to −0.8 V with a 10-mV step, and the amplitude of 20 consecutive depressing spikes increased from 1 to 1.8 V with a 40-mV step. Note that the 1.8-V, 30-ns pulse was not sufficient to induce the phase change from crystalline to amorphous. The resistance exhibited a gradual repeatable change ranging from 2.2 to 3.0 kΩ, and the mean resistance change per pulse was approximately 40 Ω, which indicates a relative accuracy of 1.8%. Theoretically, a more accurate modulation could be possible by using an adaptable variation-tolerant algorithm[43]. Based on the fine synaptic weight modulation that occurred in response to pulses of different polarities, more complex synaptic events could be implemented in the chalcogenide synapse.

Biologically, as Hebb stated, "Neurons that fire together, wire together"[44]. STDP, as a refinement of Hebb's theory, is considered to be a possible first law of synaptic plasticity. STDP refers to that the precise relative timing of pre- and postsynaptic spikes significantly affects the sign and magnitude of long-term synaptic modification, which have been found to vary in different cases[19,45,46]. (i) In temporal windows for excitatory to excitatory connections, long-term potentiation (LTP) occurs if the presynaptic action potential precedes the postsynaptic firing ($\Delta t > 0$, where Δt is the relative time interval of the pre- and postsynaptic spikes), whereas presynaptic activity that followes postsynaptic spike ($\Delta t < 0$) causes long-term depression (LTD). (ii) In windows for excitatory to inhibitory connections, LTP and LTD can be induced in the opposite manner. In some other cases, synaptic modification depends only on the relative timing amount of the pre- and postsynaptic spikes, but not on their orders. For example, (iii) a symmetric Hebbian learning rule occurs at the neuromuscular junction, which means that potentiation occurs when Δt is ~0 and depression when Δt moves away from 0. Moreover, (iv) in synapses between spiny stellate neurons in neocortex-layer 4, depression occurs at all values of Δt. Biological experimental results indicated that these different STDP forms could be ascribed to the influence of different spikes, reflecting the complexity of the respective underlying cellular mechanisms, and that they have a variety of functional consequences in neural information processing.

These four different STDP forms with nanosecond-scale time windows were successfully implemented in our chalcogenide synapse (Fig. 3) by following a typical spike paring protocol used in biological synaptic studies and in other electronic synapses. These synaptic events were demonstrated in a critical time window of approximately 500 ns, which is 10^5 times faster than the human brain. Δw represents the percent change in synaptic weight i.e., the device conductance, representing the long-term nonvolatile modification of the synaptic efficacy as a function of the time interval Δt. For example, LTP occurs when $\Delta t > 0$ and LTD occurs when $\Delta t < 0$

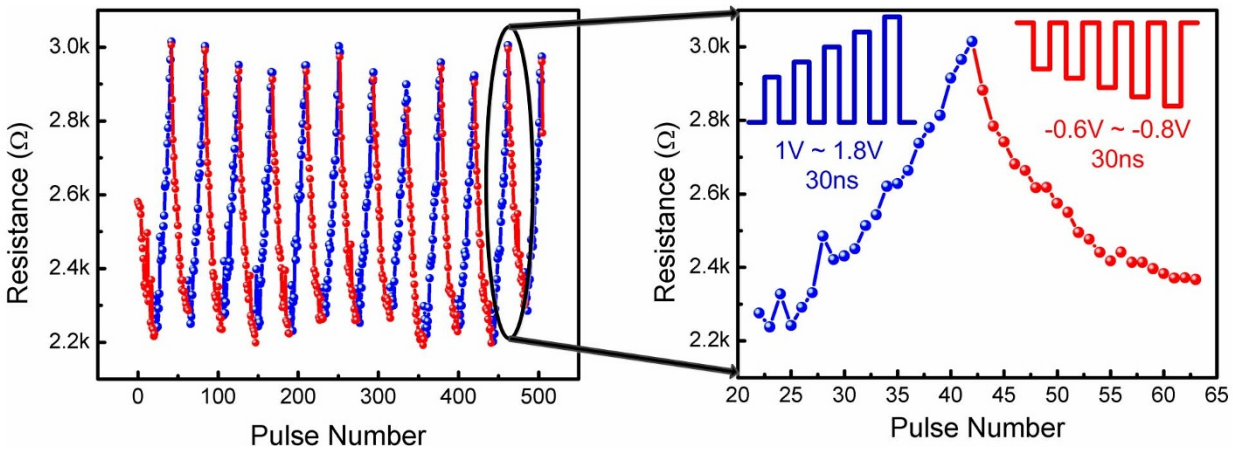

Figure 2 | Pulse-driven memristive behavior. The conductance increases or decreases in response to negative or positive pulses, respectively, representing synaptic weight modulation due to potentiating or depressing pulses. The pulse amplitudes vary with identical 30-ns widths and 1-s pulse intervals.

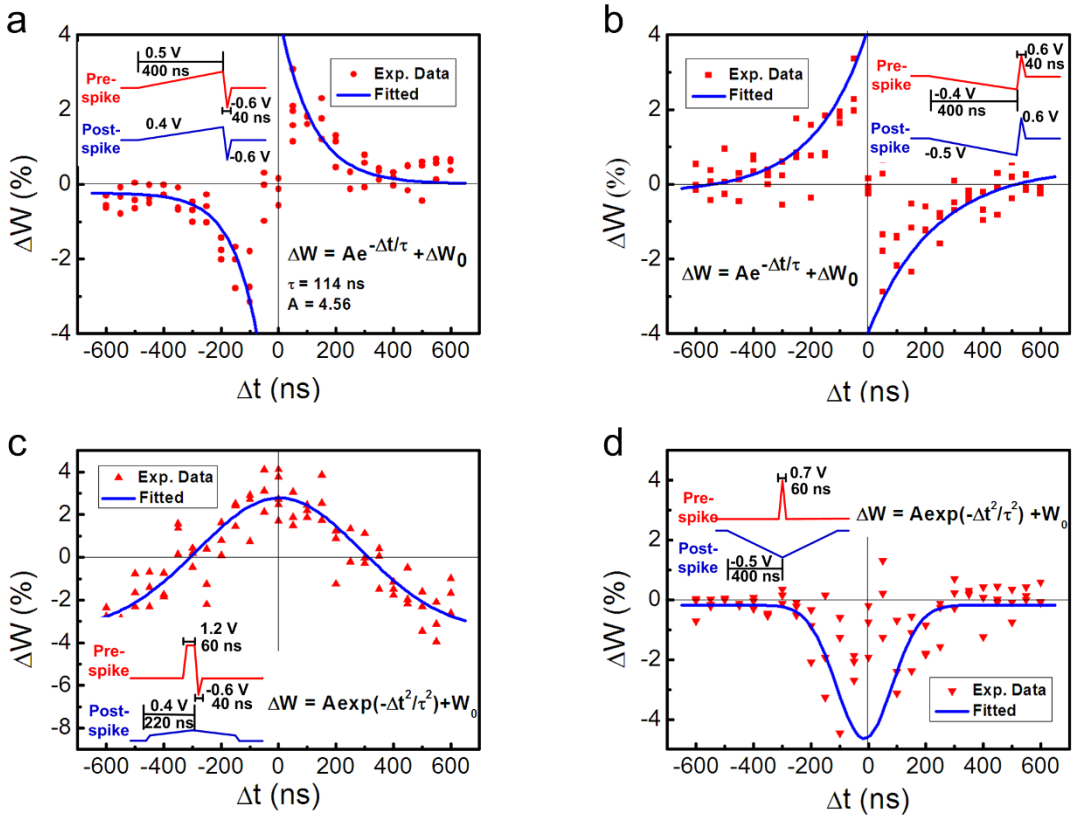

Figure 3 | Implementation of STDP with nanosecond-scale time windows in the chalcogenide synapse with the (a), antisymmetric Hebbian learning rule, (b), antisymmetric anti-Hebbian learning rule, (c), symmetric Hebbian learning rule and (d), symmetric anti-Hebbian learning rule. The red dots indicate the experimental data and the blue lines are the fitted curves. The insets show the pre- and postsynaptic spike schemes and fitting functions.

in a typical antisymmetric Hebbian learning rule as shown in Fig. 3a, and the left upper inset shows the shapes of the pre- and postsynaptic spikes.The maximum amount of synaptic modification which reached 3.26%, occured when the paired spikes were separated by only a few ns, and the evoked plasticity decreased to nearly zero as Δt increased. A total of 75 spike pairs were applied in our measurements, and the STDP data had statistical scatter, which also exists in biological synapses.

When we applied the pulse stimulus to drive the device resistance variation, a threshold voltage V_θ exists, approximately 0.6 V. The pulse amplitudes of all pre- and post-spikes in all STDP experiments were less than 0.6 V, which are below the threshold, that means a single pre- or postspike could not modify the weight. When the pre- and post-spike arrived at the device in an opposite direction, the amplitude of the total voltage at the device may exceed the threshold, leading to a resistance variation. The effective flux that can influence the resistance variation should be

$$\varphi(t) = \int V_E dt, \tag{2}$$

Where

$$V_E = \begin{cases} V_{pre} - V_{post} + V_\theta & V_{pre} - V_{post} < -V_\theta \\ 0 & -V_\theta \le V_{pre} - V_{post} \le V_\theta \\ V_{pre} - V_{post} - V_\theta & V_{pre} - V_{post} > V_\theta \end{cases}, \tag{3}$$

As Δt increases, the effective voltage V_E and effective time both decrease, leading to the decrease in effective flux, so the evoked synaptic weight change also decreases (Note that ns-level weight modulation does not equal to the ns-level STDP time window, see Supplementary Fig. S3 and Fig. S4).

STDP can be simplified in computational neuroscience using mathematical models by fitting it with an exponential function:

$$\Delta w = Ae^{-\Delta t/\tau} + \Delta w_0, \tag{4}$$

where A and τ refer to the scaling factor and time constant of the STDP function, respectively, and Δw is a constant representing a non-associative component of the synaptic change[47]. Here A = 4.56 and τ = 114 ns for the LTP in antisymmetric Hebbian learning rule, whereas the time constant of the STDP window is of the order of tens of milliseconds for biological synapses. Additionally, the other three STPD forms could be implemented by modulating the shapes of the spike pairs. For example, the antisymmetric anti-Hebbian learning rule could be realized by applying the same spike pairs as those used in the Hebbian learning rule in a reversed temporal sequence (Fig. 3b). Moreover, the learning function for the symmetric Hebbian learning rule and symmetric anti-Hebbian learning rule could be expressed as a Gaussian function (Fig. 3c and Fig. 3d):

$$\Delta w = A \exp(-\Delta t^2/\tau^2) + \Delta w_0. \tag{5}$$

Tuning of the STDP time window. The above process allowed us to successfully implement ultrafast STDP events in a chalcogenide memristor. Furthermore, by employing the same spike coincidence strategy, we could easily tune the time constant of the STDP rules by modulating the pulse width and interval, which is critical to the application of electronic synapses in neuromorphic engineering. On one hand, synapses with various τ in different cortex locations or develop periods are related to different computational tasks and play instructive roles in neural functions[48,49]. For example, recent studies revealed that relative spikes separated by 25 ms or more promote synapse elimination in development as in adult plasticity.

When spikes are separated by 20 ms or less, the activity is perceived as synchronous, and elimination is prevented[50]. On the other hand, if the chalcogenide synapse allows the implementation of STDP on various temporal scales, meaning that the chalcogenide synapse respondes only to the pre- and postspike forms rather than to the spiking rate, circuit design flexibility could be improved while reducing the complexity of peripheral neuron circuits.

We demonstrated STDP forms with different time constants, as shown in Fig. 4 a–c. The time windows in these diagrams are 5 μs, 500 μs and 50 ms, respectively, the latter of which is comparable to biological values. The single spike pulse for the 5 μs STDP was modulated to approximate 5 μs width, whereas the shapes of the spike pairs for 500 μs and 50 ms were modulated to a sequence of step-up pulses with an identical 500-ns width and pulse intervals of 50 μs and 5 ms, respectively (details of the spike pairs, see Supplementary Fig. S5 and Fig. S6). The pulse width of the spikes were enlarged to provide a greater injection of charges. This enhancement of the charge-trapping amount broadened the resistance variation range, which led to an increase in the scaling factor. The increase in the the pulse intervals resulted in an increase in the time constant. After exponential fitting, the A/τ for the 5 μs, 500 μs and 50-ms time window are 32.5/1292 ns, 40.5/298 μs and 93.3/35.4 ms, respectively.

Note that, biologically, the neurons always fire persistently and generate pre- and postsynaptic spike trains to affect the synaptic facilitation and depression. In our above STDP experiments, only one pre- and post-spike pair was applied to evoke the change in synaptic weight, resulting a relative small Δw. When we increased the spike pair number, the evoked weight change also increased. Take the LTD in 500-ns time window for example, the largest synatptic weight change can reach -45% if we input 220 continous pairs of pre- and post-spikes (See Supplementary Fig. S7).

Discussion

Compared with other emerging electronic synapses[5,6,11,13,14,16,27], the analog chalcogenide synapse displayed the advantages of ultralow operation voltage, ultrafast synaptic events and feasibility of time window tuning (Fig. 4d). While chalcogenide devices have already demonstrated a drastic reduction in power and time requirements for operation[51,52], the mature CMOS-compatible fabrication processes of chalcogenide materials enable us to intergrate the electronic synaptic matrix with traditional CMOS neuron chips with the goal of performing more complex cognitive functions in one chip, such as visual pattern cognition and associative learning[28]. And based on the network arthictecture (crossbar and 3D stacking), the important superiority of neural system, parrallelism, could be further investigated. In addition, the energy accumulation phenomenon associated with chalcogenide's amorphous state has been proposed to emulate neuronal threshold spiking behavior, which was verified in our memristor device (Supplementary Fig. S8 and Fig. S9). We envisage a complete neuron-synapse system being implemented in a

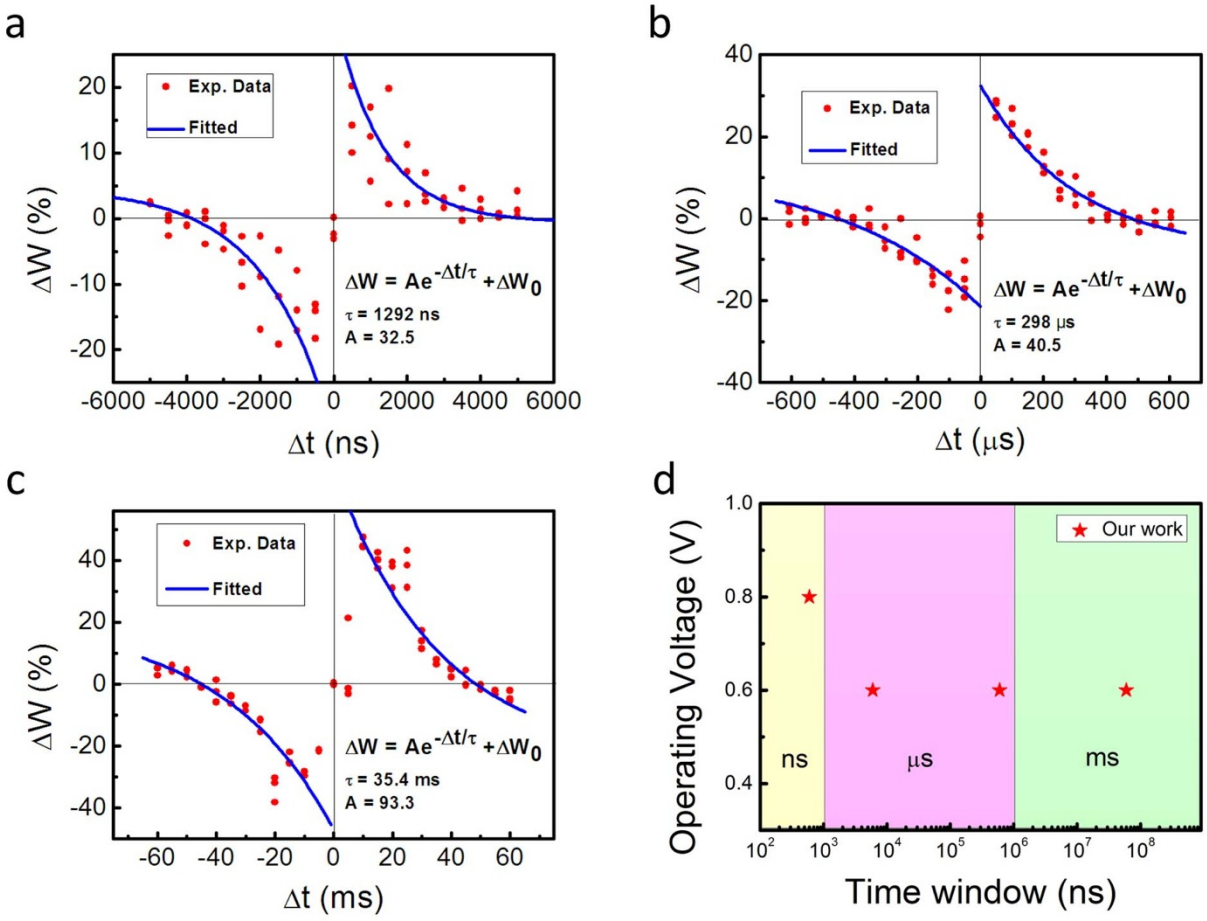

Figure 4 | Tuning of the STDP time window. (a) A 5 μs time window with a time constant of 1.29 μs. (b) A 500 μs time window with a time constant of 298 μs. (c) A 50-ms time window with a time constant of 35.4 ms. The time constant τ is tuned by modulating the pulse width and interval. The increasing of scaling factor A results from the enhancement of the resistance change variation due to wider pulses that provide more injection charges. (d) Chalcogenide synapse shows its advantages: operating at ultralow voltage and tuning of the time window down to the nanosecond scale, whereas the time window of biological synapse is about 50 ms.

chalcogenide-based matrix, which could be an attractive option for the design of future neuromorphic system.

This study demonstrated that ultrafast synaptic events can be implemented in chalcogenide synapses. We revealed that the intrinsic memristive characteristics of crystalline GST originated from the charge trapping and releasing by defects in the material. The memristance offered us a foundation for emulating synaptic weight modulation, and we used it to implement four different STDP forms. Furthermore, the feasibility of STDP time window tuning in this material was also demonstrated from 50 ms to 500 ns, the latter of which is 10^5 times faster than the speed of STDP in human brain. In principle, the scaling up of the number of analog/plastic synapses with low power consumption and ultrafast response times is in urgent demand for further evolution of neuromorphic chips. We believe that the completely passive, non-volatile chalcogenide synapse is a strong contender for replacing the existing transistor- and capacitor-based electronic synapse and provides a promising method of surpassing Von Neumann architecture.

Methods

Chalcogenide device fabrication. The chalcogenide device was fabricated on a Si substrate with a 1 μm thick thermally grown SiO_2 layer. The confined structure (Fig. 1B inset) was fabricated using magnetron sputtering, photolithography and lift-off processes. The thicknesses of the bottom electrode (TiW), $Ge_2Sb_2Te_5$ (GST) film, SiO_2 insulator and top electrode (TiW) were 50, 150, 100 and 150 nm, respectively, and all deposited without the substrate heating. The background and working pressures for GST sputtering were below 10^{-5} Pa and approximately 0.5 Pa. The GST deposition rate was approximate 0.5 nm/s at 30 W DC power. The contact area (1 μm diameter) was patterned using photolithography. The GST and SiO_2 films were deposited subsequently using lift-off with supersonic vibration in acetone to remove the AZ5214 photoresist.

Electrical characterization. The electrical measurements of the chalcogenide device were conducted on a self-built electrical characterization system containing a semiconductor characterization system (Keithley 4200-SCS), an oscilloscope (Agilent Technologies DSO5012A), a Precision LRC Meter (Agilent E4980A) and a self-design PCB testing board, as shown in Fig. S1.

The pulse generator integrated in the system has the specifications of pulse duration, rising time and falling time ranging from 10 ns to 1 s, each portion of segment pulse, including duration, rising time and falling time, ranging from 20 ns to 1 s, and amplitude ranging from −5 to 5 V. AC pulse channel, DC current/voltage force and sense channels converge to a Keithley 4205 Remote Bias-Tee and output to memristor. The wire-bonded memristor chip is embedded in the PCB testing board, while two terminals of the testing boarding connected to two terminals of a selected memristor cell, respectively. In Fig. S1, Switch1 (SW1) to SW5 are selectively closed or opened. When only one channel is needed to send and sense signal, like IV curve sweeping and sending pulses to gradually change the resistance, SW1 is closed, the others are opened. When two channels are needed, like emulating STDP, SW2 is closed, the others are opened. When closing SW3 or SW4, wave forms of the corresponding nodes can be observed by oscilloscope.

To measure the capacity of the memristor device, the wire-bonded memristor chip is connected to the Precision LCR Meter though a Test Fixture (Agilent 6334A) applying 10 MHz, 10 mV small signal.

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Author contributions

Y. L. and X. M. conceived and designed the experiments. Y. L. and Y. Z. drafted the paper. Y. Z., L. X. and X. X. carried out the electronic measurements, Y. L., J. Z. and L. X. contributed to the device fabrication and material analysis, Y. L. carried out the simulation, Y. L., X. M. and H. S. performed theoretical analysis. X. M. directed the projects and provided overall guidance throughout. All authors discussed the results and commented on the manuscript.

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