Ultralow-Power Electronics for Biomedical Applications

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Annu. Rev. Biomed. Eng. 2008. 10:247–74

First published online as a Review in Advance on April 4, 2008

The *Annual Review of Biomedical Engineering* is online at bioeng.annualreviews.org

This article's doi: 10.1146/annurev.bioeng.10.061807.160547

1523-9829/08/0815-0247$20.00

Key Words

ultralow-power circuits, energy harvesting, subthreshold operation, CMOS, implantable devices, wireless communication

Abstract

The electronics of a general biomedical device consist of energy delivery, analog-to-digital conversion, signal processing, and communication subsystems. Each of these blocks must be designed for minimum energy consumption. Specific design techniques, such as aggressive voltage scaling, dynamic power-performance management, and energy-efficient signaling, must be employed to adhere to the stringent energy constraint. The constraint itself is set by the energy source, so energy harvesting holds tremendous promise toward enabling sophisticated systems without straining user lifestyle. Further, once harvested, efficient delivery of the low-energy levels, as well as robust operation in the aggressive low-power modes, requires careful understanding and treatment of the specific design limitations that dominate this realm. We outline the performance and power constraints of biomedical devices, and present circuit techniques to achieve complete systems operating down to power levels of microwatts. In all cases, approaches that leverage advanced technology trends are emphasized.

Contents

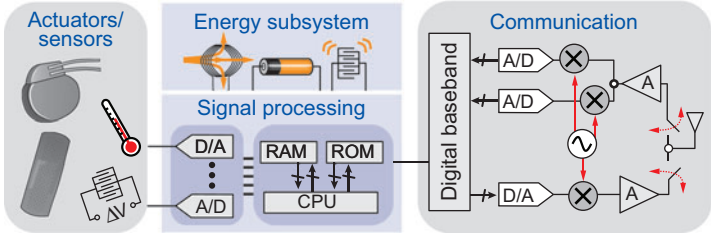
1. INTRODUCTION

Recent advances in integrated circuit (IC) technology, as well as innovations in circuit design techniques, have led to systems with processing capabilities that can supplement, or even entirely replace, complex biomedical operations such as speech spectral analysis. Importantly, however, with the right technical approach, this functionality can be achieved at power levels and form factors allowing these systems to be entirely implantable. Indeed the processing capabilities of ICs are virtually unlimited, but energy, in biomedical electronics, is highly limited. For example, if an implanted medical device were powered by a low-power general purpose processor, which consumes approximately 10 mW, current battery technology would accommodate approximately 3 days of operation. Alternatively, dedicated solutions, employing specialized low-power design techniques, consume approximately 8 μW, achieving more than 10 years of operation with the same battery (1).

A conceptual diagram for a generic biomedical device appears in **Figure 1**. The core components of the device are shown, which include data conversion, signal processing, and communication subsystems, and these interface with the biomedical environment through sensors and actuators. Additionally, an energy subsystem is required to efficiently power the electronics. This review focuses on the core electronic components and the energy subsystem, describing the specialized techniques required to achieve ultralow-energy operation for practical biomedical systems.

2. ELECTRONIC BIOMEDICAL SYSTEMS

Table 1 highlights some existing and emerging biomedical applications and lists their specific performance requirements. In general, the power levels consumed range from a few microwatts to a few milliwatts, and adhering to these stringent power budgets sets an upper limit on the number



IC: integrated circuit

Figure 1

Conceptual diagram of a generic biomedical device.

Table 1 Examples of existing and emerging applications for biomedical devices

Application	Performance specification				
	Power	ADC/DAC	Processor	Communication	Energy source
Pacemaker and cardioverter-defibrillator (1, 2)	<10 μW	1 kSPS, 8b ADC	1 kHz DSP	Inductive link	10-year lifetime battery
Hearing aid (3, 4)	100–2000 μW	16 kSPS, 12b ADC	32 kHz-1 MHz DSP	Telecoil	1-week lifetime rechargeable battery
Analog cochlear processor (5, 6)	200 μW	16, 1 kSPS, 8b ADCs	Analog DSP (~16 MIPS)	Inductive link	1-week lifetime rechargeable battery
Neural recording (7, 8)	1–10 mW	Up to 1000s of channels, 100 kSPS, 8b ADC	n/a	High rate inductive link	Inductive power
Retinal stimulator (9, 10)	250 mW	10 kSPS, 4b DAC (per electrode)	No embedded DSP	High rate inductive link	Inductive power
Body-area monitoring (11)	140 μW	1 kSPS, 12b ADC (per channel)	<10 MHz DSP	Far-field wireless link	Battery

of computational operations that can be performed in each case. Consequently, optimizing the constituent circuits and systems, as well as developing efficient algorithms compatible with the chosen implementations, is central to biomedical electronics design.

First demonstrated in the 1950s, one of most common implanted biomedical devices is the pacemaker (1). These devices are among the most highly energy constrained, requiring years of operation on a single battery charge to avoid repeated surgery. The average power consumption of a pacemaker is on the order of five to ten microwatts, and is enabled by the minimal processing requirements and low analog-to-digital converter (ADC) speeds (100–1000 samples per second) (1). Modern pacemakers, however, often include support for cardiac defibrillation, which requires large electric pulses that are both power and energy intensive, resulting in significant circuit design challenges.

Like pacemakers, both hearing aids and cochlear processors are relatively mature biomedical applications. Today, they make front-running strides in power-management (3, 4, 6). Their power consumption ranges down to hundreds of microwatts, and, in some cases, by leveraging high dynamic range ADCs (i.e., 75 dB), they dynamically adjust their power, performance, and ergonomics simultaneously. This agility allows them to easily adapt for individual patients, but, even more impressively, also for the varying acoustic environments each patient faces.

In contrast to pacemakers and hearing aids, neural recording systems and retinal stimulators are emerging applications. Researchers are focused on challenges in the interface and acquisition electronics as well as processing platforms. Nonetheless, many critical challenges are being dealt with by using smart arrays that leverage both material processing innovations and electronics innovations, leading to the integration of more than 100 acquisition channels in a neural recording system (7, 8) and 16 stimulus electrodes in a retinal stimulator (10). Implanted stimulators and recorders offer the potential to revolutionize the treatment of many medical conditions. For example, implanted deep-brain stimulators are used to treat patients with Parkinson's disease (12) and intramuscular stimulation is being investigated for treating paralyzed muscles and limbs (13).

Finally, as biomedical devices become more prevalent, there is increasing need for these devices to support the formation of body-area networks. Body-area networks allow for individual devices to collaborate and communicate with one another. For instance, a finger-mounted pulse

ADC: analog-to-digital converter

oximeter worn by a patient in an operating room can wirelessly send its status to medical personnel to enhance patient monitoring. Electronic devices compatible with body-area networks have widely varying performance requirements depending on the specific application, but power requirements are typically on the order of hundreds of microwatts to milliwatts. Further, for robust communication, the devices must employ standards-compliant wireless communication links.

Radio-frequency identification (RFID): technology to uniquely identify devices using electromagnetic or electrostatic coupling

3. LOW-POWER ELECTRONICS

The stringent energy constraints dominate architectural and implementation decisions throughout the design of biomedical systems. Ultralow-power circuits require specialized techniques, and their associated design trade-offs and limitations are highly specific to this realm. In this section, the critical components of biomedical electronic devices, namely the energy subsystem, the signal processor, the ADC, and the communication transceiver, are treated and analyzed individually with specific consideration to state-of-the-art and emerging approaches to power management.

3.1. Energy Subsystem

Because energy is such an essential resource, it must be efficiently generated, stored, and delivered. The energy subsystem realizes these functions in the form of three main blocks, an energy harvester, an energy storage device, and a voltage converter, which are discussed in the following subsections.

3.1.1. Energy harvester. Devices with lifetimes longer than a single battery charge that cannot be connected directly to the power grid must receive energy from an external source or harvest energy from the ambient environment. For nonimplanted systems, batteries can be recharged or replaced, but, for the user's benefit, as infrequently as possible. For instance, users of behind-the-ear cochlear instruments recharge their batteries daily. For implanted systems, however, batteries cannot be easily removed without surgery, and alternate wireless energy harvesting approaches must be considered. The key energy harvesting options for biomedical devices are presented in **Table 2** (14–17).

To supply energy to implanted devices, wireless electromagnetic energy transfer is an effective and commercially proven technique. It involves transmitting electromagnetic energy into the body and collecting it via a coil or antenna. Low-frequency electromagnetic energy transfer is currently used in cochlear implants, radio-frequency identification (RFID) implants, retinal prosthetics, and neurostimulators (9, 20). The physical process underlying low-frequency wireless energy transfer is near-field electromagnetic induction. Near-field induction involves a transmitter coil generating a changing magnetic field, typically at carrier frequencies in ISM frequency bands such as 14 MHz and 27 MHz. The changing magnetic field induces an AC electrical current in a coil at the receiver.

Table 2 Energy-harvesting options (14–17)

Energy source	Performance
Thermoelectric	60 $\mu W\ cm^{-3}$
Light	100 $\mu W\ cm^{-2}$ (office), 100 $mW\ cm^{-2}$ (direct light)
Vibration	4 $\mu W\ cm^{-3}$ (human motion)
Heel strike	10–700 mW (walking)
Near-field inductive energy transfer	2 mW at 10 cm (card-size antenna, 1 W transmit) (18)
Far-field electromagnetic energy transfer	2 μW at 4 m (card-size antenna, 500 mW transmit) (19)

The AC signal is then rectified to DC and regulated to a stable voltage. Alternatively, rectification is not required if logic is operated directly off an AC supply (21).

Near-field wireless energy transfer results in electromagnetic fields that can heat tissue and generate electromagnetic interference on nearby electronics. Hence, the wireless link must meet regulatory guidelines, including those proposed by the FCC in the United States and the ETSI in Europe (22). For small implanted applications, where volume constraints limit the size of the receive coil, the practical range of energy transfer is limited to a few centimeters. To increase the transfer distance and increase efficiency, both transmitter and receiver can be tuned to induce resonant coupling (23). Alternatively, longer-distance communication can be achieved by operating at frequencies above hundreds of megahertz and employing far-field power transfer (19). However, often, these high frequencies cannot easily penetrate the skin, and channel losses in the body keep overall efficiencies low.

Microelectromechanical systems (MEMS): devices and machines fabricated using microfabrication techniques with a critical dimension of the order of micrometers

Energy gathering is most useful and flexible when harvesting ambient energy, in which the source of energy exists inherently as part of the system. This is not the case for near-field wireless energy transfer, where an explicit powered transmitter is required. An emerging approach that exploits true ambient energy is vibrational energy harvesting from the user's movement. Microscale vibrational energy harvesters have been shown to generate approximately 5 $\mu W\,cm^{-3}$ from human motion (14). This has been applied to self-winding watches, which produce 5 μW on average and 1 mW when forcibly shaken. For higher-power applications, tens to hundreds of milliwatts can be harvested by scavenging energy from the heel strike of a person's gait (14).

For implanted applications, vibration-to-energy converters must be fabricated on the microscale (24). Microelectromechanical systems (MEMS) technology is ideal for these applications, as it allows for the fabrication of mechanical systems equal in size to a microchip. One example of MEMS technology is the MEMS energy harvester presented in Reference 16, which has been fabricated for a low-power biomedical system that includes a power controller and a programmable digital signal processor. The MEMS device operates as a transducer where mechanical motion results in a varying capacitance. **Figure 2*a*** presents the charge-constrained energy conversion cycle using the MEMS variable capacitor as part of a power converter. Charge is transferred to and from the variable capacitor when its capacitance is at a maximum and minimum, respectively. In Reference 16, this charge transfer must be synchronized; however, it is possible to reduce system complexity and power consumption with an asynchronous architecture (25). **Figure 2*b*** shows the fabricated MEMS prototype (26). The MEMS transducer implements a variable capacitor ranging from 2 pF to 260 pF and generates 5 μW of usable energy from a vibration source of 2520 Hz.

An emerging research direction in energy scavenging is to harvest hydraulic energy in the human body, including blood flow, heart beats, and contraction of blood vessels. A 2-mm^2 nanogenerator has been shown to generate currents as high as 35 nA when stimulated by ultrasonic waves that might be found inside a biofluid (27).

3.1.2. Energy storage. To achieve long operational lifetimes, most portable and implantable biomedical devices have local reserves of energy. These local reserves are often stored electrically in a capacitor or chemically in a battery. Primary (nonrechargeable) batteries are used for single-use biomedical applications, such as swallowable capsules, or for devices with a sufficiently long battery life, such as wristwatches or pacemakers, where replacing the battery is not a burden. Silver-oxide primary batteries have been used to power swallowable capsules for the 8-h examination of a patient's digestive tract (28). In long-lifetime applications where primary batteries become prohibitively expensive or inconvenient to replace, secondary (rechargeable) batteries are preferred. A common application of secondary batteries is to power the behind-the-ear instrument of cochlear implants. Two important issues facing secondary batteries are that their capacity degrades over

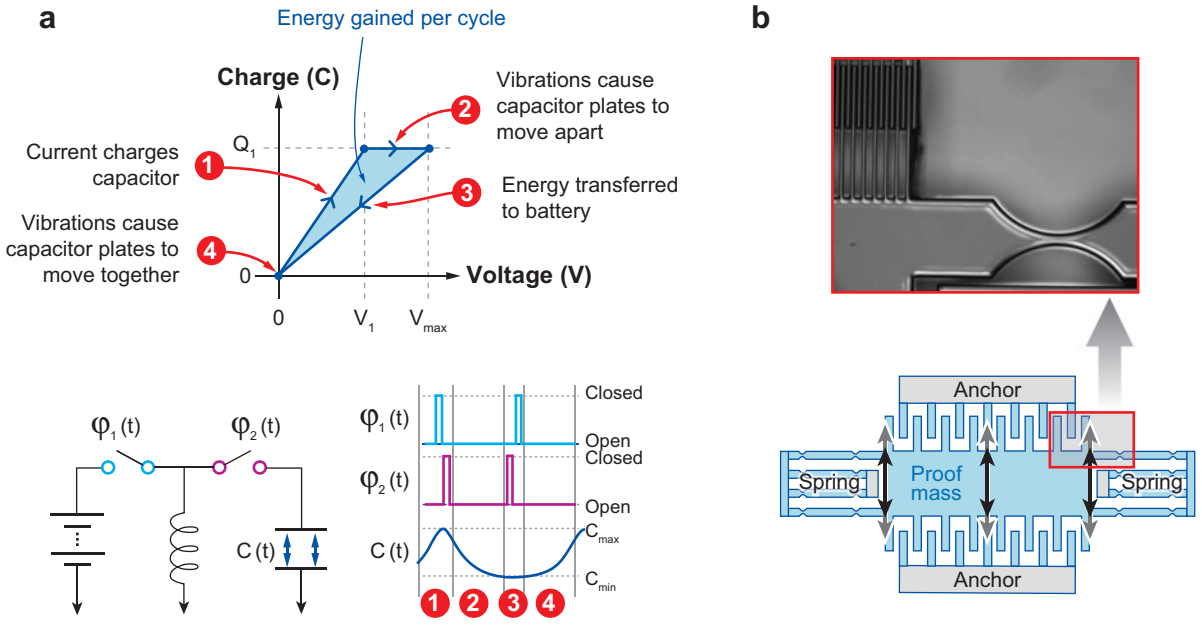


Figure 2

(*a*) Charge-constrained energy conversion cycle for a variable capacitor-based vibration-to-electric energy converter. A conceptual circuit schematic and timing diagram are shown. (*b*) Block diagram and close-up microphotograph of a microelectomechanical system (MEMS) transducer that is part of a vibration-to-electric energy converter (26).

time and that not all batteries can supply the high peak currents required by applications, including cardioverter-defibrillators.

An emerging energy storage technology that has the potential to solve these problems is thin-film batteries (29). Thin-film batteries possess long lifetimes of thousands of charges and discharges, low series resistance, and comparable energy density to existing batteries. These batteries can be hundreds of micrometers thin and are amenable for implantable applications where volume must be minimized. A second emerging technology that promises to improve upon capacitors by increasing their energy storage density is ultracapacitors. In an ultracapacitor, the aluminum electrodes of a traditional capacitor are coated with a thin layer of extremely porous electrically conductive activated carbon, the separator is made of a porous nonconducting material, and the interior is filled with a liquid electrolyte rather like a battery. When a voltage is applied, the positive ions from the electrolyte are absorbed into the activated carbon on the negative electrode and vice versa. The Helmholtz principle of double layers combined with the extremely high surface area of the activated carbon yield more than one hundred times the energy density of traditional capacitors. Although they have extremely high power density compared with chemical batteries, traditional ultracapacitors have only approximately 5% the energy density of lithium batteries. However, there has been research in using a coating of vertically aligned carbon nanotubes in place of the activated carbon (30). If successful, this has the potential to achieve comparable energy densities to lithium ion batteries.

3.1.3. Voltage converter. As load devices often operate at different voltages than the battery voltage or the voltage out of the energy harvester, a voltage converter is used to generate an appropriate and stable supply for the load. By generating an appropriate voltage for the load,

a voltage converter can extend battery life by allowing the load device to operate at its optimal energy point. The key challenge of voltage converters for biomedical applications is achieving high efficiencies at ultralow-power levels and in a small volume (31). Moreover, the output voltage must not fluctuate from its desired value even though the converter can suffer from a variable battery voltage, varying load current, and switching noise (32).

CMOS: complementary metal-oxide-semiconductor

Switched capacitor voltage converter: a voltage converter that uses capacitors to transfer energy to the output, often stepping the voltage up or down

The voltage converter for a biomedical device must be optimized for the voltage and current required by the load. Energy-efficient digital complimentary metal oxide semiconductor (CMOS) circuits operate off a supply voltage at or below 1 V, and most biomedical applications require currents between a few microamps to a few milliamps. To generate these voltages from a higher-voltage battery, a step-down (buck) converter is required. When only a small step-down is required, a low drop-out linear regulator is a simple and robust approach; however, for a large step-down, the efficiency of an LDO is poor and switching regulators are preferred.

Micropower switching converters have demonstrated efficiencies greater than 80% for loads down to 1 μW (33). The two main voltage converter topologies are switched capacitor–based and inductor/transformer–based switching converters. These converters can be configured in both step-down (buck) and step-up (boost) configurations. The power conversion efficiency of a switching converter is dictated by the following equation:

$$\text{Efficiency} = \frac{E_{load}}{E_{load} + E_{conduction} + E_{switching} + E_{parasitics} + E_{control} + E_{leakage}} \times 100\%. \quad (1)$$

In Equation 1, E_{load} represents the energy delivered to the load per switching cycle, and the other denominator terms represent sources of energy loss. At ultralow-power levels, leakage and control losses can significantly degrade overall efficiency and thus must be minimized. Simple control loops must be designed that allow for scaling power consumption with output power. Leakage can be mitigated through on-chip power gating and voltage scaling. Finally, high-quality passive components and switches are required for maximum efficiency. **Figure 3** shows simplified circuit implementations for step-down switched capacitor– and inductor-based converters and highlights the key sources of efficiency losses.

For highly integrated implantable applications requiring microwatt power levels, switched capacitor voltage converters are an effective approach. Switched capacitor converters can be integrated on the same silicon chip with other processing and communication circuits without external components, allowing for a compact system realization. As the output voltage is dictated by fixed

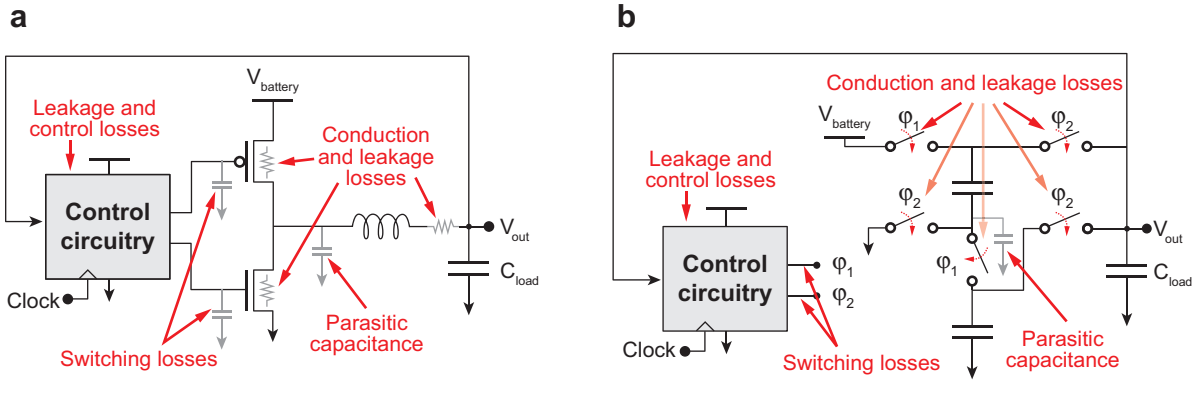


Figure 3

Circuit implementations of (*a*) inductor-based and (*b*) switched capacitor–based step-down converters. Key sources of efficiency losses are indicated.

Dynamic voltage scaling (DVS): a method to achieve energy savings by dynamically varying the voltage supplied to an electronic circuit, thereby reducing power consumption through a combination of reduced active and leakage energy

capacitor ratios, the majority of capacitive voltage converters have a limited, discrete set of output voltages. The implementation of dynamic voltage scaling (DVS), to reduce power consumption, requires variable supply voltages. Switched capacitor converters can be enhanced with additional switches and capacitors to be able to realize sufficient granularity of output voltages for DVS (34). Switched capacitor converters are used in implantable pacemakers to generate the 5 V supply that is used to stimulate the heart muscle (1, 35).

At power levels in the tens of milliwatt range and above, external inductors and capacitors are usually required to realize efficient voltage converters. At these power levels, inductor/transformer-based converter architectures are preferred to switched capacitor converters due to their high efficiencies and ability to generate arbitrary output voltages. Inductor-based converter architectures are simple to realize, requiring only a few digital switches, an output filter, and control circuitry (36). Transformer-based switching converters are used in cardioverter-defibrillators, which use a buck-boost flyback converter to generate 750 V pulses to shock the heart (37). Ultimately, with proper circuit design, both switched capacitor converters and inductor/transformer-based converters can efficiently power portable and implantable biomedical devices.

3.2. Ultralow-Power Signal Processing

The types of processing operations required for biomedical devices include filtering, spectral analysis, correlation, threshold/envelope detection, modulation, and data compression. Further, in all cases, the transfer functions must adapt to the perceptions and responses of individual users. As a result, a high degree of programmability in the defining parameters is critical. Generally, two processing domains exist: analog and digital. Hybrid approaches, where the strengths of one processing domain are used to assist the other, also exist for specialized applications (38, 39). Broadly, however, analog signal processing is governed by the rich input-output characteristics of transistors. On one hand, as described in Section 3.2.1, certain complex computations can be performed very efficiently by exploiting these (40); however, sensitivities to environment, biasing, noise, and variation limit their dynamic range. Digital signal processing, on the other hand, quantizes the signal to margin against these sensitivities, but requires additional hardware to process the quantization residue. Here, the need to convert physical analog signals into digital signals with the appropriate resolution, via analog-to-digital conversion, is unavoidable. Because this can be a high-power operation, analog preprocessing should be considered to reduce the ADC dynamic-range or sampling rate requirements.

3.2.1. Low-power analog signal processing. Critical considerations for analog circuits are the power cost of increasing dynamic range and the inconsistency in precise device behavior. The human ear, for instance, can detect sounds ranging from minute air vibrations, on the order of a tenth of an atomic diameter, to noises at the threshold of pain, representing over 110 dB of dynamic range. In analog circuits, however, large-signal excursions alter device operating conditions, resulting in nonlinear distortion, and small-signal excursions are indecipherable due to fundamental device noise. Unfortunately, in advanced technologies, the linear range is decreasing rapidly due to voltage limitations that the fine device features can withstand. Simultaneously, increasing the signal-to-noise ratio (SNR) fundamentally requires a quadratic increase in power. Consequently, selective device biasing and circuit topologies are required to perform analog computations efficiently. Moreover, as many biosignals of interest are at low frequencies, circuits are highly susceptible to 1/f and popcorn device noise. Techniques, such as chopper stabilization and correlated double sampling (41), which are used to cancel device parameter offsets, also help to manage these (42).

Sub-threshold operation. The transconductance behavior of a MOSFET, where an input voltage, V_{GS}, generates an output current, I_D, is critical to analog circuits. The threshold voltage, V_t, loosely separates the two regimes of V_{GS}, where I_D, for an NMOS, is given by Equations 2 and 3 (43), respectively:

$$I_D = I_0 e^{\frac{V_{GS}-V_t}{n\phi_{th}}}\left(1 - e^{\frac{-V_{DS}}{\phi_{th}}}\right) \quad : \quad V_{GS} \leq V_t \tag{2}$$

$$I_D = k'\frac{W}{L}\left((V_{GS} - V_t)V_{MIN} - \frac{V_{MIN}^2}{2}\right) \quad : \quad V_{GS} > V_t \tag{3}$$

Here, I_0, k', and W/L are physical and geometric parameters, and $V_{MIN} = \min(V_{GS} - V_t, V_{DS}, V_{DSAT})$, to account for various operating conditions where the MOSFET behavior differs. In particular, V_{DSAT} represents an equivalent saturation voltage beyond which the speed of current carriers cannot increase due to excess scattering from impeding atomistic interactions.

Equation 2 has an exponential dependence on both V_{GS} and V_t; as a result, I_D reduces by more than an order of magnitude for every 100 mV decrease in $(V_{GS} - V_t)$, and the relative currents in sub-V_t can be very low for a given device width. Accordingly, the relative transconductance, g_m (which is defined as $\frac{\partial I_D}{\partial V_{GS}}$), is also low. Importantly, however, the transconductance efficiency, $\frac{g_m}{I_D}$, is highest in sub-V_t (44). The biasing current, I_D, sets the operating point of the transconductor and typically determines its power consumption because it must be held static to avoid output distortion. Therefore, sub-V_t has superior power efficiency. The associated cost is reduced circuit speed due to the lower absolute output current; however, for biomedical applications, where the processing bandwidths are typically less than 1 MHz, the speed is sufficient, particularly where V_{GS} is close to V_t. This operating point is particularly beneficial because $\frac{g_m}{I_D}$ improves very marginally in deep sub-V_t, but I_D continues to degrade rapidly.

Sub-V_t: operating region of a MOSFET where its gate-source voltage, V_{GS}, is less than the parameter threshold voltage V_t

Translinear circuit: circuit that exploits the exponential current-voltage characteristic of transistors to achieve large-signal linear operation

Linear analog circuits. The relationship in Equation 2 is nonlinear and would lead to severe distortion in analog processing blocks. Confining the operating region to a small linearized range would impose severe noise limitations, which require increased power to mitigate. Alternatively, translinear circuits take advantage of the exponential behavior of sub-V_t MOSFET and bipolar junction transistor (BJT) devices to achieve large-signal linear operation (45). Their use has proven useful for many biomedical applications: bandpass filters are used in silicon cochleae (5), programmable amplifiers and filters are used in cardiac sense-amplifiers for pacemakers (46, 47), and analog multipliers are used for contrast computation in silicon retinas (48, 49).

Second-order effects, particularly in MOSFET devices, alter the exponential behavior, however, and limit the practicality of translinear circuits. An alternate strategy for achieving linear transfer functions uses operational transconductance amplifiers (OTAs) in negative feedback. Here, high-gain, but nonlinear amplifiers ensure that the inputs to the nonlinear devices remain small, and therefore within their linear range. A critical consideration for feedback topologies is maintaining stability. Nonetheless, OTAs often provide a robust implementation, and programmability can be achieved by controlling their gain. Accordingly, OTA-based implementations have been demonstrated in the same biomedical applications as those mentioned for translinear circuits: Variable gain amplifiers and bandpass filters are used in silicon cochleae (6, 50), and cardiac sense-amplifiers and filters are used in pacemakers (51, 52).

Nonlinear analog circuits. Often the critical information in a biomedical signal is characterized by a few important parameters, such as sign, peak-value, etc. Rather than using linear processing to preserve the entire signal, extracting and processing only the useful parameters can lead to a more power efficient implementation. For instance, using peak-detectors and comparators, beat-to-beat

variability can be extracted from electrocardiogram waveforms to monitor heart condition (53), and spectral power can be determined from audio data to stimulate inner-ear electrodes in silicon cochleae (6). Both approaches greatly reduce the performance requirements of subsequent analog-to-digital conversion, and they are highly power efficient due to the ease of implementing the required operation with inherently nonlinear devices.

Active power: the power consumption in a digital circuit that is attributed to the charging and discharging of circuit nodes during logic transitions

Activity factor: the rate, per clock cycle, that a digital circuit node performs an energy-drawing transition (e.g., low to high transition)

3.2.2. Low-power digital signal processing. Because devices in a digital circuit have a large noise margin, they are robust to the distortion and noise effects plaguing analog circuits in advanced technologies. The ability to benefit accordingly from technology scaling trends has enabled elaborate digital architectures that are highly reconfigurable and energy efficient, offering great possibilities for biomedical devices. In fact, in some applications, entire signal processing algorithms are customized to suit patient perceptions (4, 54), or the performance, SNR, and even functionality are dynamically optimized to minimize power and area overheads (3, 55). Using the low-power techniques described in this section, the high level of agility afforded by digital circuits can be aggressively leveraged for general biomedical applications.

Digital circuit energy and performance. The dominant source of power in digital circuits is called active power, P_{ACT}, and is consumed during logic transitions when charge must be transferred from the supply voltage, V_{DD}, to the physical capacitance of a signal carrying circuit node, C_L. P_{ACT} for each node is given by $\alpha_{0\rightarrow1} C_L V_{DD}^2 f_{clk}$ (43). Digital logic gates conventionally perform a new computation every clock cycle; however, depending on the circuit functionality and implementation, transitions might not occur at the clock frequency, f_{clk}. Therefore, $\alpha_{0\rightarrow1}$ reflects the average number of $0\rightarrow1$ transitions per clock-cycle and can be greater than 1 due to glitches. The actual energy consumed for an entire function, which is a relevant metric with regards to the energy constraint, can be determined by summing the total capacitance that transitions during the course of the operation, $C_{TOT} = N\sum_{i=All\ Nodes} \alpha_{0\rightarrow1} C_{L,i}$, where N represents the number of clock cycles required to complete the function. Then, the total active energy is given by

$$E_{ACT} = C_{TOT} V_{DD}^2. \quad (4)$$

From Equation 4, reducing the supply voltage yields significant energy savings but comes at the cost of reduced performance due to lower output currents available to switch the circuit node capacitances. **Figure 4** considers a simple digital circuit and shows the impact of scaling V_{DD} on delay and energy. In biomedical applications, the reduced performance that comes with voltage scaling is often acceptable because the accompanying energy savings are so significant (56).

More generally, however, in some real-time applications, system-level throughput constraints, modest as they may be, must be met. In such cases, parallelism, combined with voltage scaling, can be employed to simultaneously achieve the required performance and energy efficiency (56). Here, a hardware unit is replicated M times, so each unit can operate at a frequency reduced by a factor of M, while maintaining the same overall performance. The reduced frequency per unit, however, enables voltage scaling and improved energy efficiency. Of course, the necessity of interface combiners imposes additional overhead; nonetheless, often system partitioning and algorithm redesign allow for highly parallelized implementations with very low overhead (57).

It should be noted that architectural and algorithmic techniques have also been developed and widely used to reduce energy by minimizing $\alpha_{0\rightarrow1}$ (58). For example, balancing logic delays from timing-path inputs can avoid glitching, and optimizing logic function implementations, while considering the input signal statistics, can result in a reduced amount of total switching (59).

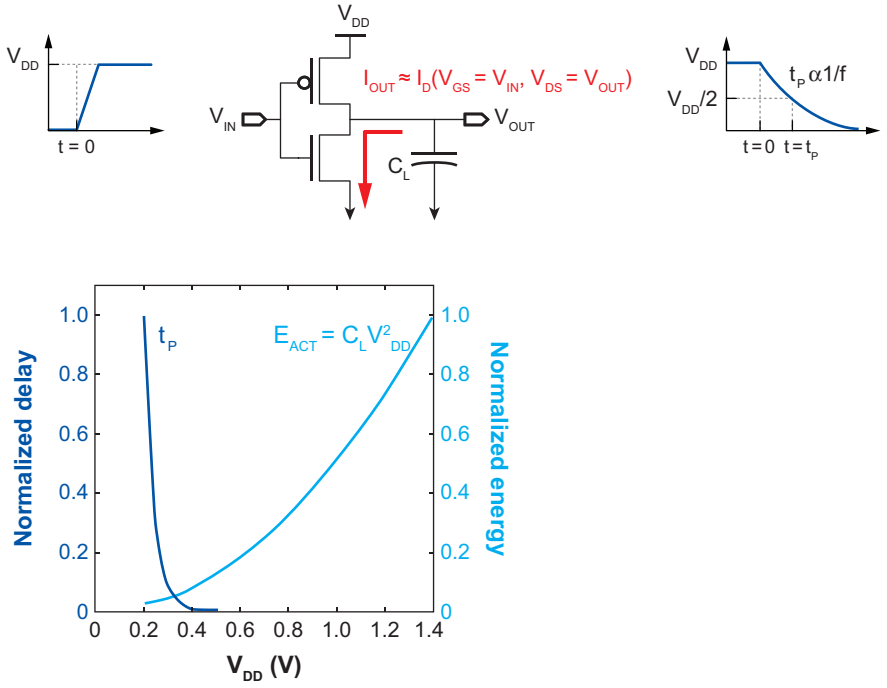


Figure 4

Circuit delay and active energy of a digital circuit with respect to supply voltage.

Dynamic voltage and frequency scaling. A low-power design model for many biomedical implantable and wearable devices, including biosensor networks (60), consists of reactive nodes that perform only minimal monitoring operations for the vast majority of the time. On detection of an event, their operational state is elevated to execute the appropriate signal processing along with actuation or data transmission. In either case, the performance demand, or workload, increases instantaneously. While circuits operating statically at a reduced voltage cannot accommodate the performance increase, a widely used technique is to dynamically increase their voltage (61). As shown in **Figure 5**, this approach utilizes a voltage controlled oscillator (VCO) to set the circuit's operating frequency and a voltage regulator to optimally set V_{DD} (62). The VCO replicates the critical speed-limiting signal path in the digital circuit, ensuring that its period is sufficient for the circuit delays at any given V_{DD} (63). The loop works by comparing an input reference clock, which sets the desired frequency based on the system performance constraint, with the VCO frequency. If the VCO frequency is lower, the controller issues a command to the voltage regulator to increase V_{DD}, which subsequently increases the VCO and circuit frequency; if the VCO frequency is higher, the opposite command is issued until the circuit frequency eventually matches the reference. An alternative approach uses a lookup table to map desired circuit performance to a predetermined V_{DD}; here, the regulator V_{DD} can be immediately set in a feed-forward manner (62).

Standby mode power reduction. Minimizing circuit node activity, $\alpha_{0\to1}$, is also an effective method for reducing active power. A simple architectural solution is to partition designs into fine-grained functional blocks and implement independent standby modes for each, as shown in **Figure 6**. Then, during standby, the local clock (*LCLK*) can be gated, prohibiting logic transitions (i.e., $\alpha_{0\to1} = 0$) and eliminating active power consumption.

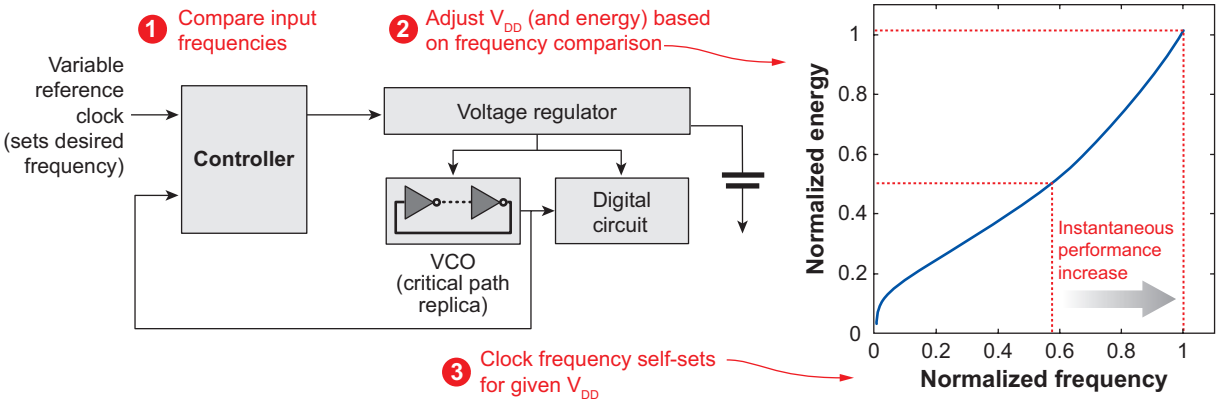


Figure 5

Achieving selectable performance states using a dynamic voltage-scaling loop.

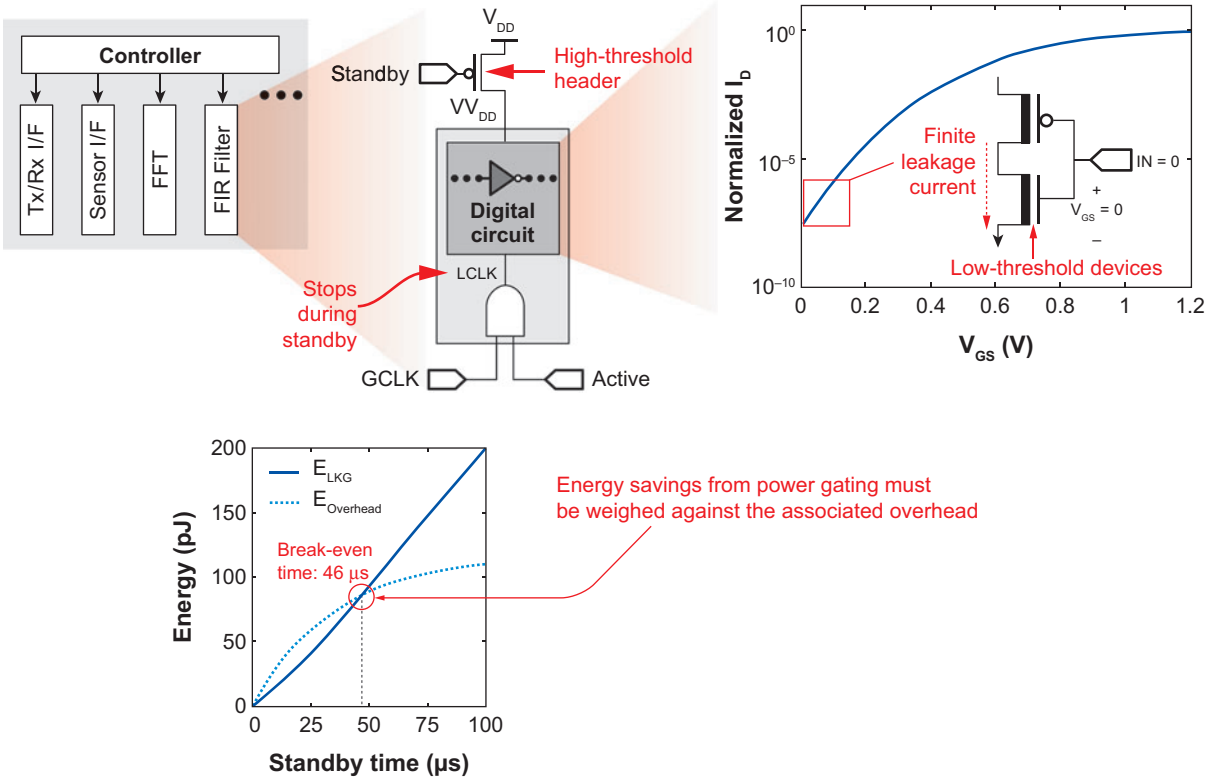


Figure 6

Fine-grained clock and power gating to eliminate active and leakage power during local standby modes (courtesy N. Ickes, MIT).

The power reduction techniques described thus far only address active power. In standby, however, an additional source of power, leakage power, P_{LKG}, becomes significant. P_{LKG} refers to idle-mode current that flows while logic circuits are in a high or low state, and it is particularly prominent in advanced technologies, where, by design, V_t is low in order to maximize performance. As shown in **Figure 6**, even when V_{GS} is reduced to zero, some finite leakage current continues to flow. To eliminate it, the supply voltage must also be gated using high-threshold header devices that have much lower leakage current (64, 65). Of course, header device control, as well as power-supply voltage (VV_{DD}) recovery after standby, has some associated energy overhead, $E_{Overhead}$. A simulation of $E_{Overhead}$, as well as the circuit's leakage energy, E_{LKG}, is shown in **Figure 6** for a finite impulse response (FIR) filter implementation after entering standby (at $t = 0$). Power-gating only saves energy in this example if the duration of the standby mode exceeds the break-even time of 46 μs, and it should not be applied for shorter periods of inactivity.

Leakage power: the power consumption in a circuit that is attributed to sub-V_t conduction even during periods of circuit inactivity

Minimum energy sub-threshold operation. When aggressive voltage scaling is employed, such that the supply voltage is near or below the MOSFET threshold voltage, the resulting leakage energy becomes significant even during normal circuit operation because the circuit delay increases exponentially. In this scenario, the power supply cannot be gated until the operation is complete, and the leakage power integrates over the operating time. Consequently, E_{LKG} is given by Equation 5:

$$E_{LKG} = \int_{Op\ time} P_{LKG}\, dt. \tag{5}$$

Although scaling V_{DD} is highly effective for reducing E_{ACT}, the circuit delay increases rapidly at very low voltages (as shown in **Figure 4**) and E_{LKG} increases correspondingly. The opposing energy trends are shown in **Figure 7** for a 32b adder, and they give rise to a minimum total energy voltage (66). Importantly, this minimum energy voltage occurs in the sub-V_t regime (i.e., V_{DD} of 0.3–0.4 V) for most practical digital circuits, and the energy savings exceed an order of magnitude compared with the nominal supply voltage. For instance, a scalable fast Fourier transform (FFT) processor, which can provide spectral energy computation for silicon cochleae, operates at a minimum energy voltage of 0.35 V consuming 155 *nJ/FFT*, over a 15x reduction compared with the nominal V_{DD} energy (67). Using parallelism and pipelining, the corresponding clock frequency of 10 kHz can support the 1 *kFFT* s^{-1} throughput requirement of implantable speech processors.

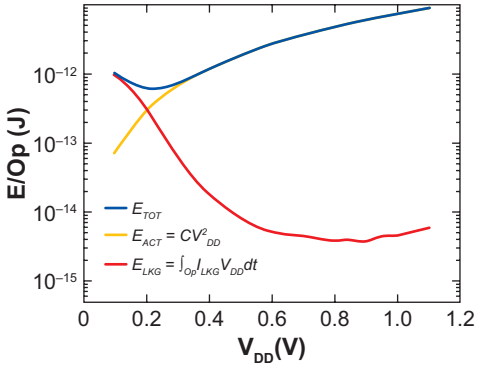


Figure 7

Minimum energy voltage resulting from opposing active and leakage energy profiles.

SNM: static noise margin

Ultralow-voltage design challenges. Aggressive voltage scaling into sub-V_t requires special circuit topologies and design methodologies to address two fundamental challenges: V_t variation and degraded I_{ON}/I_{OFF}. With the extremely fine device dimensions of advanced technologies, a countable number of atoms interact to set the device parameters, and small fluctuations, known as random dopant fluctuation (RDF) (68), and process-control limitations prominently affect V_t. Consequently, I_D, due to its exponential dependence on V_t (see Equation 2), varies overwhelmingly, prohibiting circuit topologies that rely on relative device strengths. Additionally, because the absolute currents are low in sub-V_t, the I_{ON}/I_{OFF} ratio is degraded by three to five orders of magnitude compared with nominal supply voltages. As a result, the interaction between both "on" and nominally "off" devices becomes important in setting node voltages.

The resulting behavior of logic gates degrades dramatically. **Figure 8*a*** shows how the voltage transfer characteristic (VTC) of an inverter deviates due to global variation, resulting from process control limitations, and local variation, resulting from RDF. The effect is even worse for more complex logic gates, such as NANDs, where the output low level can be degraded by a weakened series path that must fight a strengthened parallel path. **Figure 8*a*** shows the resulting histograms for the logic low level of a NAND gate in the presence of variation and the logic high level of a NOR gate, which faces the complementary problem. Accordingly, to avoid logic level failures, gates must be upsized appropriately to reduce the effects of RDF (69).

Static random access memories (SRAMs) pose the first failure point in low-voltage designs because, to maximize density, they rely on ratioed circuits and shared nodes that are subject to many parallel leakage paths. The commonly used six-transistor (6T) storage-cell is analyzed in **Figure 9**. Data are written by asserting the word-line (WL) to enable the access devices *M5/6*, which must be strong enough to overpower the local feedback. However, in sub-V_t, the relative strengths cannot be guaranteed due to variation. Similarly, data are read by precharging the bit-lines, *BLT/BLC*, and detecting a discharge caused by the series combination of *M1/2* and *M5/6*. Due to the initial precharge, however, transients can disturb the internal storage nodes, *NT/NC*. The analysis can be formulated by assuming that *BLT/BLC* are at V_{DD}, and *M5/6* essentially fight *M1/2*, tending to raise the voltages at *NT/NC*. In the extreme case, the storage node that should be low can flip state, causing a read-upset. Margin against this effect, called the static noise margin (SNM) (70), is quantified by examining the butterfly plots, where the transfer function from

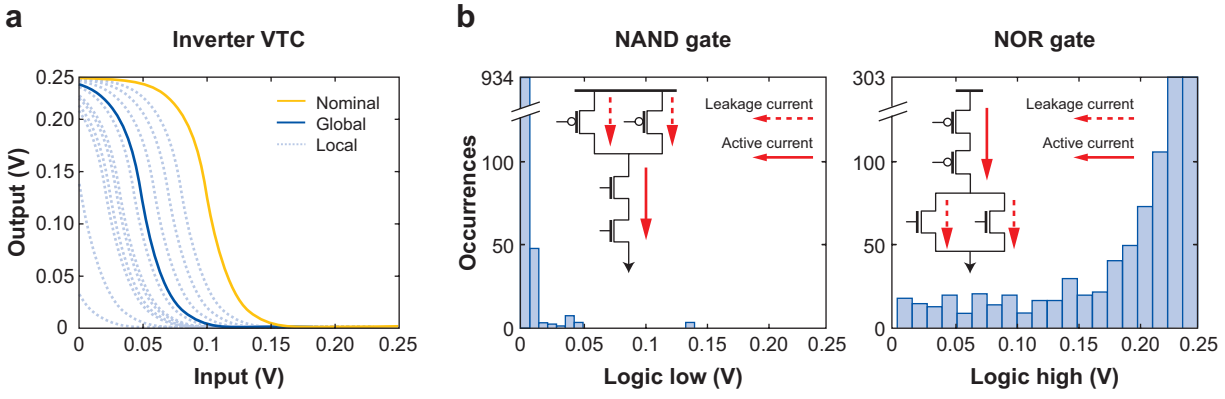


Figure 8

Output logic level degradation in a digital gate in a 65 nm complimentary metal oxide semiconductor (CMOS) technology shown as (*a*) variation in the voltage transfer characteristic (VTC) and (*b*) logic low and high histograms for NAND and NOR gates respectively (courtesy J. Kwong, MIT).

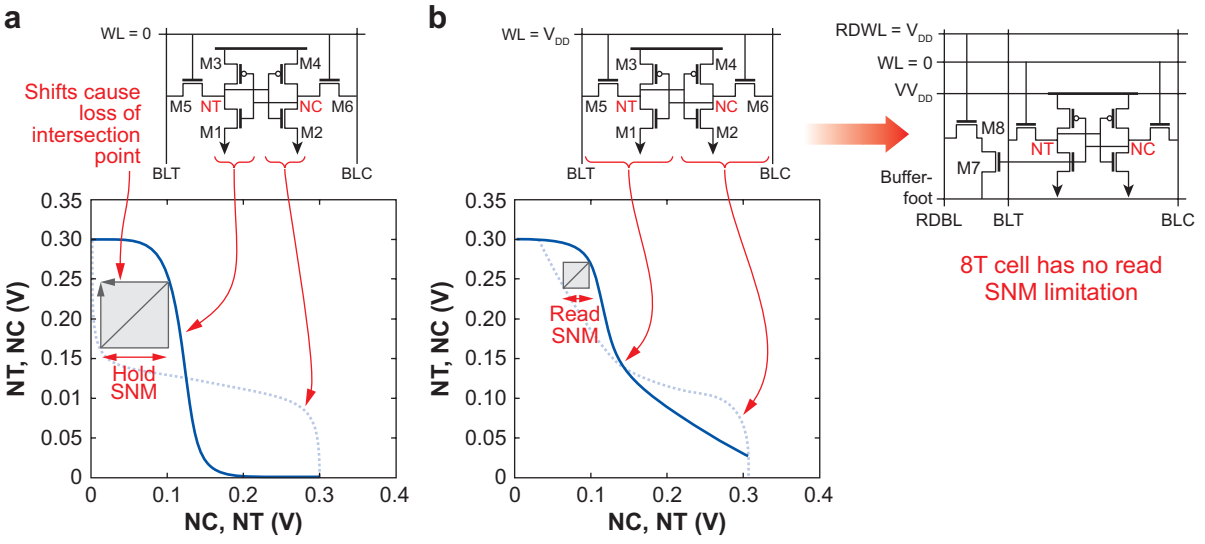


Figure 9

Bit-cell butterfly plots showing (*a*) 6T hold static noise margin (SNM) and (*b*) 6T read SNM, which is eliminated in the 8T cell described in Reference 71.

NC-NT is superimposed on the transfer function from *NT-NC*. In **Figure 9*a***, the presence of three intersection points indicates that both digital states can be stably stored, and a third, midstate can exist only meta-stably; small perturbations will cause its value to regenerate to one of the two stable states. If, however, variation is severe enough to shift both curves by an amount equal to the edge length of the largest embedded square, one of the intersection points is lost, indicating inability to hold the associated data state. Importantly, as shown in **Figure 9*b***, the read SNM is considerably smaller than the hold SNM and, therefore, limits low-voltage operation.

An alternate 8T storage-cell that operates down to sub-V_t is also shown in **Figure 9*b*** (71). Here, reads are performed on a separate port via the read bit-line (RDBL), so the storage nodes can be isolated, eliminating the read SNM limitation. To maximize density, many cells can share RDBL, and when unaccessed, their leakage currents are gated by properly controlling Buffer–Foot from the array periphery. Last, to enforce the relative strength of *M5/6* over the storage devices during a write operation, the cell supply voltage VV_{DD} is appropriately reduced using a peripheral supply driver. Hence, the hazards of parallel off devices imposing bit-line leakage and variation skewing the relative strengths required for writeability are both avoided to achieve full operation to below 0.35 V. The resulting savings in leakage power are over a factor of 20 compared with operation at 1 V.

3.3. Analog-to-Digital Conversion

DSP: digital signal processor

Because physical biomedical signals are analog, an ADC is required before they can be processed digitally to take advantage of the sophisticated capabilities of a digital signal processor (DSP). Precisely how much processing is done before the ADC is a matter of system-to-system optimization. ADC requirements depend on system characteristics, namely bandwidth and dynamic range, so system optimization must consider ADC power, which can be a significant portion of the total

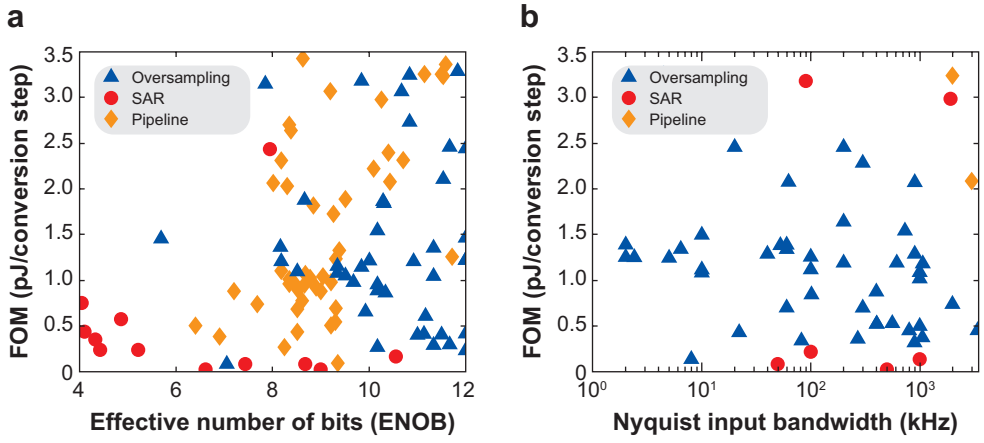


Figure 10

Figure of merit (FOM) for reported analog-to-digital converter (ADC) with respect to (*a*) effective number of bits and (*b*) sampling-rate (courtesy B. Ginsburg, MIT).

power. As one might expect, the energy per conversion, which is an important metric for ADCs, increases as the dynamic range and sampling rate requirements increase. An empirical figure of merit (FOM) for ADCs normalizes their power consumption to the Nyquist sampling rate, F_S, and the dynamic range, expressed as 2^{ENOB} (where *ENOB* is the effective number of bits output) (72):

$$FOM = \frac{P}{2^{ENOB} F_S}. \quad (6)$$

Scatter plots of the FOM for reported ADCs are shown in **Figure 10** for the *ENOB* and sampling rates of interest in most biomedical applications. State-of-the-art converters today achieve an FOM of as low as 4.4 fJ per conversion-step (73); however, generally, dynamic ranges beyond those yielded by eight-bit converters have a steeper power increase due to device noise limitations in the ADC circuits; the same is true when sampling rates exceed tens of megahertz because devices must be biased further above V_t. Based on observed trends, successive approximation register (SAR) and oversampling ADCs achieve the optimal FOM for most biomedical applications, but pipeline converters may be required for some high-speed biomedical systems.

Successive approximation ADC. A typical implementation of a SAR ADC is shown in **Figure 11*a***, where the sample and hold (S/H) and digital-to-analog converter (DAC) are implemented as one capacitor array; during input acquisition, the negative of the input voltage is sampled on the top-plates, and, subsequently, during the conversion the binary weighted capacitors are successively switched between ground and V_{DD} by a digital controller, performing a binary search that eventually converges to the digital output code. Importantly, all components, except the comparator, are either passive or digital. Accordingly, the voltage scaling and clock-gating approaches discussed in Section 3.2.2 enable micropower SAR implementations (73, 75).

The comparator, particularly in high-resolution SAR converters, whose gain requirements are immense, often dominates power consumption. However, as mentioned in Section 3.2.1, because of its nonlinear operation, it can be highly power efficient. In particular, it can leverage regeneration, where a single-stage amplifier continuously feeds back its output to enhance a slight input perturbation (76). Unfortunately, regenerative structures typically suffer from large input

SAR: successive approximation register

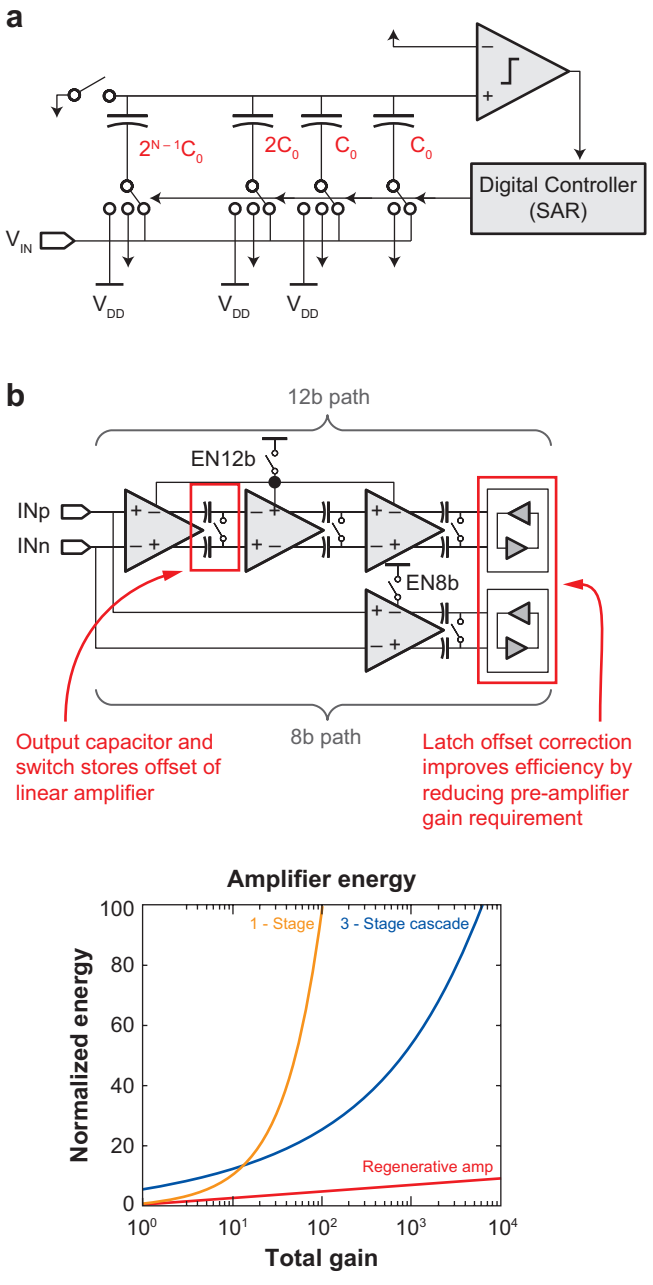


Figure 11

Successive approximation register analog-to-digital converter (SAR ADC) (*a*) block diagram and (*b*) comparator implementation employing latch offset correction to improve efficiency (73).

offsets, and, where absolute analog-to-digital conversion is required, less efficient nonregenerative preceding amplifiers, whose offsets can be corrected, are used. Alternatively, offset compensation can be used as in the regenerative latch as described in Reference 73 and shown in **Figure 11*b***. First, two paths are used here to select between a high-resolution 12b mode and a low-power 8b mode for dynamic power-performance scaling. Second, in both cases, the gain requirement of the less-efficient linear preamplifiers is reduced by offset compensation in the regenerative latch.

Within the latch, multiple feedback loops are used to store the offset correction biasing on an auxiliary input, such that the latch can be reset without requiring an explicit autozeroing input reference before every decision. Importantly, all of the feedback structures reuse the same bias current, leading to a highly power-efficient implementation.

Oversampling ADC. Oversampling converters use a low-resolution ADC (e.g., 1-bit) whose output is subtracted from the input sample and integrated; the output of the integrator is repeatedly converted (commonly up to 256 times) so that the average of all ADC conversions is a high-resolution digital representation of the input. Because only a low-resolution ADC is required, which can be implemented with a comparator, this architecture can be highly power efficient. Typically, the integrator is implemented with an OTA; however, its linearity is not critical, and therefore its power consumption can be acceptable. Further, highly digital implementations of the averaging decimation filter and comparator imply that advanced power management can benefit the efficiency and scalability of oversampling ADCs considerably (3). Unfortunately, however, because they require many samples for each conversion, one-time biomedical events can not be detected, limiting their applicability somewhat.

High-speed ADC. To achieve increased ADC performance, the approach of parallelism, introduced in Section 3.2.2 for digital circuits, can be applied. An efficient architecture, such as the SAR ADC, can be time-interleaved, with each channel operating closer to sub-V_t (77, 78).

With time-interleaved converters, however, mismatch and timing skew between channels can cause significant degradation in the overall performance. Alternatively, a pipeline architecture can be used where each bit is converted by a separate stage that also amplifies the residue voltage by 2 and passes the result to the subsequent stage for further conversion (79) (generally, each stage can convert any number of bits, but for simplicity, a 1 bit per stage example is discussed here). Because each input sample is processed by the same sequence of stages, mismatch and timing skew are precluded. Unfortunately, however, the need for precise gain-by-2 has conventionally required highly linear OTAs, as shown in the configuration of **Figure 12*a***, which, as mentioned in Section 3.2.1, can consume a lot of power. Effectively, the OTA applies negative feedback to force all of the sampled residue voltage charge from $C1$ on to $C2$, giving an output voltage of $2V_{IN}$.

An emerging approach that replaces OTAs with more power-efficient comparators is shown in **Figure 12*b*** (80). Here, instead of driving the output with an OTA, the current source charges it until the comparator's input voltage ramps to zero. Subsequently, the comparator trips, and the current source is disabled with the output at $2V_{IN}$. As mentioned in Section 3.2.1, the nonlinear comparator can be implemented far more efficiently and its performance scales more favorably with advanced technologies. Other ADC architectures have also been mapped to pipelined stages for enhanced conversion rate; in Reference 81, for instance, time-based conversion and processing are performed at each stage without OTAs, increasing the performance of integrating ADCs.

3.3. Communication Transceivers

The communication subsystem allows a biomedical device to send and receive information to and from other devices. This information can serve as commands, such as configuration instructions, or data, such as samples from a sensor. For many basic applications, the communication link can be realized with a wired connection. Two existing wired applications are the connection between a pacemaker to its pacing leads and the connection between a pulse oximeter and a finger-mounted

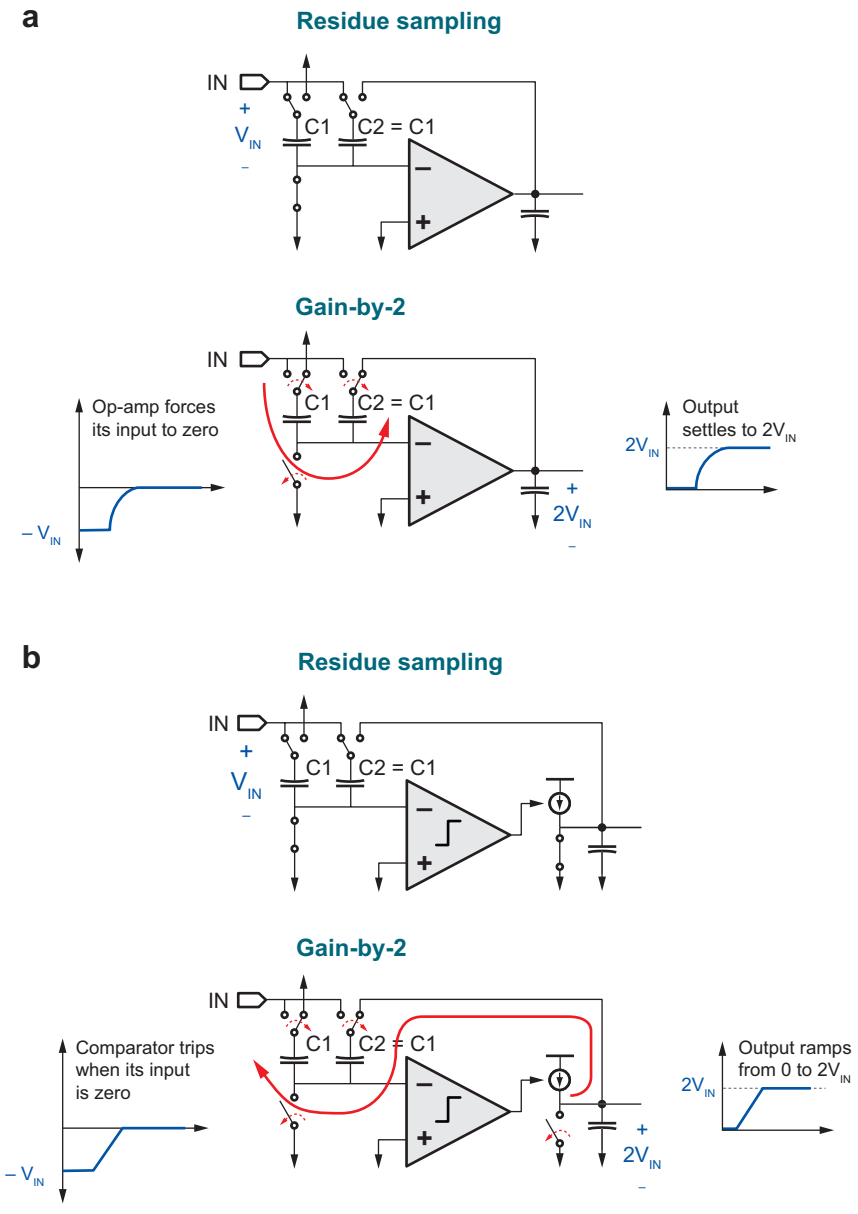


Figure 12

Pipeline stage implemented with (*a*) operational transconductance amplifier (OTA) and (*b*) comparator (80).

sensor (1). Due to the limitations of wired links, wireless communication is the dominant method of communication for biomedical devices.

The primary method of wireless communication is via electromagnetic waves through the air, either via low-frequency, near-field inductive coupling or higher-frequency, far-field wireless transmission. An alternate, emerging approach is to use the human body as a transmission medium (82). These systems typically involve attaching electrodes to a user's skin that communicate via

electrostatic coupling (83), electromagnetic waves (84), or electrooptic conversion (85). This section focuses on electromagnetic communication. However, the low-power techniques described can be applied to all communication systems, regardless of the transmission media.

3.4.1. Near-field electromagnetic wireless communication. Near-field communication operates on the principle of electromagnetic induction between two nearby coils, and is nearly identical to the concept of wireless power transfer described in Section 3.1.1. A key difference, however, is that while power transfer forms a unidirectional link, data transfer is often bidirectional, consisting of a forward and a reverse link. For implanted systems where one side of the communication link is volume and energy constrained, the forward link can consist of a high-powered transmitter that transmits both power and data, whereas the reverse link transmits only data. Due to the volume and energy constraints facing implanted systems, near-field communication links are typically limited in range to a few centimeters.

One example application of near-field communication is for data and power transfer from an external cochlear speech processor to its associated implanted stimulator (86). This application requires data rates on the order of 1 Mbps and a distance of only a few centimeters, operating at carrier frequencies such as 49 MHz (87). For emerging biomedical applications, such as neurostimulators and artificial retina, higher data rates are required. To support such high data rates using near-field communication, the wireless link requires higher bandwidths, necessitating lower-quality factor antenna coils. Data rates up to 2.5 Mbps have been demonstrated using coherent frequency shift keying with carrier frequencies of 5 and 10 MHz (88). An alternative method to achieve high data rates is via far-field electromagnetic wireless communication.

3.4.2. Far-field electromagnetic wireless communication. To realize high data rates at communication distances longer than a few centimeters, far-field electromagnetic communication is preferable to near-field communication. Far-field communication links for biomedical devices operate at carrier frequencies of hundreds of megahertz and above. The majority of low-power wireless transceivers are half-duplex where data transmission and reception do not occur simultaneously, and thus there is a transmit/receive switch connecting either the transmitter or receiver to the antenna.

Wireless standards. A key trend in far-field wireless communication is the emergence of standards that ensure coexistence or interoperability between devices. Early biomedical devices used ad-hoc, propriety communication protocols with only basic coexistence support. As biomedical devices become more prevalent, these proprietary radios are becoming less practical and more expensive than standards-compliant radios. Key low-power standards for biomedical devices are MICS, WMTS, Bluetooth (IEEE 802.15.1), and Zigbee (IEEE 802.15.4). Of these standards, Bluetooth and Zigbee require interoperability, whereas MICS and WMTS only require coexistence.

Energy-efficient circuits and systems. All of the aforementioned standards occupy a low-power, short-range space that is significantly different than cellular standards. As energy is highly constrained, emphasis is placed on minimizing the energy per bit of the radio, corresponding to the amount of energy required to transmit or receive a bit of data. For a given transmitter or receiver, energy per bit can be calculated with the following equation:

$$\text{Energy per bit} = \frac{\text{Power}}{\text{Data rate}} + \frac{\text{Power} \times (\text{Turn-on} + \text{Turn-off time})}{\text{Packet length in bits}}. \quad (7)$$

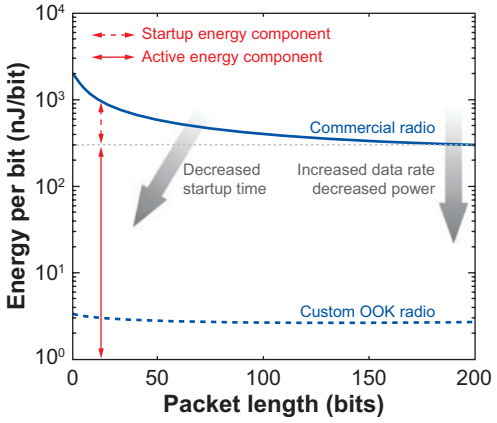


Figure 13

Energy per bit of commercial 802.15.4 receiver compared to a custom on-off keying (OOK) receiver (89).

To minimize energy per bit for a wireless transceiver, optimizations must be made to reduce the turn-on/off time and power consumption of the radio while concurrently increasing the data rate and packet length. At the system level, one effective approach to minimize energy per bit is by aggressively duty cycling a radio operating at a fast instantaneous data rate. This results in energy savings because radios at high data rates typically consume less power per bit than low-data-rate radios. However, at high data rates, losses due to the turn-on/off time become more significant and must be minimized relative to total time the radio is on.

The effects of increasing data rate and reducing turn-on time are shown in **Figure 13**, where the energy per bit of a commercial 802.15.4 receiver is compared with a custom on-off keying (OOK) receiver (89). Whereas the commercial 802.15.4 radio operates at 250 kbps and requires 320 μs to turn on, the custom OOK radio operates at 1 Mbps and requires 2.5 μs to turn on in receive mode.

The OOK radio uses noncoherent communication to reduce circuit and architectural complexity. When there is sufficient margin in the link budget, choosing a noncoherent modulation instead of a coherent modulation can result in significant energy savings. Noncoherent communication does not encode information in the carrier phase and instead encodes information in the carrier frequency and/or amplitude. This allows for significantly reduced architectural complexity at the cost of reduced link margin. For highly energy constrained systems where power consumption is dominated by transceiver fixed power consumption rather than transmitter output power, the power savings afforded by noncoherent communication is often worthwhile (89).

To minimize power consumption while achieving fast start-up time, the OOK receiver has an envelope detection-based architecture with a highly scalable radio-frequency (RF) front-end. By using an envelope detector, no high-frequency oscillator or phase-locked loop is required by the receiver in contrast to a traditional direct conversion receiver architecture. This allows for reduced power consumption and a fast turn-on time of 2.5 μs. The receiver power consumption can be scaled depending on link requirements, scaling from 0.5 mW to 2.6 mW, with an associated sensitivity of −37 dBm to −65 dBm at a bit error rate (BER) of 10^{-3}. The transmitter consists of an oscillator, mixer, and power amplifier and avoids the need for a phase-locked loop by stabilizing the oscillator with a surface acoustic wave (SAW) resonator.

A key challenge for implanted radios is to minimize the overall volume of the antenna and circuits while still achieving low-energy operation. The limited size of the antenna combined with the

OOK: on-off keying

Noncoherent communication: a communication method that does not encode information in the carrier phase and instead encodes information in the carrier frequency and/or amplitude

RF: radio-frequency

Ultrawideband (UWB) communication: communication based on wireless signals with bandwidths exceeding 500 MHz or 20% of the center frequency

lossy human body that surrounds it result in a poor antenna gain. A typical MICS band implanted antenna has a modeled gain of −35 dBi resulting from human body losses (90). To minimize the volume of the circuits, the transceiver must be as integrated as possible, requiring few if any off-chip components other than a crystal oscillator. Realizing compact, low-power transceivers is difficult because their high-frequency circuits often require off-chip filters, resonators, and passive components. Off-chip components, such as bulk acoustic wave (BAW) resonators, can allow for ultralow-power RF circuits but at the cost of increased volume (91); however, advanced packaging techniques, such as system-in-package or chip stacking, can mitigate this problem. A recent trend that promises to increase integration while decreasing power consumption is the emergence of the highly digital radio. A highly digital radio minimizes the use of external components and instead leverages advanced CMOS devices to realize equivalent functionality in less area and power.

A highly digital ultrawideband transceiver chipset has been recently demonstrated that can be adapted for use in biomedical devices (92, 93). A block diagram of the transceiver architecture is shown in **Figure 14**. Wireless communication is via the transmission and reception of short, 2-ns ultrawideband pulses in the 3-to-5 GHz frequency band. These ultrawideband (UWB) pulses are much wider in bandwidth and narrower in time than traditional narrowband signals. These wide bandwidths with relaxed frequency tolerances allow for highly digital architecture, as they are amenable to low-power integration in advanced digital CMOS processes (94). UWB signals can be efficiently amplified and processed with wide-bandwidth, low-Q circuits, which can be easily integrated on-chip with minimal area.

The transmitter uses an all-digital architecture and calibration technique to synthesize these pulses with programmable width and center frequency. Depending on the desired center frequency, the digital delay line is calibrated and the appropriate number of edges is selected. The transmitter consumes primarily CV_{dd}^2, switching energy at high data rates and requires 43 pJ to transmit a single pulse.

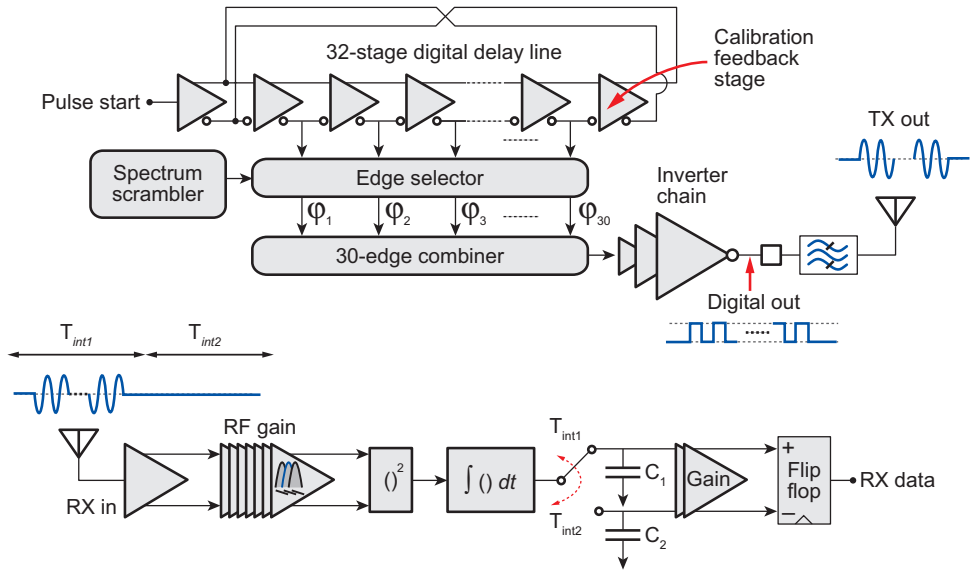


Figure 14

Block diagram of an ultrawideband (UWB) transceiver implemented in 90 nm complimentary metal oxide semiconductor (CMOS), incorporating an all-digital transmitter and an energy detection, noncoherent receiver (92, 93).

The receiver uses a noncoherent, integrating energy detection architecture. The receiver amplifies the appropriate UWB frequency band, filters out adjacent frequency bands, and squares the signal to generate an analog representation of the received signal power. By integrating the squared signal over a time period and storing this value on a capacitor, the receiver obtains a representation of the amount of received energy. Pulse-position modulation is employed and the receiver compares the amount of energy received in two adjacent time periods ($T_{\text{int}1}$ and $T_{\text{int}2}$) to determine whether a "1" or "0" was transmitted. The receiver architecture does not require a high-frequency phase-locked loop, as the only clock required is a low-frequency bit-decision clock. The receiver can turn on within 2 ns and requires 2.5 nJ bit^{-1}.

4. OUTLOOK AND CONCLUSIONS

Continued device scaling and integration have enabled dramatic reductions in energy consumption for the key building blocks of electronic biomedical devices. A system-level approach is required to reduce power consumption to microwatts, which is the power level limiting many biomedical applications. Architectures and circuits for biomedical devices should exploit application attributes to minimize energy dissipation. For example, the slow speeds inherent to biological systems allow processing blocks to operate in the sub-V_t regime to achieve an order of magnitude energy savings. Further savings can be achieved through careful partitioning between the analog and digital domains, as analog preprocessing allows for relaxed digital processing requirements but at the cost of increased design complexity and noise sensitivity. As most biomedical devices need only a short-range, low-data-rate wireless communication link, transceiver architectures can leverage techniques such as noncoherent communication and highly digital architectures. Energy to power the electronics should be collected from external sources, through methods such as electromagnetic energy transfer, and harvested from ambient sources, such as vibrations. Advances in miniature energy scavengers offer the promise of fully implanted, autonomous biomedical devices, enabling a broad range of exciting new applications.

SUMMARY POINTS

1. Energy is a highly limited resource in biomedical devices, particularly in implanted applications. A system-level approach is required to minimize power consumption and ensure maximum functionality.
2. Energy harvesting is an emerging technology that has the potential to remove the need for batteries in many biomedical devices. Key harvesting approaches suitable for biomedical devices include wireless, vibrations, and thermal.
3. At micropower levels, leakage and control losses significantly degrade the efficiency of DC-DC voltage converters. To minimize these, digital techniques such as power gating and frequency scaling can be applied to the DC-DC converter.
4. Analog and digital circuits have different strengths; analog circuits use the rich input-output behavior of transistors to perform area- and power-efficient computations, whereas digital circuits have superior robustness and scalability that enable elaborate and programmable architectures. The flexibility afforded by digital circuits also allows them to benefit from sophisticated power management, greatly improving their power efficiency.

5. Sub-V_t operation results in increased transconductance efficiency in analog circuits and reduced active power in digital circuits. As a result, it often leads to the most energy-efficient implementations, and their performance, which is greatly reduced due to the lower device currents, is usually sufficient for biomedical application requirements.
6. Digital circuit energy is dominated by active energy and, in sub-V_t, leakage energy. Active energy can be reduced by scaling the supply voltage or minimizing node transition activity. Leakage energy can be reduced by employing high-V_t MOSFETs to gate idle-mode currents during standby.
7. RDF is a primary barrier to ultralow-voltage design, particularly in SRAMs. To manage RDF, specialized topologies and careful circuit design must be employed.
8. SAR and oversampling ADCs provide the speed and resolution requirements for most biomedical applications and can achieve micropower operation for many such systems of interest.
9. Low-frequency inductive coupling can be used to supply power to an implanted device as well as allow for bidirectional communication.
10. The energy per bit for a wireless radio can be minimized through a variety of techniques, including operating at high instantaneous data rates and using simple architectures such as highly digital transmitters and noncoherent receivers.

FUTURE ISSUES

1. A standard electronics platform is required that is energy efficient and can be easily reconfigured to satisfy a broad set of biomedical applications.
2. As CMOS technology advances, subthreshold leakage is consuming an increasing percentage of overall power consumption. What techniques can be applied to mitigate this problem and how can devices be optimized for biomedical applications?
3. How can energy harvesting be improved to better harvest human motion and other ambient energy sources?
4. Biomedical systems require energy-scalable ADCs that can adapt resolution or speed for time-varying requirements. What are appropriate ADC architectures and topologies that allow for significant energy savings at reduced resolution and speed?
5. What is the optimal wireless protocol for body-area networks that allows for low-power, robust operation in a miniature form-factor?
6. Biocompatible packaging must be developed that allows for compact integration of MEMS energy scavenging, radio components (antennas, FBAR resonators, etc.), and CMOS-integrated circuits.

DISCLOSURE STATEMENT

The authors are not aware of any biases that might be perceived as affecting the objectivity of this review.

ACKNOWLEDGMENTS

The authors thank Professors Martha Gray, Hae-Sung (Harry) Lee, Jeffrey Lang, Joel Schindall, Jose Oscar Mur-Miranda, and David Wentzloff for their helpful discussions and correspondence. The authors also thank Joyce Kwong, Nathan Ickes, Yogesh Ramadass, and Brian Ginsburg for their technical assistance. This work is funded by DARPA, FCRP, and Texas Instruments.

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Volume 10, 2008

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