Ultralow-Power Smart Temperature Sensor with Subthreshold CMOS Circuits

Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya
Department of Electrical Engineering
Hokkaido University, Sapporo 060-0814 Japan
Tel: +81-11-706-6080, Fax: +81-11-706-7890
E-mail: k_ueno@sapiens-ei.eng.hokudai.ac.jp

***Abstract*— We proposed a smart temperature sensor LSI consisting of subthreshold CMOS circuits. The sensor was composed of a bias circuit, a PTAT current generator, an A/D converter, and a counter circuit. All of the circuits were designed so that MOSFETs in the circuits would operate in the subthreshold region to achieve ultralow power consumption. The PTAT current generator was the key component of the sensor and was constructed by using the characteristics of a MOSFET in the subthreshold region. Simulation with SPICE demonstrated that the circuit can be used as a smart temperature sensor with ultralow-power consumption of 6 μW or less.**

I. INTRODUCTION

In the near future, intelligence network systems with various smart sensors will be developed and spread over the world to construct infrastructures for the age of information. Such network systems require a huge number of sensor ICs that measure various physical data in our surroundings, store and process the measured data, and output the data on demand. These sensor ICs must operate with ultralow power because they will probably be placed under conditions where they have to get the necessary energy from poor energy sources such as microbatteries or solar cells.

In this paper, we propose one such sensor IC, a temperature sensor that can operate with a low power of microwatts or less. Many temperature sensors consisting of CMOS circuits have been reported [1-5] but are unsuitable for use in the intelligence network systems because of their large power consumption of several hundred microwatts. To achieve ultralow-power operation, we propose a temperature sensor IC that uses MOSFET circuits operated in the subthreshold region. Our sensor produces an output that is proportional to absolute temperature (PTAT output). In the following, Section II outlines the construction and operation of our temperature sensor, Section III describes the circuit implementation of the sensor, and Section IV illustrates the operation of the sensor with the results of SPICE simulation.

II. CONSTRUCTION OF THE SENSOR

Figure 1 shows a block diagram of the temperature sensor we propose. The sensor consists of a bias circuit, a PTAT current generator, and an A/D converter consisting of a CCO (current-controlled oscillator) and a counter. The bias circuit generates two voltages such that the difference of the voltages is independent of temperature. The PTAT current generator accepts the two voltages and produces a PTAT current in such a way described in the next section. The CCO accepts the PTAT current and produces oscillation pulses whose frequency is proportional to absolute temperature. The digital counter records the number of the oscillation pulses at short time intervals and outputs the recorded data, an AD-converted output. Thus, the circuit operates as a PTAT temperature sensor.

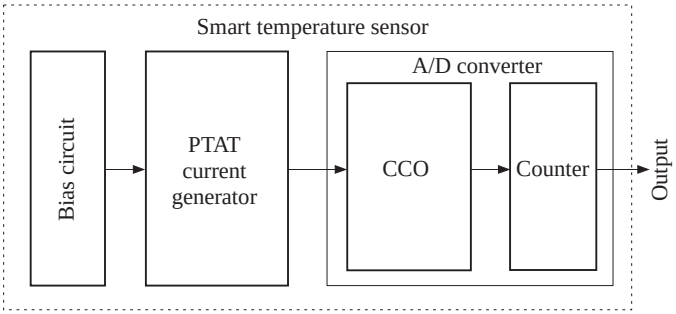

Fig. 1. Block diagram of the smart temperature sensor.

To achieve ultralow power consumption, all of the circuits in the sensor are designed so that MOSFETs in the circuits will operate in the subthreshold region . The key component of the sensor is the PTAT current generator. It makes use of the transfer characteristics of the subthreshold MOSFETs. The details of its operation are described in the following.

A. Generating a PTAT current

The subthreshold current I_D through a MOSFET is an exponential function of the gate-source voltage V_G and is given by

$$I_D = I_0 \exp\left(\frac{V_G - V_{TH}}{\eta V_T}\right), \tag{1}$$

where I_0 is a process-dependent parameter, η is the subthreshold slope factor, and $V_T(= k_B T/e)$ is the thermal voltage [6].

Making use of this subthreshold characteristic will enable us to produce a PTAT current as follows. Suppose that two MOSFETs are biased with two different voltages V_{G1} and V_{G2} to generate two subthreshold currents I_{D1} and I_{D2}. The

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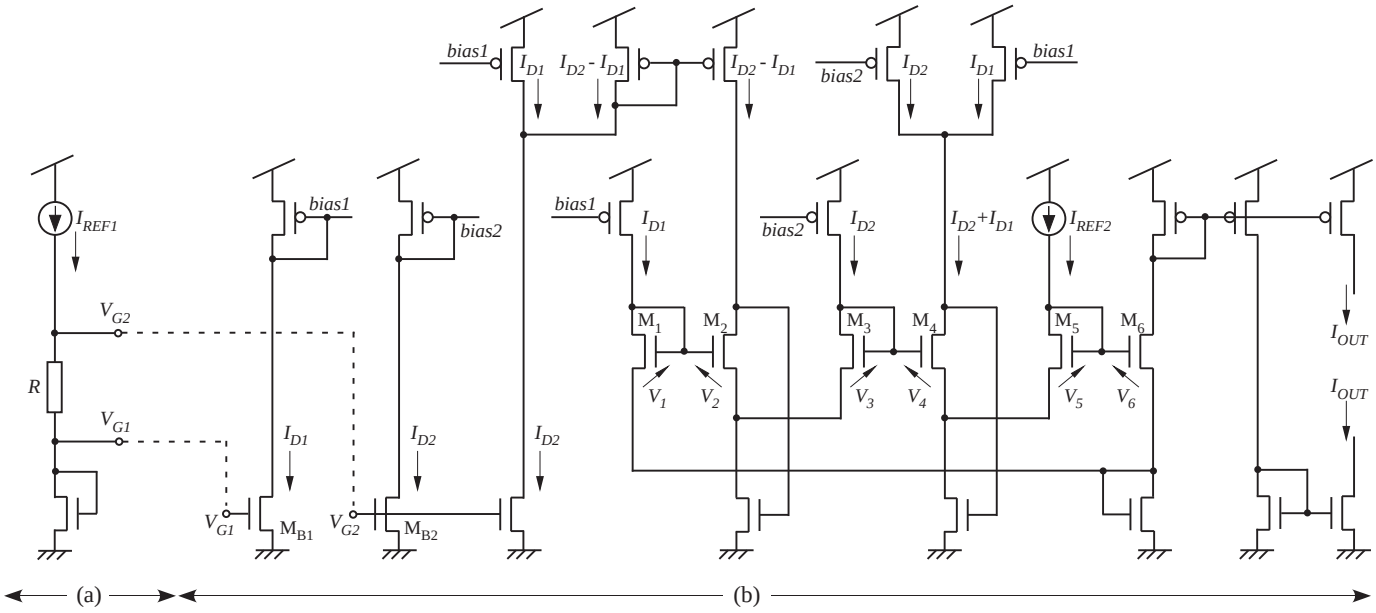

Fig. 2. (a) Bias circuit and (b) PTAT current generator, consisting of MOSFETs operated in the subthreshold region. I_{REF1} and I_{REF2} are constant currents independent of temperature.

ratio of the currents is given by

$$\frac{I_{D2}}{I_{D1}} = \exp\left(\frac{V_{G2}-V_{G1}}{\eta V_T}\right), \quad (2)$$

and

$$\frac{I_{D1}}{I_{D2}} = \exp\left(-\frac{V_{G2}-V_{G1}}{\eta V_T}\right). \quad (3)$$

For a voltage difference $|V_{G1} - V_{G2}|$ smaller than ηV_T, Eqs. (2) and (3) can be rewritten as

$$\frac{I_{D2}}{I_{D1}} = 1 + \frac{V_{G2}-V_{G1}}{\eta V_T}, \quad (4)$$

and

$$\frac{I_{D1}}{I_{D2}} = 1 - \frac{V_{G2}-V_{G1}}{\eta V_T}. \quad (5)$$

The difference between Eqs. (4) and (5) is given by

$$\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}} = 2\,\frac{V_{G2}-V_{G1}}{\eta V_T}. \quad (6)$$

The reciprocal of Eq. (6) is expressed as

$$\frac{1}{\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}}} = \frac{\eta V_T}{2(V_{G2}-V_{G1})} = \frac{\eta k_B}{2e(V_{G2}-V_{G1})}\,T. \quad (7)$$

This way, we can obtain a PTAT characteristic if voltage difference $|V_{G2} - V_{G1}|$ is independent of temperature. This PTAT characteristic can be implemented with actual circuits as follows.

TABLE I
CURRENT IN EACH MOSFET.

M_1 :	I_{D1}	M_4 :	$I_{D2}+I_{D1}$
M_2 :	$I_{D2}-I_{D1}$	M_5 :	I_{REF2}
M_3 :	I_{D2}	M_6 :	I_{OUT}

III. CIRCUIT IMPLEMENTATION

We designed the sensor with the architecture given in Fig. 1, assuming a standard CMOS process. The details of each circuit block is as follows.

A. Bias circuit and PTAT current generator

To implement Eq. (7) with a simple circuit, we rewrite the equation as

$$\frac{I_{D2}I_{D1}}{(I_{D2}-I_{D1})(I_{D2}+I_{D1})} = \frac{\eta k_B}{2e(V_{G2}-V_{G1})}\,T. \quad (8)$$

The PTAT current generator can be constructed by using this relation.

Figure 2 shows the bias circuit and the PTAT current generator. A temperature-independent reference current I_{REF1} is applied to a resistor R to generate two voltages V_{G1} and V_{G2} (for the reference current circuit, see [7]). Two MOSFETs M_{B1} and M_{B2} in the PTAT current generator accept voltages V_{G1} and V_{G2} and produce two subthreshold currents I_{D1} and I_{D2}. Transistors M_1 - M_6 accept I_{D1} and I_{D2} through current mirrors and accept $I_{D2}+I_{D1}$ and $I_{D2}-I_{D1}$ through a current adder and a current subtractor. The gate-source voltages (V_1 through V_6) for the six MOSFETs (M_1 through M_6) form a closed loop, so we find that

$$V_1 - V_2 + V_3 - V_4 + V_5 - V_6 = 0. \quad (9)$$

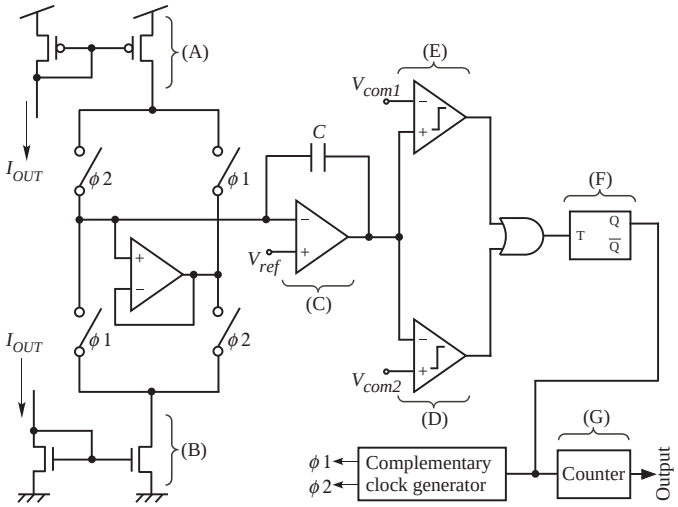

Fig. 3. Block diagram of a charge balancing A/D converter.

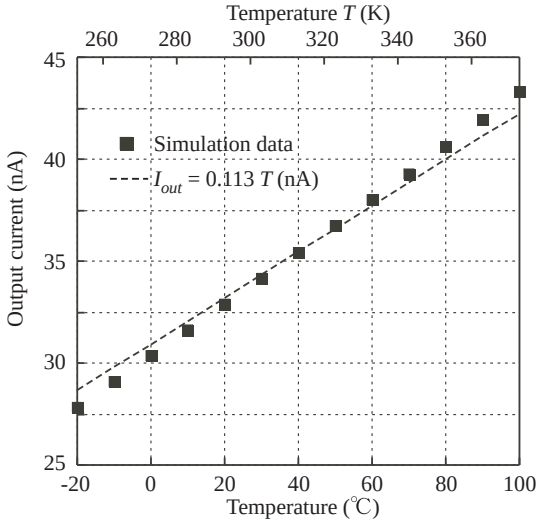

Fig. 4. Simulation results of the PTAT current generator.

Table I shows the current in each MOSFET (M_1 - M_6). From the translinear principle [8], [9], we can obtain

$$I_{D1}I_{D2}I_{REF2} = (I_{D2} - I_{D1})(I_{D2} + I_{D1})I_{OUT}, \qquad (10)$$

where I_{REF2} is a constant current independent of temperature. Therefore, output current I_{OUT} can be expressed by

$$I_{OUT} = I_{REF2}\,\frac{I_{D2}I_{D1}}{(I_{D2} - I_{D1})(I_{D2} + I_{D1})}. \qquad (11)$$

Using Eq. (8), we can rewrite Eq. (11) as

$$I_{OUT} = I_{REF2}\,\frac{\eta k_B}{2e(V_{G2} - V_{G1})}\,T. \qquad (12)$$

Voltage difference $V_{G2} - V_{G1}$ is equal to RI_{REF1}. Therefore, if reference current I_{REF2} is set equal to I_{REF1}, output current I_{OUT} can be expressed by

$$I_{OUT} = \frac{\eta k_B}{2eR}\,T. \qquad (13)$$

Consequently, we can obtain a PTAT current. Voltage difference $V_{G2} - V_{G1}$ must be 10 mV or less to produce an accurate PTAT current .

B. A/D converter

The A/D converter we used is shown in Fig. 3. It is based on the charge balancing A/D converter [10] and consists of a CCO (an integrator (C), two comparators (D, E), and a T-type flip-flop (F)) and a counter (G)). It is operated with complementary clocks $\phi 1$ and $\phi 2$ that are produced by a complementary clock generator controlled by the output of the A/D converter. The CCO produces the oscillation pulses whose frequency is proportional to PTAT current I_{OUT}, therefore proportional to absolute temperature. When the complementary clock generator produces clocks $\phi 1$ =0 and $\phi 2$ =1, PTAT current I_{OUT} is applied to the integrator through the pMOSFET current mirror (A), and the output voltage of the integrator decreases with time and falls below reference voltage V_{com2} for the comparator (D). Then the output of the comparator turns from 0 to 1, and this turns the output of the flip-flop from 0 to 1. The complementary clock generator accepts this 1 input and turns the clocks to $\phi 1$ =1 and $\phi 2$ =0. Then, I_{OUT} is applied to the integrator through the nMOSFET current mirror circuit (B) and the output voltage of the integrator increases with time to exceeds the reference voltage V_{com1} ($> V_{com2}$) of the comparator (E). The output of the comparator turns from 0 to 1 (the output of the comparator have returned to 0), and this turns the output of the flip-flop from 1 to 0. The complementary clock generator accepts this 0 input and turns the clocks to $\phi 1$ =0 and $\phi 2$ =1. By repeating these operations,

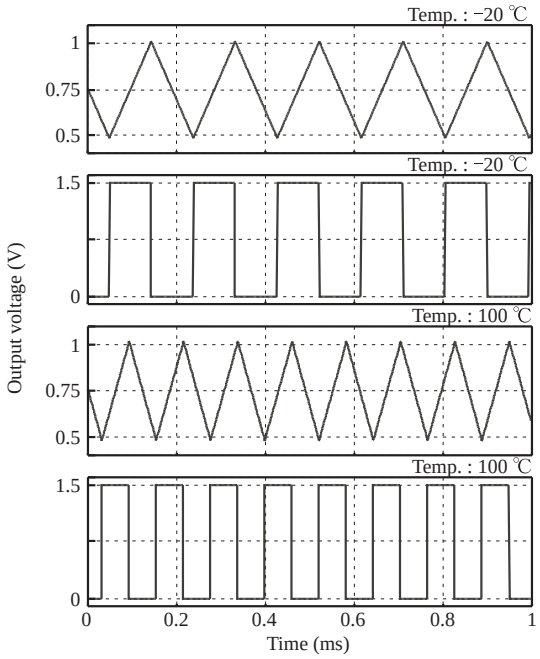

Fig. 5. Simulated output waveforms of the integrator and the counter at different temperature.

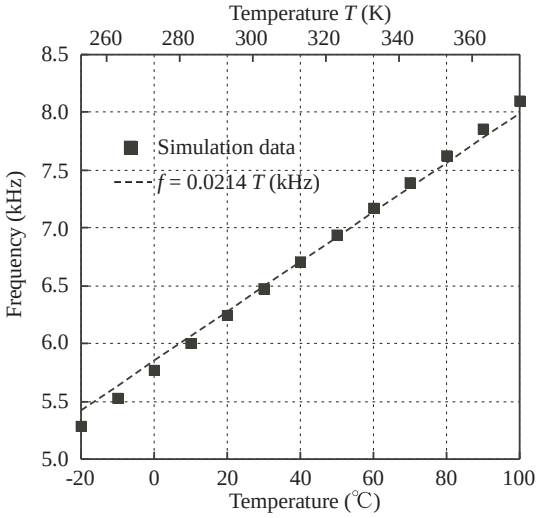

Fig. 6. Simulation results of the CCO output frequency

the CCO produces oscillation pulses that are proportional to current I_{OUT}.

The velocity of increase in the output voltage V_{int} of the integrator is given by

$$\left|\frac{dV_{int}}{dt}\right| = \frac{I_{OUT}}{C.} \tag{14}$$

Therefore, the period t_0 of oscillation is given by

$$V_{com1} - V_{com2} = \frac{I_{OUT} \cdot t_0}{2C}. \tag{15}$$

Frequency f of the output pulses can be given by

$$f = \frac{I_{OUT}}{2C(V_{com1} - V_{com2}).} \tag{16}$$

Thus, the frequency of the oscillation pulses is proportional to absolute temperature. The output pulses are applied to the digital counter to produce the AD-converted digital output.

IV. Simulation results

We confirmed the operation of the sensor by SPICE simulation, assuming a set of 0.35-μm 2P4M standard CMOS parameters and a 1.5-V power supply.

Figure 4 shows output current I_{OUT} of the PTAT current generator as a function of temperature from –20 to 100 ℃. In simulation, reference currents I_{REF1} and I_{REF2} were set to 100 nA, and resistance R was set to 100 kΩ; therefore, voltage difference V_{G2} – V_{G1} was 10 mV. The output current I_{OUT} was approximately given by

$$I_{out} = 0.113\,T \;\; (nA), \tag{17}$$

where T is absolute temperature.

Figure 5 shows the output waveforms of the integrator and the counter for two different temperatures, –20 and 100 ℃.

Figure 6 shows the oscillation frequency of the output pulses of the CCO as a function of temperature. The frequency f of the pulses was approximately given by

$$f = 0.0214\,T \;\; (kHz). \tag{18}$$

TABLE II
Performance summary

Process	0.35-μm, 2-poly, 4-metal CMOS
Supply voltage (V_{DD})	1.5 V
Temperature range	–20 - 100 ℃
Power	5.8 μW (T=100 ℃)

Table II summarizes the expected performance of the circuit. Simulation showed that the maximum power consumption was 5.8 μW at 100 ℃. A small-sized button battery (1.5 V and 35 mAh) ensures that our temperature sensor works for 1.2-year.

V. Conclusion

We developed an ultra-low power smart temperature sensor making use of subthreshold characteristics of MOSFETs. The circuit operation was confirmed by simulation with 0.35-μm standard CMOS parameters. The power consumption of the sensor was only 5.8 μW at 100 ℃. The sensor is expected to work for a year even with a small-sized button battery.

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