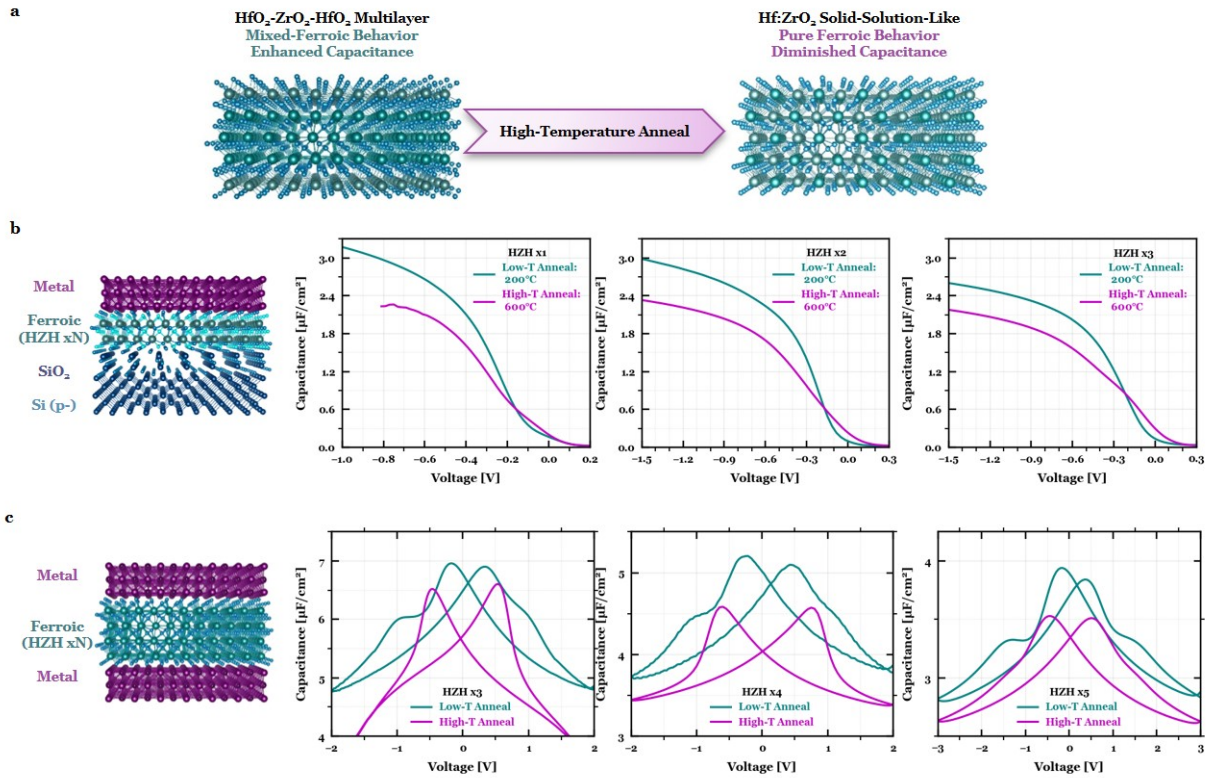
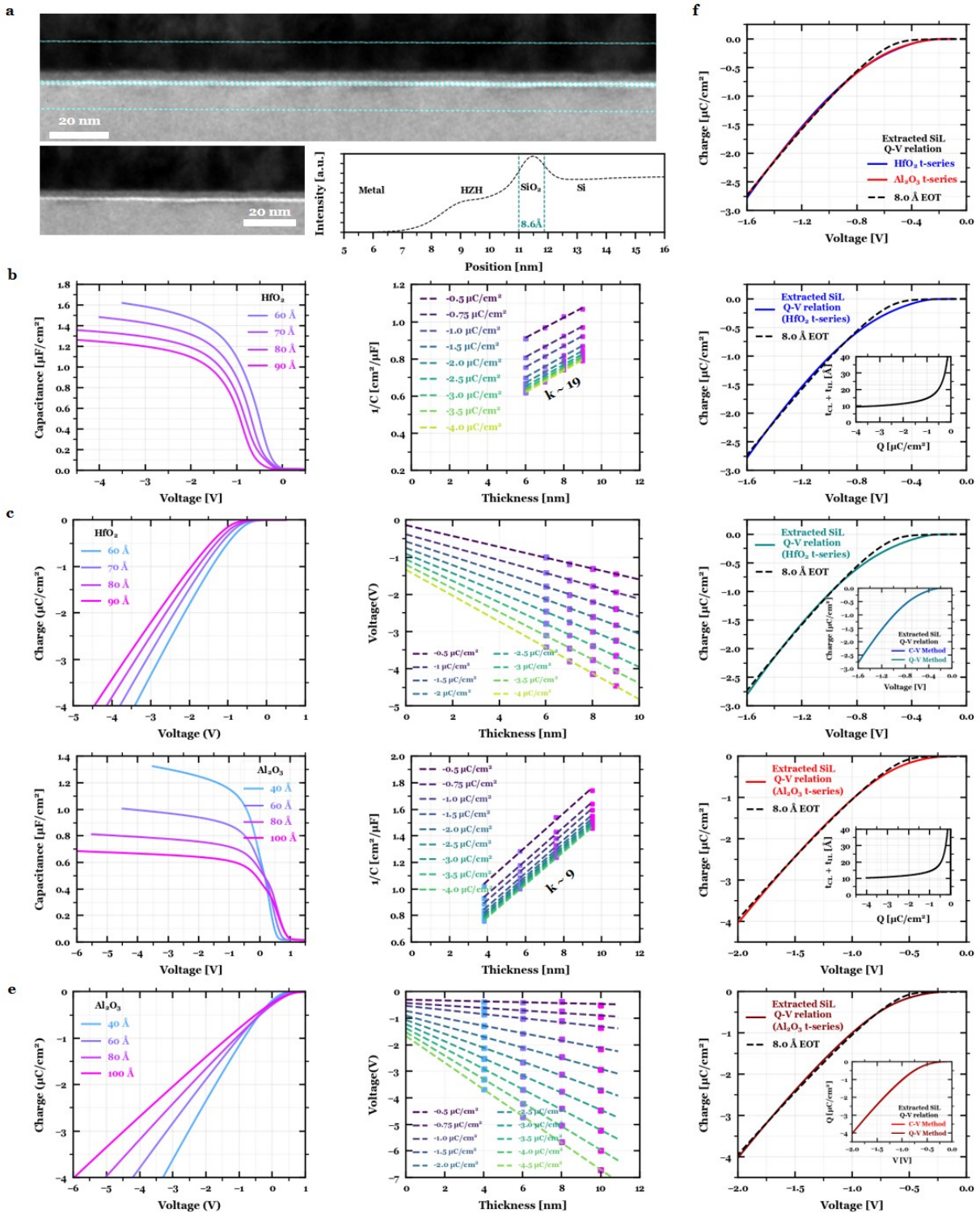
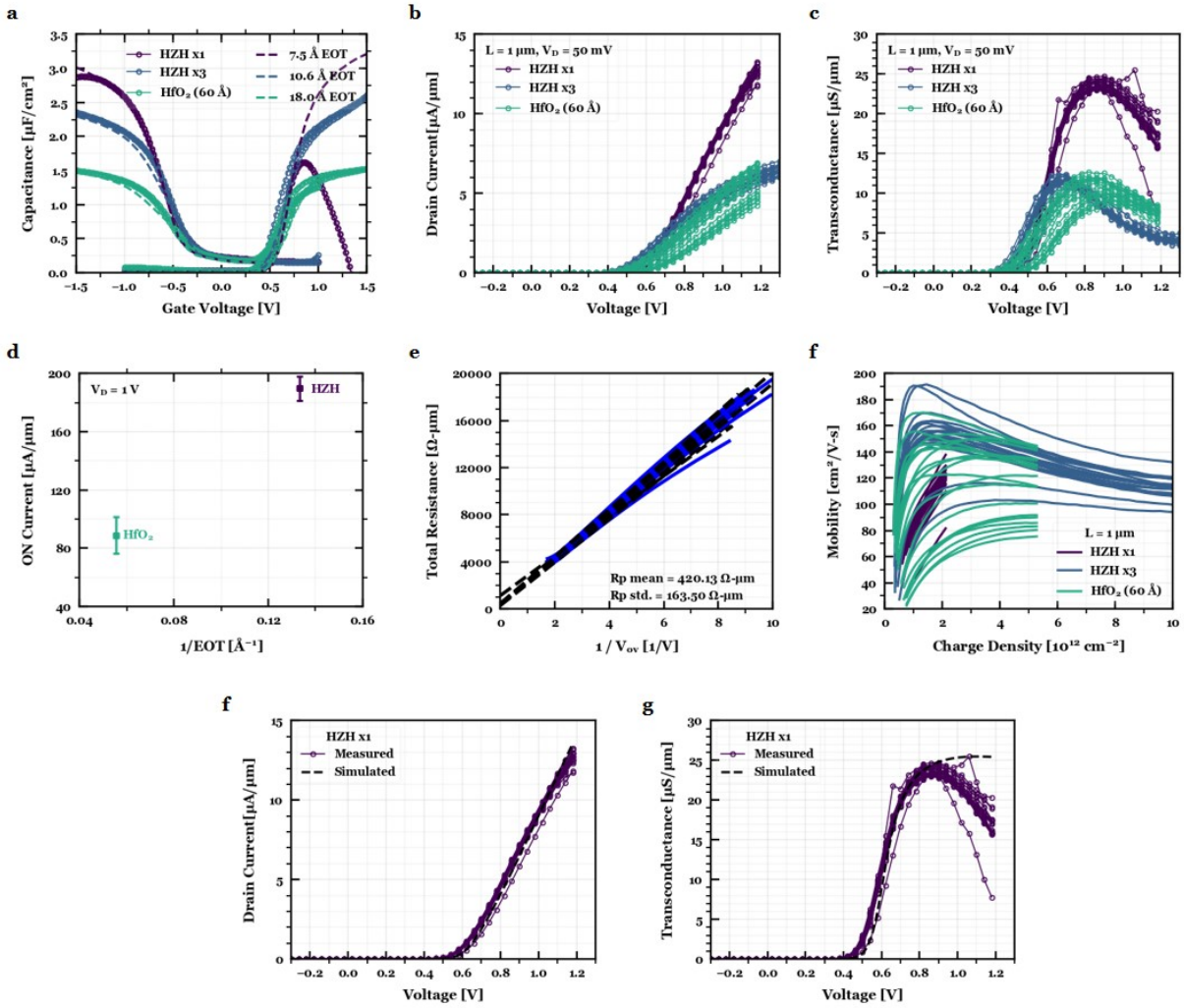


Extended Data Fig. 5. Solid solutions versus superlattice structure: Role of annealing temperature. **(a)** Schematic of HfO_2-ZrO_2 multilayer and Hf:ZrO_2 solid solution films. Under a high-temperature anneal, the multilayer structure transitions towards a Hf:ZrO_2 solid-solution-like structure demonstrating more FE-like behavior. The solid solution state yields diminished capacitance due to the lack of both the higher-permittivity AFE phase and the mixed-ferroic-induced capacitance enhancement (Fig. 1a). **(b)** Comparison of MOS capacitor accumulation *C-V* characteristics in HfO_2-ZrO_2 multilayers, where the superstructure was repeated (left) 1, (center) 2, or (right) 3 times, under both low- and high-temperature anneals. **(c)** Comparison of mixed-ferroic behavior in low-temperature treated MIM HfO_2-ZrO_2 multilayers versus FE behavior in in the same multilayers annealed at high temperatures, where the superstructure was repeated (left) 3, (center) 4, or (right) 5 times. In all instances, the high-temperature anneal (> 500°C) results in diminished accumulation capacitance compared to the low-temperature anneals, as the multilayered mixed-ferroic films presumably transition to more FE-like solid-solution alloys.


a
20 nm
20 nm
Intensity [a.u.]
Metal
HZH
SiO2
Si
8.6Å
Position [nm]
f
Charge [μC/cm²]
Voltage [V]
Extracted SiL
Q-V relation
HfO2 t-series
Al2O3 t-series
8.0 Å EOT
b
Capacitance [μF/cm²]
HfO2
60 Å
70 Å
80 Å
90 Å
Voltage [V]
1/C [cm²/μF]
-0.5 μC/cm²
-0.75 μC/cm²
-1.0 μC/cm²
-1.5 μC/cm²
-2.0 μC/cm²
-2.5 μC/cm²
-3.0 μC/cm²
-3.5 μC/cm²
-4.0 μC/cm²
k ~ 19
Thickness [nm]
Extracted SiL
Q-V relation
(HfO2 t-series)
8.0 Å EOT
tCL + tIL [Å]
Q [μC/cm²]
c
Charge (μC/cm²)
Voltage (V)
Voltage(V)
-0.5 μC/cm²
-1 μC/cm²
-1.5 μC/cm²
-2 μC/cm²
-2.5 μC/cm²
-3 μC/cm²
-3.5 μC/cm²
-4 μC/cm²
Thickness [nm]
Extracted SiL
Q-V relation
(HfO2 t-series)
8.0 Å EOT
C-V Method
Q-V Method
Al2O3
40 Å
60 Å
80 Å
100 Å
k ~ 9
Extracted SiL
Q-V relation
(Al2O3 t-series)
8.0 Å EOT
e
Extracted SiL
Q-V relation
(Al2O3 t-series)
8.0 Å EOT
V [V]

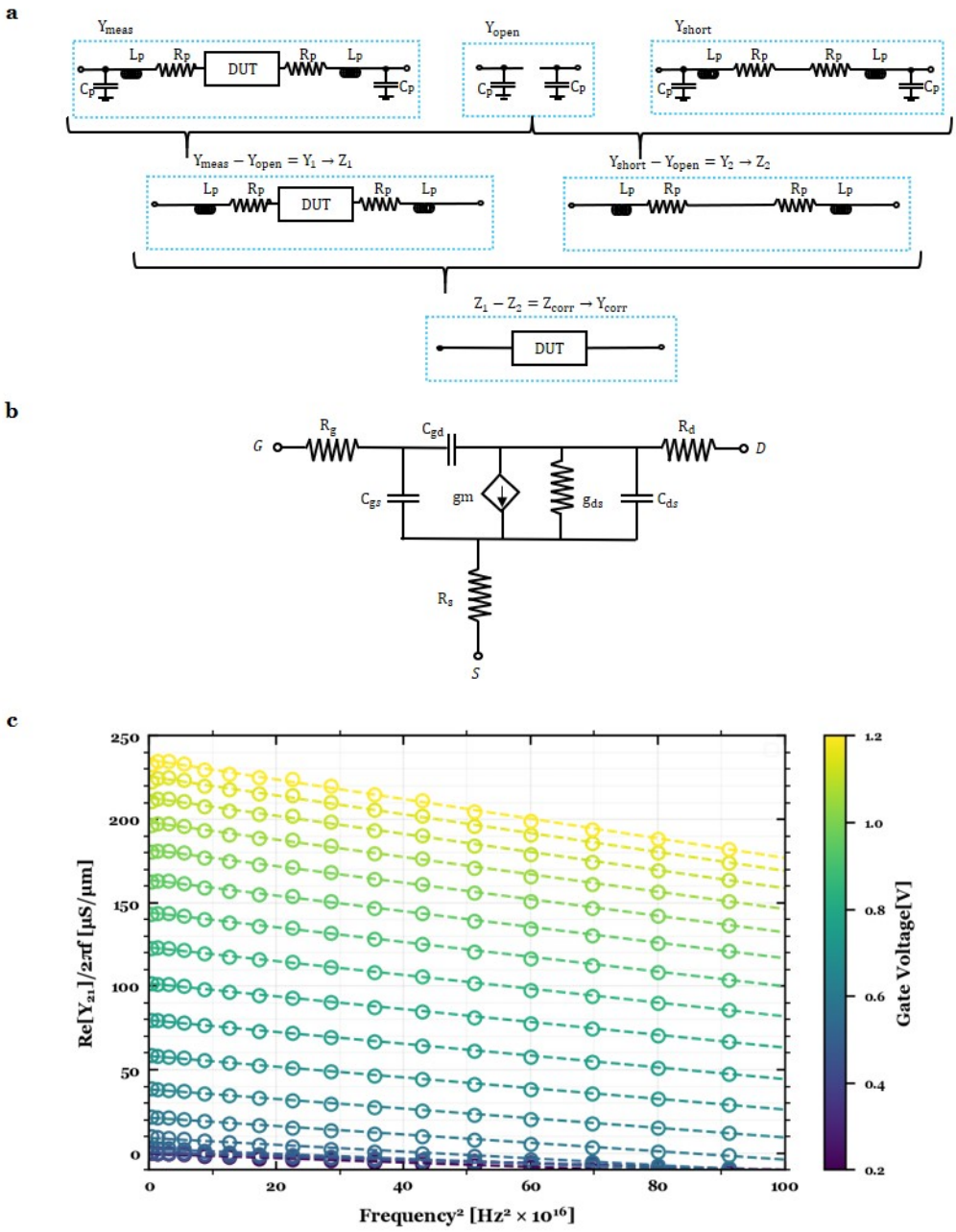
1089

Extended Data Fig. 6. SiO_2 interlayer thickness. **(a)** Wide field-of-view cross-sectional TEM images of the HfO_2-ZrO_2 multilayer structure and its corresponding intensity line scan (bottom right) averaged across the entire field-of-view (FoV) of the top cross-sectional image ($\sim$ 150 nm), specified by the teal-colored box. Note the vertical teal-colored lines in the intensity line scan correspond to the inner teal-colored box in the wide-FoV image, which delineate the SiO_2 interlayer boundaries. The bottom cross-sectional TEM image is provided to highlight the thin SiO_2 interlayer (white region) without obfuscation by the teal-colored box. A physical SiO_2 thickness of 8.6 Å is extracted from analysis of the averaged intensity line scan of the wide FoV TEM (Methods). **(b), (d)** *C-V* measurements of HfO_2 (b) and Al_2O_3 (d) thickness series in MOS capacitor structures (left), extracted inverse capacitance versus thickness at various values of charge (center), and extracted *Q-V* relation Si charge layer and SiO_2 interlayer (SiL) (right), which fits to TCAD simulations for 8.0 Å SiO_2. The SiL *Q-V* relation was found by integrating the extracted capacitance equivalent thickness of SiL versus charge (right, inset). This electrical interlayer thickness (8.0 Å) is slightly less the physical thickness determined by TEM (8.6 Å). As a sanity check, the extracted permittivity from this methodology for HfO_2 and Al_2O_3 corresponds to 18 and 9, respectively, as is expected (Methods, Permittivity Extraction). **(c), (e)** *Q-V* curves of HfO_2 (c) and Al_2O_3 (e) thickness series obtained from integrating MOS *C-V* measurements (left), extracted voltage vs thickness at various values of charge (center), and extracted *Q-V* relation of SiL (right). The SiL *Q-V* relation is consistent with the *Q-V* relation extracted from the *C-V* data (inset). **(f)** Consistency in the SiL *Q-V* relation extracted from the *C-V* data from both the HfO_2 and Al_2O_3 thickness series, which both fit to an SiO_2 interlayer thickness of 8.0 Å.



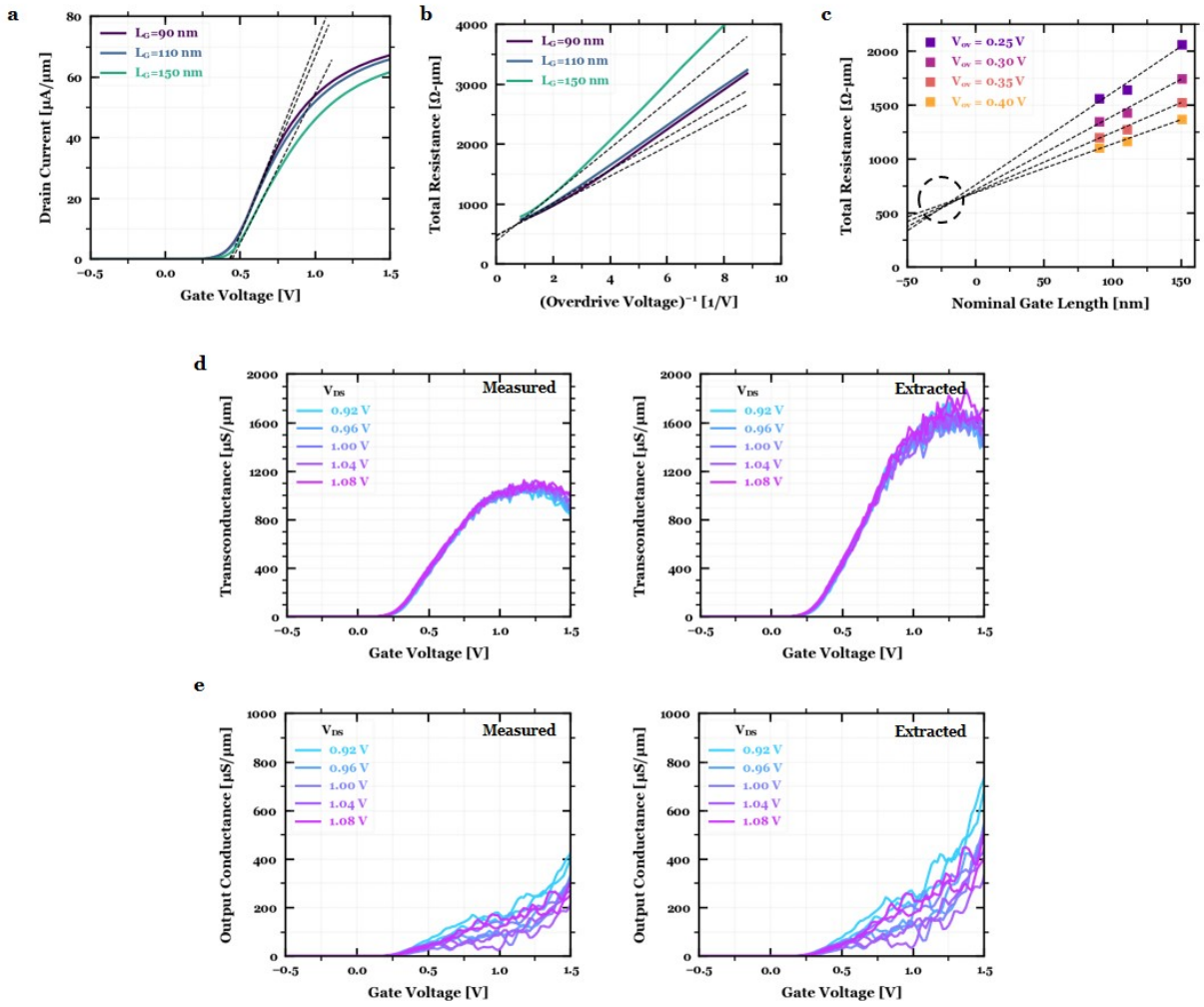
Extended Data Fig. 7. Mobility extraction. **(a)** Split *C-V* curves obtained for multilayer HfO_2-ZrO_2 gate stacks (repeated 1 and 3 times i.e. HZHx1 and HZHx3) and 60 Å HfO_2 dielectric control (Hf-60) from L_G = 50 μm bulk transistors at 10 kHz. These *C-V* curves were fit to EOT simulations of 7.5 Å, 10.6 Å, and 18 Å for HZHx1, HZHx3, and Hf-60, respectively. From the off-state accumulation *C-V*, a doping level of $N_a = 2 \times 10^{17}$ cm^{-3} was extracted and from the slope of the inversion *C-V*, the interface trap density was found to be $D_{it} = 3 \times 10^{12}$ eV^{-1} cm^{-2}. **(b, c)** I_D-V_G (b) and g_m-V_G (c) transfer characteristics for L_G = 1μm bulk transistors at V_{DS} = 50 mV for multiple devices per sample. **(d)** ON current-capacitance (plotted as I_{ON}-1/EOT) comparison

of the HZH multilayer gate stack versus the HfO_2 dielectric control for L_G = 0.5 μm devices. Here, the ON-current is defined as I_D at V_D = 1 V with an overdrive voltage V_{ov} = 0.5 V. The error bars represent 1 standard deviation of the ON-current measured from 20 different devices. As expected, the ON current increases as the inverse-EOT (proportional to the gate capacitance) increases. **(e)** Series resistance extraction from $1/V_{ov}$ method for $V_{ov} = V_{gs} - V_t$ = 0.3 V to 0.5 V for L_G = 1 μm devices. The threshold voltage was extracted from the maximum g_m method. **(f)** Extracted mobility as a function of inversion sheet charge density. The effective mobility was taken to be the average maximum mobility across multiple L_G = 1 μm devices. **(g, h)** Transfer I_D-V_G (g) and g_m (h) data fit to a constant mobility model based on the extracted effectively mobility in (f). A summary of the EOT-mobility trend from the various samples is provided in Figure 3b.



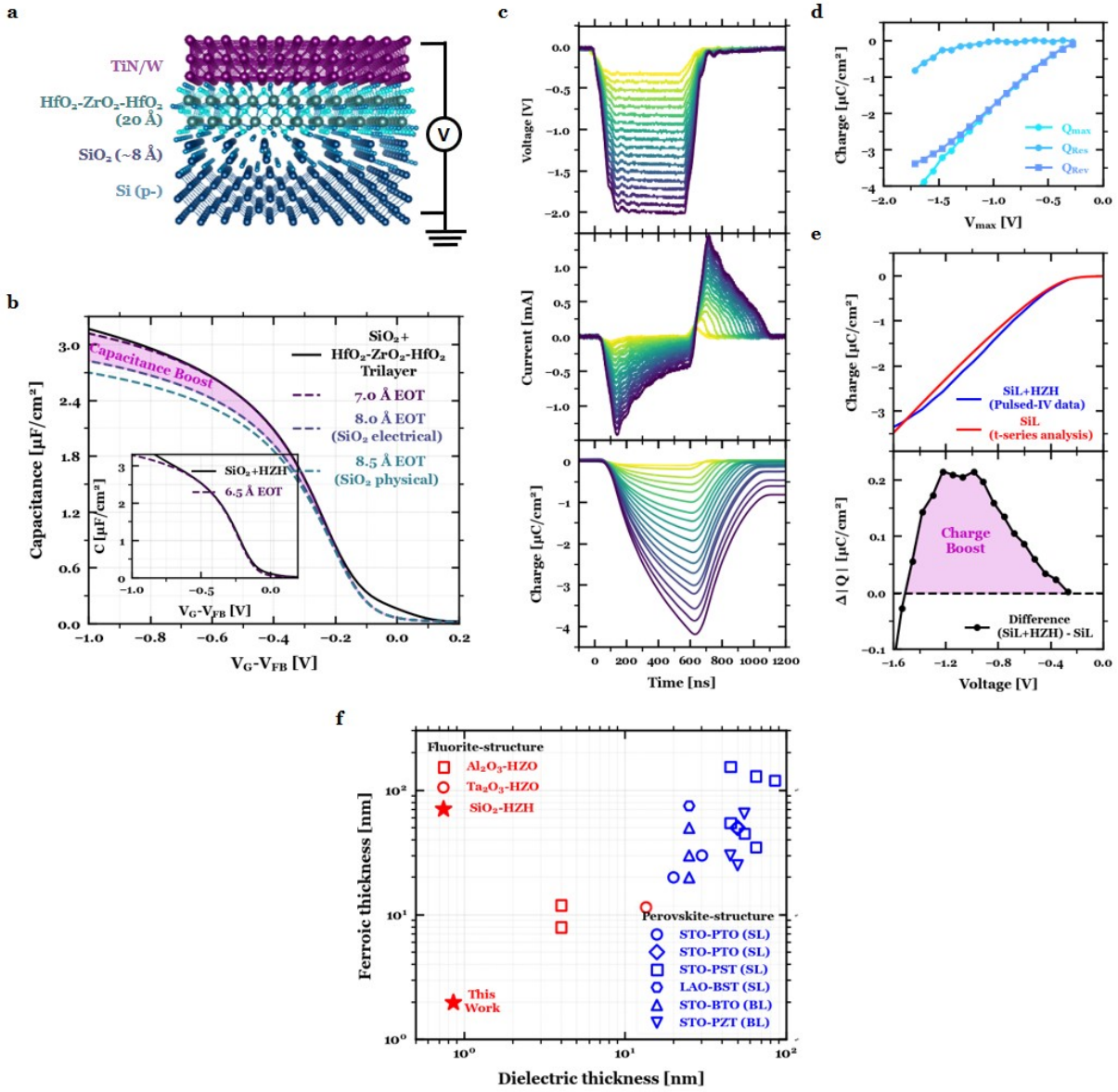
Extended Data Fig. 8. RF device characterization. **(a)** De-embedding procedure for extracting corrected admittance parameters (Y_{corr}) by decoupling parasitic shunt capacitance and series resistance and inductance by measuring scattering parameters for the device under test (DUT) as well as open and short structures. More details can be found in the Methods. **(b)** Small-signal model for

transistor used to extract transconductance (g_m) and total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$)). **(c)** De-embedded $\frac{Re[Y_{21}]}{2\pi f}$ (open circles) as a function of squared frequency at different DC V_{GS} bias points extrapolated to the zero frequency limit (dotted lines) to extract the RF g_m. All data shown was extracted from bulk transistors (L_G = 1 μm) integrating the 2 nm HfO_2-ZrO_2-HfO_2 ferroic gate stack.



Extended Data Fig. 9. Transconductance extraction. **(a)** Threshold voltage extraction by linear extrapolation for various channel lengths. All channel lengths give nearly constant V_T ($\sim$ 0.42 V), satisfying the assumption for the line resistance method. **(b)** Source/drain series resistance extracted using the $1/V_{ov}$ method (Methods). By performing a linear interpolation of the total resistance for V_{ov} = 0.5-0.6 V, the extracted series resistance is $\sim$ 500 Ω-μm. **(c)** Source/drain series resistance extracted using the line resistance method (Methods). The trend is considered down to L_G = 90 nm, which intersects at $\sim$ 500-600 Ω-μm – consistent with the $1/V_{ov}$ method– with an L_G offset of $\sim$ 50 nm. **(d), (e)** Measured (left) and extracted (right) transconductance (d)

and output conductance (e) versus V_G for V_{DS} = 0.9-1.1 V, assuming R_s = R_d = 250 Ω-μm for L_G = 90 nm. The de-embedding of intrinsic g_m and g_{ds} from extrinsic G_m and G_{ds} is described in the Methods. All data shown was measured on SOI short-channel transistors integrating the 2 nm HfO_2-ZrO_2-HfO_2 ferroic gate stack.



Extended Data Fig. 10. Capacitance and charge enhancement. **(a)** MOS schematic of the 20 Å HfO_2-ZrO_2-HfO_2 mixed ferroic trilayer sample on lightly-doped Si (10^{15} cm^{-3}) considered for the following accumulation *C-V* and pulsed *I-V* measurements. **(b)** Accumulation *C-V* curves for the 2 nm HfO_2-ZrO_2-HfO_2 trilayer grown on sub-nm SiO_2 fit to effective oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation *C-V* of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO_2 demonstrates

lower EOT than the thickness of SiO_2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. **(c)** The applied voltage pulse (top), the measured current response (center) and the integrated charge (bottom) as a function of time for 2 nm HfO_2-ZrO_2-HfO_2 trilayer in MOS capacitors. **(d)** The maximum charge Q_{max}, the residual charge Q_{res}, and their difference, Q_{rev}, derived from the charge vs time curve for each of the voltage pulses (Methods). **(e)** The reversible charge of the MOS layer (top) compared against the extracted charge of the Si charge layer plus SiO_2 interlayer (SiL) derived electrically (Extended Data Fig. 5f). The charge boost (bottom) present in the total MOS structure (SiL plus HZH capacitors) compared to just the SiL is a signature of negative capacitance, as previously demonstrated in metal-ferroelectric-insulator-metal (MFIM) structures[47,67]. **(f)** Scatter plot of reported ferroelectric-dielectric systems demonstrating negative capacitance at the capacitor level via capacitance (*C-V* measurements) or charge (pulsed *I-V* measurements) enhancement. The plot considers fluorite-structure bilayers[47,67] (red), perovskite-structure bilayers[22,91] (blue, BL), and perovskite-structure superlattices[38–41] (blue, SL). This work employing sub-nm SiO_2 interlayer and 2 nm HfO_2-ZrO_2 multilayer on silicon (black, star) provides the most scaled demonstration of negative capacitance, as supported by enhanced capacitance from *C-V* measurements (b) and amplified charge from pulsed *I-V* measurements (e) relative to the SiO_2 dielectric interlayer.

Figures

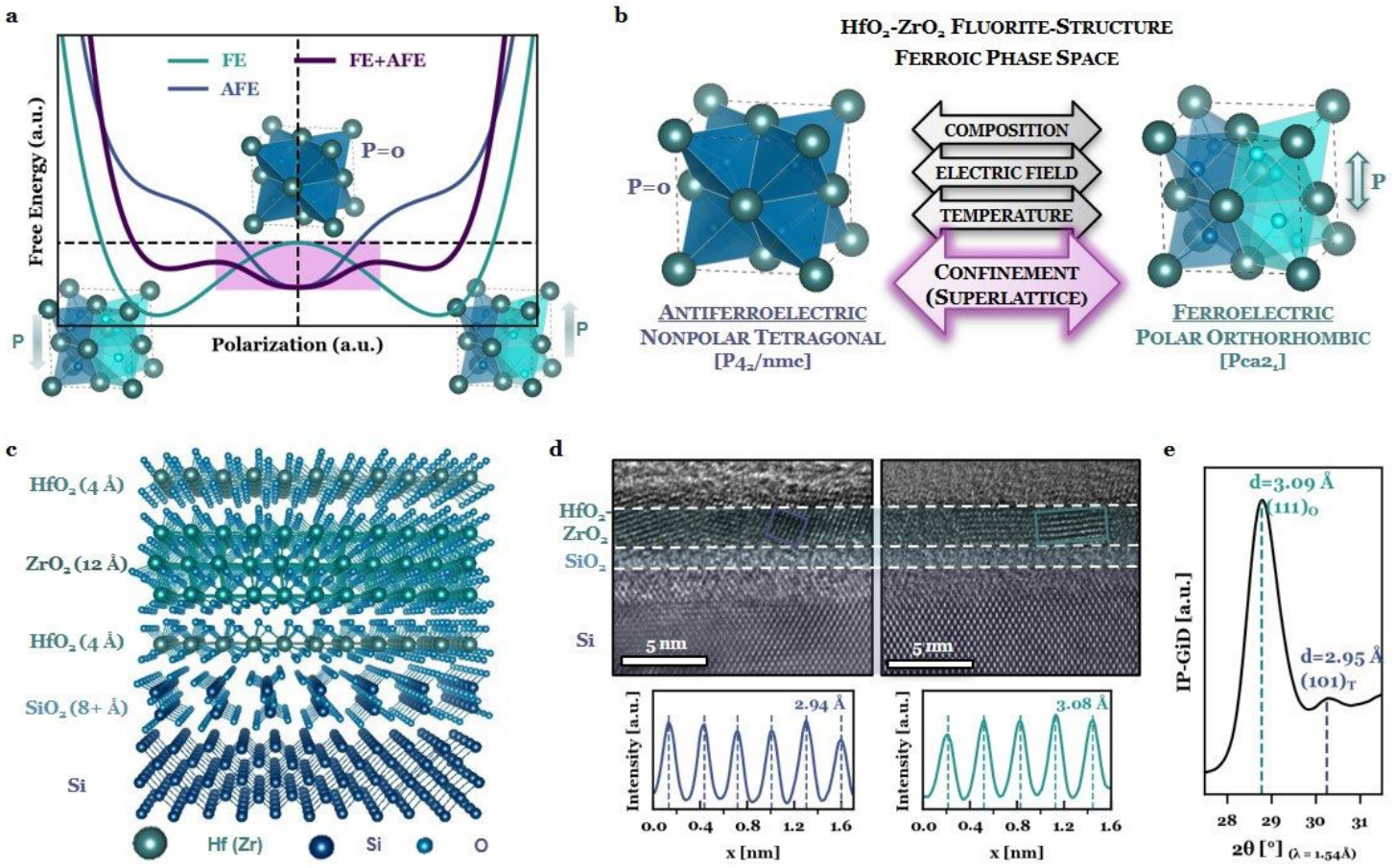


Figure 1

Atomic-scale design of negative capacitance in ultrathin HfO2-ZrO2. (a) Phenomeno logical model of negative capacitance (NC) in a mixed ferroic system. Landau free energy land scapes for a FE, AFE, and mixed FE-AFE system (Methods). Mixed FE-AFE phase competition should suppress polarization48 and enhance electric susceptibility22,40 via proximity to a phase4 boundary, and flattens the energy landscape, desirable traits for NC stabilization. The stable energy minimum of the composite free energy landscape, corresponding to the negative curvature (NC) regime of the ferroelectric energy landscape, is highlighted. (b) Engineering ferroic phase competition in the HfO2-ZrO2 fluorite-structure system. Beyond the conventionally-studied tuning parameters – composition, electric field, temperature23,35 – here we introduce dimensional confine ment via superlattice layering to tailor ferroic phase competition at the atomic-scale. (c) Schematic of the HfO2-ZrO2 fluorite-structure multilayer on Si; the heterostructures maintain distinct layers (i.e. not solid solution alloys) based on EELS, XRR, and depth-resolved XPS (Extended Data Fig. 1). The role of the layering on the underlying ferroic order and capacitance is studied by electrical measurements as a function of HfO2-ZrO2 stacking structure and annealing temperature (Extended Data Fig. 4 and 5, respectively). (d) HR-TEMimage of the atomic-scale HfO2-ZrO2-HfO2 trilayer (top) and extracted d-lattice spacings (bottom) corresponding to the fluorite-structure AFE

tetrago nal (P42/nmc, red) and FE orthorhombic (Pca21, blue) phases, respectively. The layer delineations are approximate, as the HfO2-ZrO2 and SiO2 interlayer thicknesses are more rigorously deter mined by XRR and TEM analysis (Extended Data Fig. 1 and 6, respectively). Note imaging the crystallinity of the HfO2-ZrO2 layers requires mistilt with respect to the Si lattice (Methods). (e) Synchrotron IP-GiD demonstrating the presence of both the AFE T-phase (101)t and FE O-phase (111)o reflections whose d-lattice spacings are consistent with those extracted from TEM. Detailed indexing to higher-order reflections for structural identification of the ferroic phases is provided by wide-angle synchrotron diffraction (Extended Data Fig. 2a). Further evidence of inversion symmetry breaking is provided by second harmonic generation and synchrotron linear dichroism (Extended Data Fig. 2c,d). Additionally, the evolution between these two ferroic phases are also studied as a function of temperature (Extended Data Fig. 3).

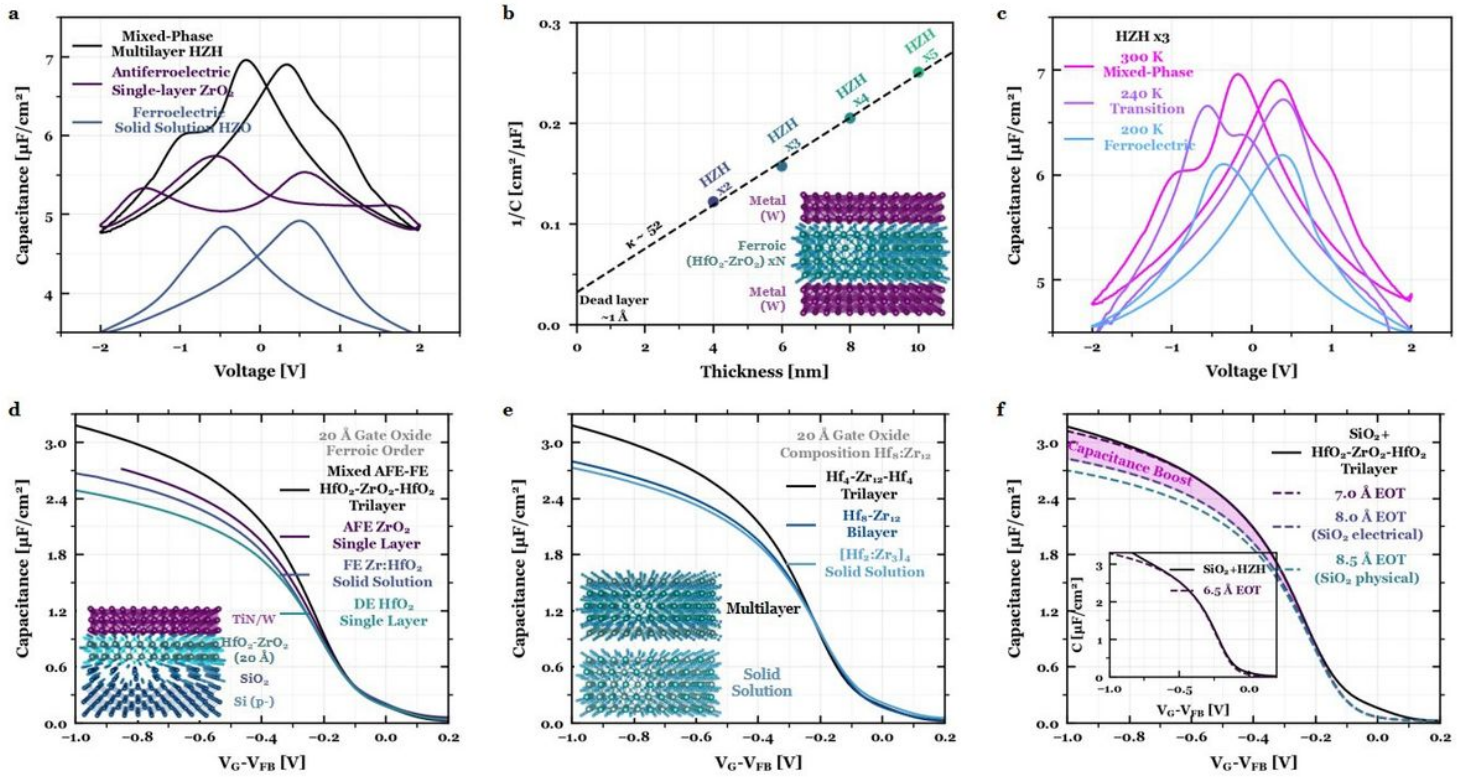


Figure 2

Enhanced capacitance in ultrathin HfO2-ZrO2 mixed-ferroic heterostructures. (a) MIM C-V hysteresis loops for a mixed FE-AFE HfO2-ZrO2 multilayer demonstrating higher ca pacitance compared against its AFE (ZrO2) and FE (Zr:HfO2) counterparts of the same thickness. (b) Inverse capacitance versus thickness of the MIM HfO2-ZrO2 multilayers up to 5 superlattice repeats (10 nm), with an extracted permittivity of 52 (Methods), extremely large for HfO2-based oxides. (c) MIM C-V hysteresis loops for HfO2-ZrO2 multilayers of the same periodicity demon strating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature. The proximity to the temperature-dependent phase transition (Extended Data Fig. 3) suggests the HfO2-ZrO2 heterostructures lies near its maximum electric susceptibility position, ideal for negative capacitance stabilization40,48. (d) MOS accumulation

C-V of HfO2-ZrO2-HfO2 trilayer compared to AFE ZrO2, FE Zr:HfO2, and DE HfO2, all of the same thickness (20 Å), indicating mixed-ferroic behavior is optimal for enhancing capacitance rather than purely FE or AFE behavior. (e) Accumulation C-V of the HfO2-ZrO2-HfO2 trilayer compared to bilayer and solid solutions films of the same thickness (ALD cycles) and composition (Hf:Zr cycles). Inset: Schematic of multilayer (Hf and Zr cations vertically separated) versus solid solution (Hf and Zr cations inter-mixed). These results suggest the capacitance enhancement in multilayer films is not simply driven by Hf:Zr composition23,35, but instead the atomic-scale stacking (Extended Data Fig. 4, 5). (f) Accumulation C-V curves for a 2 nm HfO2-ZrO2-HfO2 trilayer grown on sub-nm SiO2 fit to effective oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation C V of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO2 demonstrates lower EOT than the thickness of SiO2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. Furthermore, these 2 nm ferroic gate stacks demonstrate amplified charge from pulsed I-V measurements relative to the SiO2 interlayer (Extended Data Fig. 10). Notably, this 2 nm HfO2-ZrO2 multilayer on sub-nm SiO2 provides the most scaled demonstration of charge and capacitance enhancement at the capacitor-level (Extended Data Fig. 10).

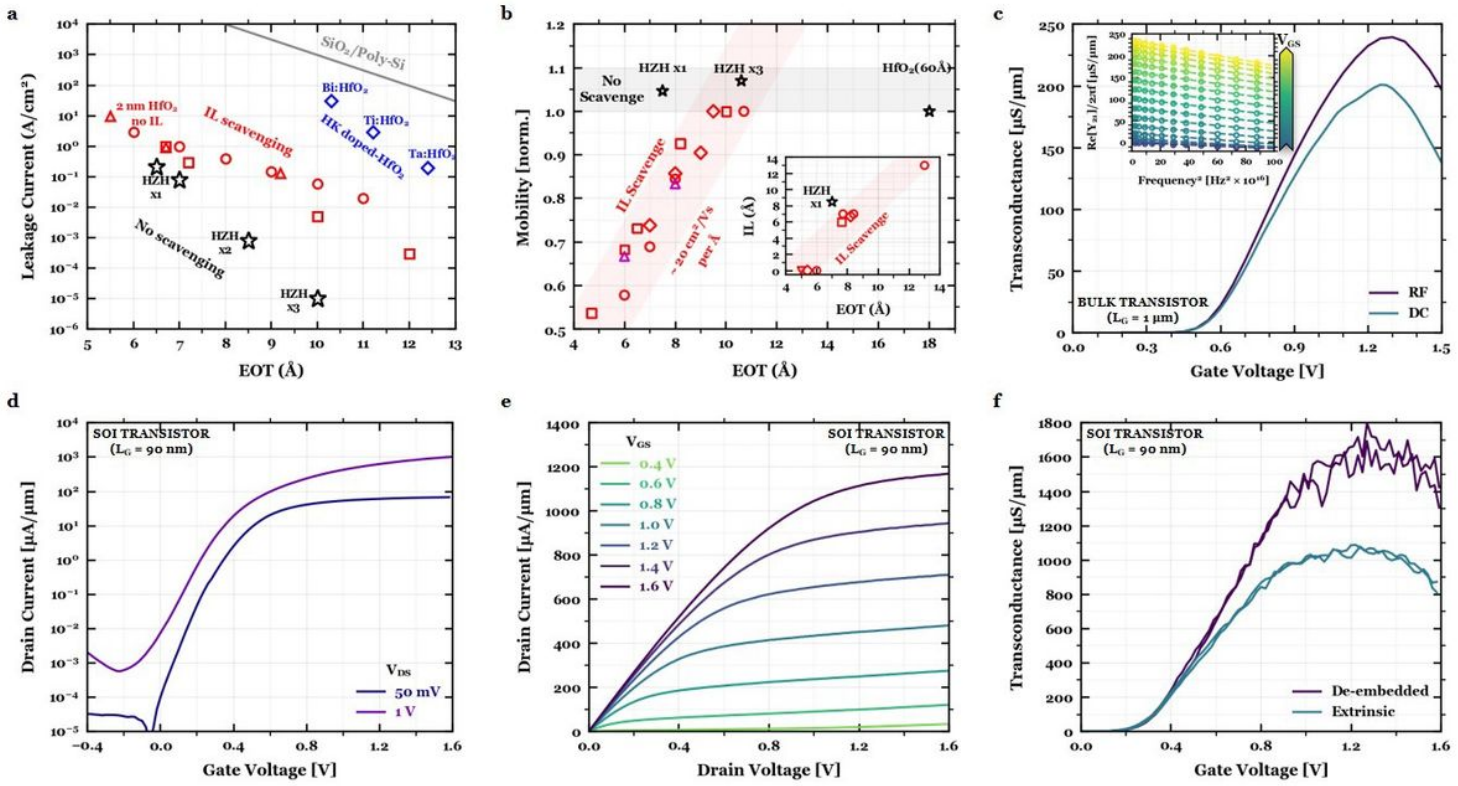


Figure 3

Device performance benefits utilizing ultrathin mixed-ferroic HfO2-ZrO2 gate stacks. (a) Leakage-effective oxide thickness (JG-EOT) scaling of the multilayer gate stacks (black) bench marked against reported HKMG literature3, including interlayer-scavenged 2 nm HfO2 (red), high-doped HfO2 (blue), and SiO2/poly-Si (gray). The leakage is the lowest reported for a 6.5-7.0 Å EOTMOS capacitor on silicon3, due

to the EOT reduction without requiring interlayer SiO2 thickness reduction. (b) Normalized mobility versus EOT scaling of the multilayer gate stacks (black) benchmarked against reported HKMG literature3, including interlayer-scavenged 2 nm HfO2 (red) and hybrid silicate-scavenged interlayer (magenta). For EOT scaling in conventional HKMG systems, the SiO2 interlayer has to be reduced to lower EOT, which leads to degraded mobility3. In this case, enhanced capacitance in HfO2-ZrO2 multilayers achieves scaled EOT without having to thin the SiO2 interlayer; therefore, mobility is not degraded. Inset: SiO2 interlayer thickness versus EOT scaling comparing the 7.0 Å EOT HfO2-ZrO2-HfO2 trilayer against notable HKMG literature which employ interlayer scavenging to reduce EOT3. This scatter plot highlights the underlying reason for the enhanced leakage-EOT and mobility-EOT behavior in the ultrathin trilayer gate stacks: low EOT without reduced SiO2 interlayer thickness. (c) Transconductance (gm) versus gate voltage (VG) 450 for long-channel bulk transistors (LG = 1 m) obtained from both DC (derivative of ID-VG) and RF (Re[Y21]) measurements (Methods) at VDS = 1 V. Inset: De-embedded Re[Y21] (open circles) as a function of squared frequency at different DC VGS bias points extrapolated tothe zero frequency limit (dotted lines) to extract the RF gm (Extended Data Fig. 8). The high frequency measurements help suppress defect contributions which would otherwise dampen the intrinsic gm. (d, e, f) DC I-V transfer characteristics (ID-VG, d), DC output characteristics (ID-VD, e), and DC transconductance (gm-VG, f) for short-channel (LG = 90 nm) SOI transistors. Notably, the maximum on-current and gm at VDS = 1 V exceeds 1 mA/m and 1 mS/m. DC mobility and transconductance values are carefully extracted after de-embedding the series resistance from double-swept I-V measurements (Extended Data Fig. 7 and 9, respectively).