Unambiguous Extraction of Threshold Voltage Based on the Transconductance-to-Current Ratio

A. I. A. Cunha*, M. C. Schneider, C. Galup-Montoro, C. D. C. Caetano, and M. B. Machado

Department of Electrical Engineering, Federal University of Santa Catarina,
Florianópolis, SC, CEP 88040-900, Brazil,
*Department of Electrical Engineering, Federal University of Bahia
Escola Politécnica, Salvador, BA, CEP 40210-630, Brazil
E-mails: aiac@ufba.br, {marcio, carlos, cleber, marciobm}@eel.ufsc.br

ABSTRACT

This paper presents a very simple methodology for determining the threshold voltage. The procedure is based on the expressions of the Advanced Compact MOSFET (ACM) model, valid in all regimes of operation, which assures physical meaning, consistency and reliability for the results. The extraction of the threshold voltage is accomplished over a single measured drain current characteristic in the linear region, in order to avoid short channel effects. Experimental results for the extraction of threshold voltages in 0.35 and 0.18μm CMOS tecnhologies are shown.

Keywords: extraction, threshold voltage, transconductance to current ratio

1 INTRODUCTION

The threshold voltage V_T is a fundamental parameter in modeling and characterization of MOS transistors. Roughly speaking, this parameter represents the onset of conduction of the channel. V_T is important not only for both analysis and design of MOS integrated circuits but also for technology characterization. Therefore, the prominent effort that has been made to devise reliable practical methods for determination of the threshold voltage is fully justified.

At least, a dozen of methods to extract the threshold voltage are available [1]-[3]. As pointed out in [2], a method to extract V_T should (a) be valid for all technologies, (b) determine the gate voltage where the inversion layer starts to be created, and (c) be easily applicable. We endorse requirements (a) and (c) but rephrase (b) - "the threshold voltage extraction should be associated with a clear definition of V_T based on physics".

From references [1]-[3], it is clear that the extraction of the threshold voltage in a simple and consistent manner still remains an unsolved problem. In this work, we present a methodology for the extraction of the threshold voltage, based on the Advanced Compact MOSFET (ACM) model [4], [5]. Since the analytical expressions of the MOSFET characteristics in the ACM model are valid from weak to strong inversion, inconsistencies generated by regional models are by all means avoided. The procedure proposed for the extraction of V_T is performed over the weak and moderate inversion regions with small drain-source voltages so that short channel effects impose no drawbacks. Even series resistances of source and drain might be disregarded owing to the negligible voltage drops across them.

In the following Section, we revisit the expressions of the ACM model and interpret the threshold voltage accordingly. In the third Section, we present the procedure for the extraction of the threshold voltage. In the fourth Section, we exhibit the experimental results for the extraction of V_T obtained from our methodology and compare them with those extracted from methods considered to be acceptable [1], [2].

2 THE ACM MODEL

The ACM (Advanced Compact MOSFET) model consists of simple, accurate, and single equations that represent the device behavior in all regimes of operation, using well-known physical parameters [4], [5]. With such features, the ACM model is very appropriate for the simulation of circuits in CMOS technology. The methodology for extracting the threshold voltage presented here are based on the following set of expressions of the ACM model:

$$I_D = I_S\left(i_f - i_r\right) \tag{1}$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{2}$$

$$V_P - V_{S(D)B} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)\right] \tag{3}$$

$$V_P \cong \frac{V_{GB} - V_{T0}}{n} \qquad (4)$$

where I_D is the drain current, I_S is the specific current, $i_f(i_r)$ is the normalized forward (reverse) saturation current or inversion level, μ is the effective mobility, C'_{OX} is the oxide capacitance per unit area, ϕ_t is the thermal voltage, W is the effective channel width, L is the effective channel length, n is the slope factor (slightly dependent on gate voltage), V_{GB} is the gate-bulk voltage, V_{DB} is the drain-bulk voltage, V_{SB} is the source-bulk voltage, and V_P is the pinch-off voltage.

According to eq.(4) of the ACM model, the threshold voltage is the value of V_{GB} for which the pinch-off voltage equals zero. From eq.(3) this condition corresponds to an inversion level i_f equal to 3 for $V_{SB}=0$. Now, using the concept of threshold voltage as the gate voltage such that $i_f = 3$ under the condition $V_{SB} = 0$, we are going to show how to measure V_{T0} from the ACM model.

3 EXTRACTION OF THE THRESHOLD VOLTAGE

The gate transconductance $g_{mg} = \partial I_D / \partial V_G$ is an important small-signal parameter concerning the characterization methodology that we describe in this work. In the ACM model, g_{mg} is explicitly expressed in terms of the normalized saturation currents.

Differentiating (3) with respect to gate voltage, after taking into account (4), yields:

$$\frac{\partial i_{f(r)}}{\partial V_G} = \frac{2}{n\phi_t}\left(\sqrt{1+i_{f(r)}} - 1\right) \qquad (5)$$

Neglecting the dependence of I_S upon gate voltage the transconductance-to-current ratio becomes

$$\frac{g_{mg}}{I_D} \cong \frac{1}{i_f - i_r}\left(\frac{\partial i_f}{\partial V_G} - \frac{\partial i_r}{\partial V_G}\right) = \frac{2}{n\phi_t\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)} \qquad (6.a)$$

From (6.a), assuming the dependence of n on V_G to be negligible, the maximum value of g_{mg}/I_D occurs for the trivial condition $i_f = i_r = 0$, that is deep in weak inversion, and is equal to $1/(n\phi_t)$. Therefore, one can write

$$\frac{g_{mg}}{I_D} = \left(\frac{g_{mg}}{I_D}\right)_{max} \frac{2}{\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)} \qquad (6.b)$$

Eq. (6.b) is the basis of a very simple and quick method for determining V_{T0}, using a single current-voltage characteristic, as will be shown next. For a MOSFET biased at a fixed drain-to-source voltage, we will show that the transconductance-to-current ratio deviates from a maximum value in weak inversion by a factor that depends only on the inversion level. The slight variations of the slope factor and mobility with gate voltage over the measurement range are disregarded in this procedure.

The following steps should be accomplished for extracting V_{T0}:

(i) Connect the test device as shown in Fig.1. To reduce the short-channel effects, V_{DS} must be small ($2\phi_t$ or below). For simplicity, V_{SB} is taken equal to zero.

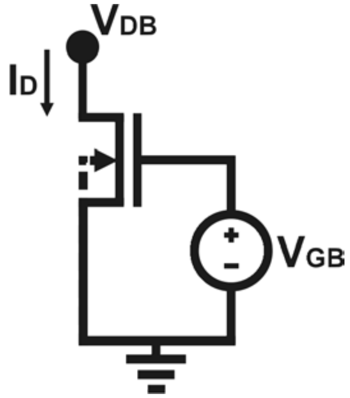

Fig.1: Circuit configuration for measuring the common-source characteristics

(ii) Measure the I_D vs V_{GB} characteristic.

(iii) Plot the g_{mg}/I_D vs V_{GB} characteristic (Fig.2).

(iv) Determine the maximum value of g_{mg}/I_D.

(v) For the V_{DS} you have chosen and $i_f = 3$, evaluate i_r numerically through

$$\sqrt{1+i_r} + \ln\left(\sqrt{1+i_r} - 1\right) = \sqrt{1+i_f} + \ln\left(\sqrt{1+i_f} - 1\right) - \frac{V_{DS}}{\phi_t} = 2 - \frac{V_{DS}}{\phi_t} \quad (7)$$

We have derived eq. (7) by writing eq. (3) for both i_f and i_r.

(vi) Using (6.b), calculate the ratio $(g_{mg}/I_D)/(g_{mg}/I_D)_{max}$ that corresponds to $i_f = 3$, and to the value of i_r determined in step (v). In our methodology, we have chosen $V_{DS} = \phi_t/2$ that, from (7), results in $i_r = 2.1196$ for $i_f = 3$. The introduction of these two values of i_f and i_r in (6.b) gives $g_{mg}/I_D = 0.5310(g_{mg}/I_D)_{max}$ (circle in Fig.2).

(vii) Since $V_{SB} = 0$, V_{T0} is the value of V_{GB} for which the condition $g_{mg}/I_D = 0.5310(g_{mg}/I_D)_{max}$ holds.

It should be noticed that, since the magnitude of drain current in moderate inversion is very small, the voltage drops through the parasitic resistances are negligible. Moreover, the extraction is accomplished for constant inversion level (i_f) and V_{SB} = 0, thus for constant V_P. Mobility degradation does not significantly affect the procedure because it is rather a function of V_P than of V_{GB} itself and because V_{GB} varies too little in the range of interest. The proposed methodology is independent of the slope factor n, therefore it is also valid for devices with non-negligible fast surface state concentration, which essentially affects n.

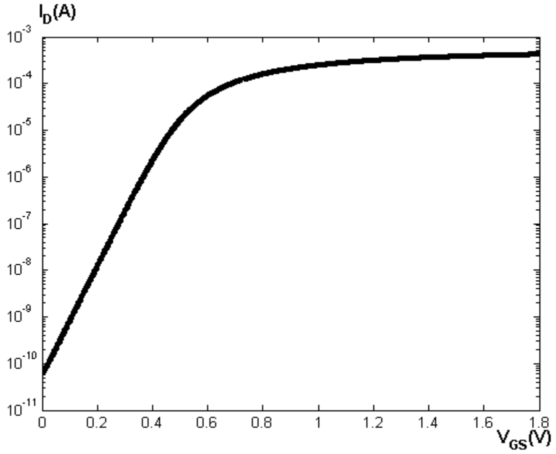

Fig.2. Drain current vs. gate voltage for V_{DB} = 13 mV ≅ $\phi_t/2$ and V_{SB}=0. L_m=0.2 μm (mask channel length), W_m = 20 μm (mask channel width). TSMC - 0.18 μm technology.

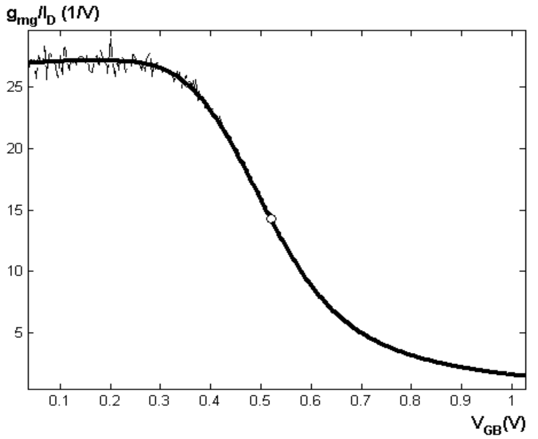

Fig.3. Transconductance-to-current ratio for V_{DB} = 13mV ≅ $\phi_t/2$ and V_{SB}=0. Dotted line: measured g_{mg}/I_D; solid line: filtered g_{mg}/I_D; circle: $g_{mg}/I_D=0.5310(g_{mg}/I_D)_{max}$. L_m= 0.2 μm (mask channel length), W_m = 20 μm (mask channel width). TSMC - 0.18 μm technology.

4 EXPERIMENTAL RESULTS

Measurements of the common-source characteristic in the linear region, with V_{SB} = 0 and V_{DS} = 13 mV have been accomplished for seven NMOS and seven PMOS transistors for 0.18 and 0.35 μm CMOS technologies. The mask channel lengths are 0.2, 0.3, 0.4, 0.5, 0.6, 0.8, and 2.0μm for 0.18μm technology and 0.4, 0.6, 0.8, 1.0, 1.2, 1.6, and 4.0μm for 0.35μm In order to reduce the relative noise level and mismatching, each transistor is composed of the parallel association of ten devices. The circuits have been fabricated by TSMC.

The Fig. 2 shows the dependence of the drain current on the gate voltage for a device whose channel length L=0.2μm in 0.18μm CMOS technology. Fig. 3 is the plot of the transconductance-to-current ratio vs. gate voltage of the device in Fig. 2. As mentioned before, the threshold voltage is the gate voltage for which the gm/Id equals 53% of its peak.

Table I exhibits the value of threshold voltage extracted for each test device through the proposed methodology, the extrapolation in the linear region (ELR) (1), and the second derivative logarithmic (SDL) method (1). One major drawback of the SDL method is the need for calculating the usually extremely noisy second order derivative of the current. On the other hand, the ELR method is not based on a physical definition of threshold voltage and suffers from the influence of series extrinsic resistances and mobility degradation effects, leading to an uncertainty in the maximum slope point determination.

Table 1: Experimental results from proposed methodology, ELR and SDL methods for extracting threshold voltage (0.35μm technology).

Mask channel length (μm)	V_{T0} (V) - NMOSFET			V_{T0} (V) - PMOSFET		
	ELR	SDL	Proposed method	ELR	SDL	Proposed method
0.4	0.567	0.559	0.590	-0.703	-0.679	-0.729
0.6	0.567	0.562	0.600	-0.713	-0.730	-0.745
0.8	0.561	0.542	0.584	-0.711	-0.694	-0.740
1.2	0.553	0.526	0.570	-0.709	-0.673	-0.720
1.6	0.546	0.524	0.564	-0.705	-0.670	-0.722
4.0	0.532	0.505	0.545	-0.692	-0.657	-0.706

As readly noted fron table I, the tree metodologies to determine V_T give different values but display similar tendencias in variation with channel length.

We have also characterized NMOS and PMOS transistors of a 0.18μm technology from TSMC with different channel-lengths. Fig. 4 shows the variation of the threshold voltage of PMOS transistors with different channel lengths.

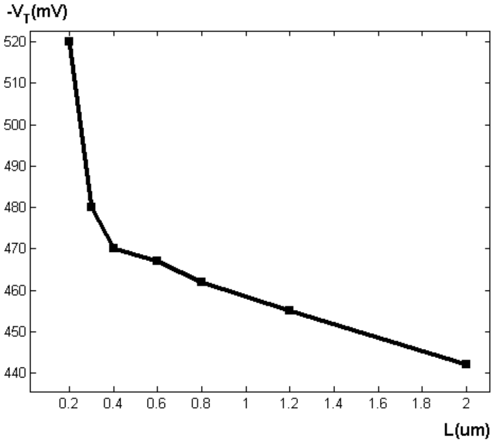

Fig.4. Threshold voltage vs. channel-length for a 0.18μm CMOS technology

The reverse short-channel effects are quite apparent in Fig. 4 and can be explained by the halo implants. The measurements we have taken for short and long-channel devices agree very well with the corresponding nominal V_T's of the technology.

CONCLUSION

The methodology described here provides a quick and reliable determination of the threshold voltage, with negligible influence of parasitic resistances, short-channel effects and transversal field degradation, owing to the regime of operation - linear region in weak and moderate inversion. The threshold voltage is evaluated according to its physical interpretation in the ACM model and its value closely agrees with the threshold voltage extracted through the extrapolation in the linear region. Using the procedure of this work to determine the threshold voltage we avoid the drawbacks of the ELR and SDL methodologies. Indeed, our method has a clear interpretation of the threshold voltage derived from physics, is not significantly affected by either series parasitic resistances or mobility degradation and the computation of second order derivatives of the current is not needed.

ACKNOWLEDGMENTS

The authors would like to thank CAPES and CNPq for the financial support and the MOSIS Educational Program for supplying the test devices.

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