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# UNCONVENTIONAL APPLICATIONS OF WIRE BONDING CREATE OPPORTUNITIES FOR MICROSYSTEM INTEGRATION

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**Abstract.** Automatic wire bonding is a highly mature, cost-efficient and broadly available back-end process, intended to create electrical interconnections in semiconductor chip packaging. Modern production wire bonding tools can bond wires with speeds of up to 30 bonds per second with placement accuracies of better than 2  $\mu\text{m}$ , and the ability to form each wire individually into a desired shape. These features render wire bonding a versatile tool also for integrating wires in applications other than electrical interconnections. Wire bonding has been adapted and used to implement a variety of innovative microstructures. This paper reviews unconventional uses and applications of wire bonding that have been reported in the literature. The used wire bonding techniques and materials are discussed, and the implemented applications are presented. They include the realization and integration of coils, transformers, inductors, antennas, electrodes, through silicon vias (TSVs), plugs, liquid and vacuum seals, plastic fibers, shape memory alloy (SMA) actuators, energy harvesters, and sensors.

## 1. Introduction

The main application of wire bonding technology is to create electrical interconnections between integrated circuit (IC) chips and their packages. The interconnections are formed by a thin metal wire, which is mechanically and electrically connected to the chip and to the package using a wire bonding tool. The requirements of the integrated circuit industry have pushed the development of the wire bonding processes towards higher speeds (number of bonds per second), improved reliability, increased density (in terms of bond pitch) and hence finer wires, and nonplanar topographies (e.g. multilayer stacks of thinned chips). Because wire bonding forms part of the back-end of semiconductor chip production, it is required to achieve exceptionally high reliability and yield in order to obtain the lowest possible packaging costs. Although alternative processes exist, such as flip-chip assembly and tape automated bonding [1], wire bonding continues to be a very important process in semiconductor packaging. This is partly due to the advantages of compliant wires under thermal and bending stress conditions, which results in high reliabilities of the packaged interconnections. It is estimated that more than  $4 \cdot 10^{12}$  wire bonds are produced annually [2].

The history of wire bonding was driven by the demands of the integrated circuit industry, resulting in high speed precision machines capable of forming microscopic metal wires into desired shapes. This begs the following question, which forms the focus and main hypothesis of this paper, namely: *Can this remarkable and mature micro-technology be used for other purposes?* As this paper will show, this is indeed possible, and the applications have high technical and possibly also commercial potential. After an overview of existing wire bonding technology, unconventional uses of wire bonding are reviewed and presented together with applications that have been reported in the literature.

## 2. Wire Bonding Technology - Overview

This section provides an overview of conventional wire bonding technologies, materials and tools, including a brief history of wire bonding.

### 2.1. Wire Bonding Mechanisms

In wire bonding, the attachment of a bond wire to a bond pad is realized by a joining process. The energy input for the joining process is a combination of force, temperature and/or ultrasonics. For standard wire bonding, three joining methods exist that are based and named after the type of energy input:

- Thermocompression (TC) bonding, first introduced in 1957 [3], uses mechanical force and a relatively high temperature on the order of 300 °C. TC is typically used for gold wire to gold pad wedge-wedge bonding. It is very sensitive to surface

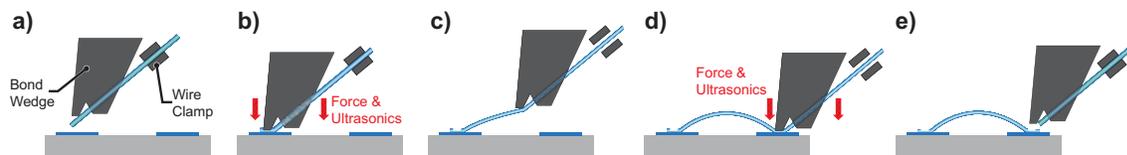
contaminants, requires high temperature and long process times and therefore has no significant commercial relevance today.

- Ultrasonic (US) bonding, introduced around 1960, is a room-temperature process and uses mechanical force and ultrasonic energy. US wedge-wedge bonding of aluminum wire to aluminum or gold pads enables the use of wires with large diameters (typically  $75 - 500 \mu\text{m}$ ) primarily for high-power electronic applications.
- Thermosonic (TS) bonding, introduced in 1970, is a combination of thermocompression and ultrasonic bonding and is typically used for ball-stitch bonding of gold wire to different pad materials. The combination of heat, ultrasound and force allows a moderate level of each type of input energy. Thermosonic bonding of thin wire (typically  $18 - 50 \mu\text{m}$ ) is today by far the most commonly used interconnection method in integrated circuit chip packaging.

## 2.2. Wire Bonding Process Technology

The two main wire bonding process technologies are ultrasonic wedge-wedge (figure 1 and 2) and thermosonic ball-stitch bonding (figure 3 and 4). The shape of the wire bonded interconnection is determined by the bonding tool used, which is typically either a wedge (figure 2 a) for wedge-wedge bonding or a capillary (figure 4 a) for ball-stitch bonding. The wedge generates two identical wedge bonds (figure 2 b) whereas the capillary generates first a ball bond (figure 4 c) and subsequently a stitch bond (sometimes called a crescent bond), as shown in figure 4 d. A ball and stitch bond generated by the capillary of a ball-stitch bonder has considerably larger dimensions with respect to the wire diameter compared to the wedge generated by a wedge-wedge bonder.

### 2.2.1. Wedge-Wedge Wire Bonding

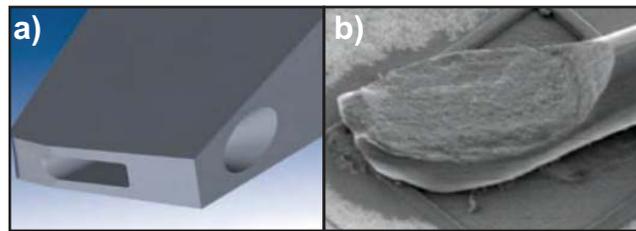


**Figure 1.** Process flow of standard wedge-wedge bonding.

Figure 1 illustrates an ultrasonic wedge-wedge bonding process, which typically employs aluminum wire that is bonded to aluminum or gold bond pads. Also copper wedge-wedge bonding was found to produce strong bonds at room temperature [4]. As shown in figure 1 a, the wire is fed through the tool towards the wedge. The wire is then pressed with a predetermined force against the bond pad. In addition, ultrasonic energy is simultaneously applied, which is generated by a transducer that vibrates the wedge parallel to the substrate and in a direction along the wire axis, with a frequency of typically  $120 - 140 \text{ kHz}$  [3], as depicted in figure 1 b. The tool then moves towards

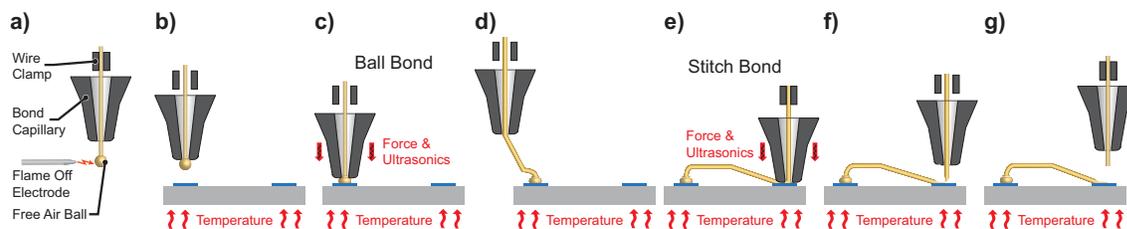
the second bond position (figure 1 c) and performs a second bond that is similar to the first one (figure 1 d). Finally, the wire clamp is closed and the wire is torn off directly behind the wedge by pulling back the tool, as depicted in figure 1 e. Ultrasonic wedge-wedge bonding of aluminum wire is an attractive room-temperature process and enables the use of both thin wire for fine pitch applications and thick wire for high power applications. However, automated wedge-wedge bonding tools are comparatively slow and have limitations in generating arbitrary loop shapes and directions [1, 3, 5].

Figure 2 a shows an SEM image of the lower part of a wedge tool that is typically made of tungsten carbide, titanium carbide or ceramic/metallic composites (cermet). The main features of a wedge tool are the feed hole, that is visible on the rightmost side and the exit hole in the center that are used to feed the wire towards the bond foot situated at the leftmost side. The bond foot is the part of the wedge tool that is in contact with the wire during the bond process and defines the impression in the bonded wire, as depicted in figure 2 b.



**Figure 2.** a) CAD image of a wedge for aluminum wire wedge bonding. b) SEM image of a wedge bond. Image courtesy of SPT Roth Ltd, Switzerland.

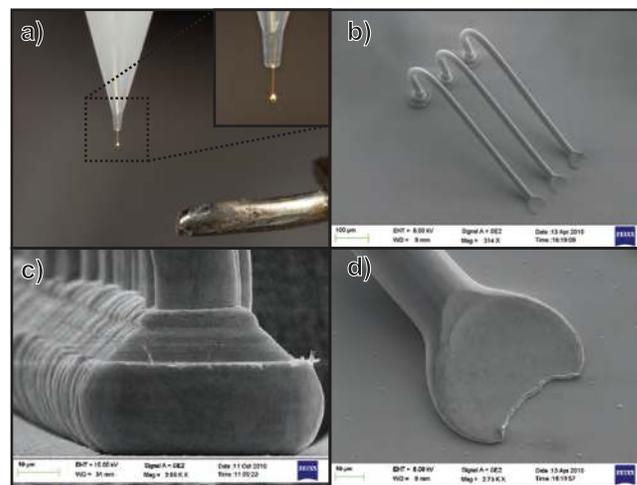
### 2.2.2. Ball-Stitch Wire Bonding



**Figure 3.** Process flow of standard thermosonic ball-stitch bonding of gold wire. A free air ball (FAB) is ball-bonded to a metal pad, and after generating a specific loop shape of the wire, it is stitch-bonded to the second bond pad.

Figure 3 a illustrates a thermosonic ball-stitch bond process using gold wire that is bonded to gold or aluminum pads. This technique and material combination is by far the most commonly used interconnection method in integrated circuit packaging. As shown in figure 3 a, gold wire is fed through a ceramic bond capillary, an electrical flame off (EFO) melts the wire and forms a gold sphere, the free air ball (FAB), at

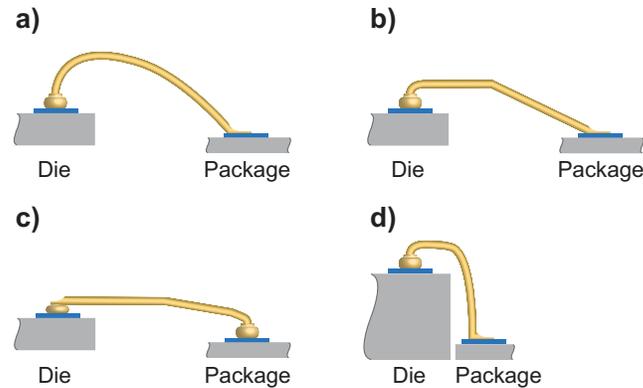
the end of the wire. The free air ball is then pulled up to the tip of the capillary and the tool moves laterally to a position above the desired bond pad on the device, which is placed on a heated work piece holder (figure 3 b). The tool then presses the free air ball with a defined force against the pad. Together with a simultaneous input of ultrasonic energy, the connection between the ball and the pad is generated, as depicted in figure 3 c. The tool moves then towards the second bond pad where the stitch bond is performed (figure 3 d and e). As shown in figure 3 e, the wire is compressed between one side of the capillary tip and the pad. Again force, ultrasonic and heat energy create the connection between the wire and the pad. The wire is torn off by closing the wire clamp and moving the tool straight up (figure 3 f - g).



**Figure 4.** a) Photo micrograph of a fine-pitch ceramic bond capillary (SBNS-35DP-C-1/16-XL, SPT Roth Ltd, Switzerland) with a 25  $\mu\text{m}$  gold bond wire and free air ball. The tip of the flame off electrode is visible in the lower right corner of the image. Inset: The tip of the capillary is tapered for fine-pitch applications. b) Scanning electron micrograph (SEM) image of three ball-stitch bonds with typical loop shape and a gold wire diameter of 25  $\mu\text{m}$ . c) SEM image of fine-pitch ball bonds with 20  $\mu\text{m}$  gold bond wire. d) SEM image of a stitch bond.

Thermosonic ball-stitch bonding of gold wire is the method of choice for most high-volume and low-cost applications and hence a very mature process, providing high reliability and throughput. This process offers the highest degree of freedom and flexibility for arbitrary loop shapes and directions of the bonded wire [1, 3, 5]. This is mainly due to the fact that the wire can be led off to any position with respect to the first bond position. The ball bond has a circular shape and hence offers a 360° freedom of movement of the bondhead and looping of the wire towards the second bond position. Wedge-wedge bonding in contrast has a more limited freedom of movement of the bondhead due to the predetermined direction of the wire that is caused by the wedge bond [3, 5]. In ball-stitch bonding, various loop shapes, mainly driven by shrinking package sizes, have been implemented over the years. Common loop shapes in electronics packaging are depicted in figure 5. The standard loop with a rounded

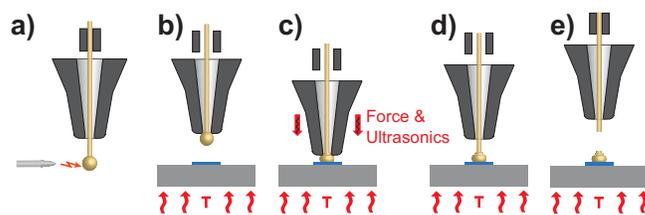
wire profile (figure 5 a) can be modified to a flat loop (figure 5 b) in order to create a lower loop profile and thereby reduce the volume of the package. More specialized loops with even lower wire profiles can be created by reverse bonding (figure 5 c). In reverse bonding first a ball bump is placed on the die. Then a ball bond is performed on the lead and the wire is then stitch bonded on the ball bump on the die. Figure 5 d depicts another type of loop that is used for ultra small chip scale packages (CSP).



**Figure 5.** Some representative examples of loop shapes that can be created by ball-stitch wire bonding. a) Standard forward loop. b) Flat forward loop. c) Reverse loop. d) Chip scale package (CSP) loop.

### 2.2.3. Gold ball bumping

Gold ball bumping is a variation of ball-stitch bonding and is widely used to create gold-to-gold interconnections for flip-chip packages used e.g. in HB LEDs and CMOS imagers [6]. The estimated cost per 100,000 ball bumps is approximately \$ 14 in high-volume [6] and thus, ball bumping can be cost competitive towards wafer-level plating processes for scenarios with I/O counts on that order or below.

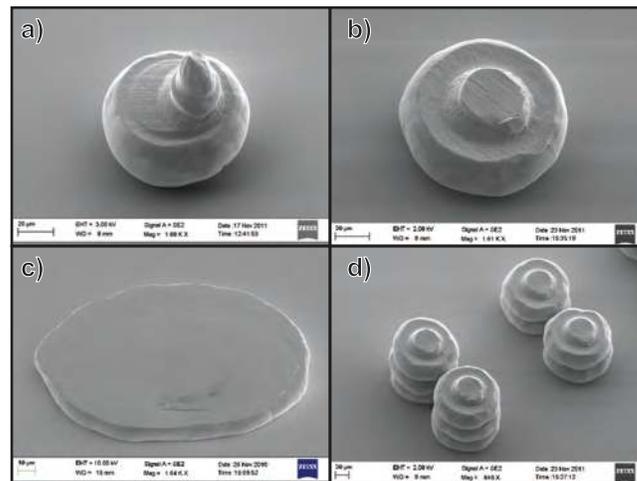


**Figure 6.** Ball bumping process flow. A free air ball is ball-bonded to a metal pad and the wire is subsequently torn off.

Gold bumps are typically formed on wafer-level according to the procedure illustrated in figure 6. Similar to the ball-stitch bonding process, an electrical flame off (EFO) forms the free air ball, as depicted in figure 6 a. The free air ball is then thermosonically bonded to a pad with the help of force, ultrasonics and temperature (figure 6 c). Instead of performing a second stitch bond, the tool now moves to a certain

height where the wire is torn off by closing the wire clamp and moving the tool straight up (figure 6 d and e).

After bumping, the wafer is typically diced, flipped and thermosonically bonded to a substrate with corresponding gold pads. Figure 7 a and b show standard gold ball bumps. In ball bumping it is common to planarize the top surface of the bumps. This technique is called coining and creates uniform bump heights, flat bump surfaces and an increased bond area, as shown in figure 7 c. Ball bumping also enables the stacking of multiple bumps, as depicted in figure 7 d. This is a commonly used technique to create higher standoffs between flip-chip bonded dies [1, 7]. Wire-bonded ball bumps can serve as an alternative to regular TSVs and have already been implemented in mass-produced devices such as CMOS image sensors [8]. However, this method is restricted to TSVs with low aspect ratios and thin substrates as the possible dimensions of ball bumps are limited.



**Figure 7.** SEM images of a) a standard Au ball bump, b) a low-profile Au ball bump, c) a coined ball bump and d) stacks of two and three ball bumps.

### 2.3. Materials Used in Wire Bonding

All wire bonding processes are limited to certain material combinations and can be sensitive to imperfections and contamination of the bond pad surfaces [1, 3, 5]. Commercially relevant and well-developed wire-pad material combinations are Au-Au, Au-Al, Au-Cu, Au-Pd, Al-Au, Al-Al and Al-Ni. Strongly emerging wire-pad material combinations are Cu-Al and Cu-Cu due to a more attractive commodity price of copper as compared to gold [3, 9]. For mainstream wire bonding, copper wire is now firmly established and many resources are focused on optimization of this process [10–12]. Other, more exotic wire-pad combinations such as Pd-Al [13, 14], Pt-Pt [15], Ni-SiC [16], Ag-Au [17], Ag-Al [18] and Ag-SiC [19] have been reported as well. Currently, the vendor Microbonds is alone in developing coated bond wires, an activity that started with X-Wire [20] and has continued with nano-metrically thin metallic coatings, although other

efforts are known [21]. X-Wire is standard gold bond wire with an electrically-insulating coating that does not hinder the ball-stitch bonding process, but requires a separate electrical connection to the wire tail end to permit ball formation. X-Wire is called so because it permits crossing bond wires to touch without a direct ohmic path being formed. It also has a high dielectric break-down voltage of more than 10 kV. As such, the wire is exceptionally well suited for new applications where wire sections may have to be placed adjacent to each other.

#### ***2.4. Wire Bonding Process Simulation***

The current state of the wire bonding business is such that most equipment owners do not have access to predictive simulations for any of the steps involved in wire bonding, and hence are completely dependent on the vendors, on generic simulation programs, or on ad hoc experiments in order to optimize process recipes. The reason appears to be that the market for a simulation toolset is currently too small. As we shall see, most of the efforts in wire bonding simulation have been made either by equipment vendors, or by research groups, and have principally been an aid to understanding, and not yet intended as tools for prediction.

Each individual step of the automatic ball-stitch wire bonding process has its own challenge that requires separate simulation capabilities: 1. Free air ball forming, 2. thermosonic ball bonding, 3. looping, and 4. wire fracture. Previous work to characterize, by simulation, the wire-bonding process has focused on the different wire bonding steps, which are briefly address here:

##### *2.4.1. Free air ball (FAB) forming*

The exact shape of the ball, as formed by the surface tension forces of the molten metal, is crucial for subsequent bonding success, and depends strongly on the electrical flame off parameters. Chen et al. [22] performed extensive studies of the parameters based on the Taguchi method, resulting in a best parameter set that can be used in a look-up table method. Tan et al. [23] improved upon this method by developing a semi-empirical model for varying wire diameter and electrical flame off conditions. Ball size prediction via a semi-empirical numerical method was achieved by Qin et al. [24] and Tan et al. [23, 25].

##### *2.4.2. Thermosonic ball bonding*

General concerns for the thermosonic ball bonding process include the bonding strength, and damage to the substrate. Of central importance is also wire weakening due to the heat affected zone (HAZ), which is typically 100  $\mu\text{m}$  to 150  $\mu\text{m}$  along the wire away from the ball. All reports [26–32] perform the necessary elasto-plastic simulation using commercial finite element packages, notably Ansys [33] and Abaqus [34]. By far the most reports have been about whether the bond is properly formed when the wire is

attached to the wedge along a very thin stripe at the apex of the wedge geometry, on the bonded-wire side of the capillary landing position. The geometry causes a strong stress concentration in the wire, which is sufficient to initiate fracture when the wire is pulled from the substrate. The pulling force required for fracture is achieved by applying a wire clamp to the wire, preventing slippage relative to the capillary, and then retracting the capillary away from the substrate. Most studies done on determining the breaking force and resulting morphology are experimental [35–37]. However, Shah et al. [37] presents a dedicated CMOS sensor for in situ online measurement of bond forces. This study was supported by extensive dynamic finite element modeling of the entire capillary assembly [33]. A simulation model for a CMOS wire bond stress sensor was created in [38]. The sensor, placed underneath the bond pad, performs real-time monitoring of the stress components in the plane during the ball or wedge formation processes. Software was used to predict the behavior of one such sensor, ultimately yielding vastly improved process conditions for ball bond formation.

### 2.4.3. Looping

The first reported simulation capability for wire bond looping is based on the finite element method reported in [39]. The method is quasi static, implying that inertial effects are not consistently taken into account. Soon thereafter the same group reported an extension to include dynamical effects [40, 41]. A further effort is found as a patent [42] and in two journal papers [43, 44]. The reported simulation method addresses the consistent computation of looping in the vertical (2D) plane of a conventional ball-stitch wire bond. The wire is represented as a chain of wire segments (the linkages) and springs connecting the segments. The springs implement the discrete bending in the elasticity and plasticity of the wire, whereas the linkages implement the inertia of the wire. The spring’s elastic stiffness is computed from the bending stiffness of the wire using beam theory. The model implements two plasticity modes, either elastic-perfectly-plastic or a softening model. A variable boundary condition for the capillary travels along the wire and defines the inertial force on the (time-dependent) wire end. The authors report a variety of simulated looping profiles for gold wire, showing that the model performs very well and is able to accurately predict the final shape of 2D wire bond profiles. In [45] they embed the simulator in a neural network optimizer. Published reports on the improvement of looping appears to be dominated by experimental reports, and are reported mainly by the workers of the machine vendor K&S [27, 46, 47] and a packaging supplier [48]. A central concern is associated with higher density of wire bonds, and low wire profiles on multi-chip packages. The goals are to avoid short-circuiting (which can also be alleviated with insulated wire), wire damage at chip edges, and robustness of long wire sweeps during the subsequent injection moulding process [48, 49].

#### 2.4.4. Wire fracture

The studies found on determining the breaking force and resulting morphology after wire fracture are experimental [35, 37, 50]. However, [37] presents a dedicated CMOS sensor for in situ online measurement of bond forces, and this study, which also focuses on the ball bond force, was supported by extensive dynamic finite element modeling with Ansys [33] of the entire capillary assembly.

### 2.5. Wire Bonding Equipment

Manufacturers of wire bonding equipment typically design and assemble highly specialized tools for dedicated fields of application, as indicted in table 1.

**Table 1.** Overview of most common wire bonding tool types.

<p><b>Fine wire bonding tools</b> Most commonly used tool for standard interconnections in integrated circuit packaging with wire diameters up to 50 <math>\mu\text{m}</math>. These tools have the highest level of maturity in terms of throughput, accuracy, bond-pitch, reliability and control of the wire bonding process.</p>
<p><b>Thick wire bonding tools</b> Wedge-wedge bonding tools are typically used for high-power interconnections that require thick wires with diameters up to 500 <math>\mu\text{m}</math>.</p>
<p><b>Ball bumping tools</b> Most regular ball-stitch bonding tools typically offer a bumping function as integral part of the software, however more specialized tools exist as well. These bumping tools are characterized by additional features such as larger bonding areas for full wafer bumping and special coining tools.</p>
<p><b>Deep access bonding tools</b> Specially designed bondheads and bond capillaries and wedges enable wire bonding in deep cavities and narrow packages.</p>
<p><b>Ribbon wire bonding tools</b> Gold and aluminum ribbon wire bonding is very attractive for interconnections in microwave circuits. The rectangular shape of ribbon wire has a lower high frequency impedance and hence lower losses compared to regular circular bond wires.</p>

Two distinctive design concepts for wire bonding tools exist. The hybrid bonder concept has a bondhead, which is situated at a fixed position and has a movable workpiece holder on an xy-stage. In contrast, tools based on a pantograph [51] or flying bondhead concept [52] have a movable bondhead with a workpiece holder at a fixed position. The flying bondhead concept offers highest performance in terms of throughput and hence process cost. This comes however to the disadvantage of limited process flexibility and small bond areas. Hybrid bonders can have interchangeable bondheads, with the work piece holder mounted on a moving stage with long travel paths. This concept offers a much higher flexibility, larger bonding area and better bond reliability compared to tools with flying bondheads. The main drawback of this concept is however a lower throughput. The substrate handling associated with both kinds of tools ranges from manual over semi-automated to fully automated [5].

The current market leader of wire bonding equipment manufacturers is Kulicke and Soffa Industries, Inc. (K&S), including Orthodyne Electronics [53]. They offer a wide spectrum of most types of manual as well as fully automated tools. Other suppliers for highly automated production equipment are Shinkawa Ltd. [54], ASM Pacific Technology Ltd. [55], Hesse & Knipps GmbH [56] and Palomar Technologies [57].

A number of equipment suppliers, such as Questar Products International Inc. [58], West Bond Inc. [59], Hybond Inc. [60] and TPT [61] offer smaller and less automated equipment partly with customized solutions mainly intended for prototyping and research. F & K Delvotec Bondtechnik GmbH [62] offers, besides a number of table-top tools, an automated hybrid wire bonding platform with interchangeable bondhead modules for ball-stitch bonding, thin and thick wire wedge-wedge bonding, deep access bonding as well as ribbon bonding.

The current market for automated wire bonding equipment for high throughput is extremely competitive. Manufacturers are therefore unlikely to provide individual customization of single tools, unless there is a strong market demand. Low-level access to the software, which can be essential for many unconventional wire bonding approaches, as described in this review paper (e.g. arbitrary loop shapes), is typically not provided. Manufacturers of hybrid wire bonding equipment, in contrast, are often focused on meeting special customer demands and can provide customizations of the tool and its software. They often provide extensive tool and software options, customized training as well as process assistance.

## ***2.6. A Brief History of Wire Bonding***

The history of wire bonding is written by only a few companies that, with few exceptions, already got involved during the initial period of the integrated circuit business, and a number of them are still going strong. Wire bonding was first reported in 1957 by a team from Bell Telephone Laboratories, who already described both wedge and capillary based ball bonding [63]. Remarkably, the authors performed experiments with gold wire diameters ranging between 5  $\mu\text{m}$  and 250  $\mu\text{m}$ . Each bond was reported to take from seconds to minutes to form. The method was termed thermocompression bonding. A successful bond required to elevate the temperature of the substrate to somewhere between 200 °C and 300 °C, and applying 35 – 70 MPa of pressure. Already in 1959, Kulicke and Soffa Industries, Inc. (K&S) introduced the first commercial thermocompression bonder. The bonder was based on a device that Western Electric (the manufacturing division of Bell Telephone Laboratories) had developed in-house and had commissioned K&S to industrialize [53].

Ultrasonic bonding of metals was first patented by Sonobond Ultrasonics, Inc. [64] in 1960. The company initially supplied the ultrasonic transducers for wire bonding to other vendors, and later built their own wire bonder. The next important step came in the 1960s, when thermosonic bonding was first reported [65], a method which has become the industry standard because of its low temperature, pressure, and adaptability.

Apart from the equipment, wire bonding relied on a fundamental understanding of thin metal film and wire metallurgy under processing conditions, as initiated by [66]. Wire bonds require capillaries to guide the wire and transmit the pressure for the bond. The first commercial capillary for wire bonding was introduced in 1967 by the Gaiser Tool Company [67]; they followed with the first ceramic capillary in 1970.

In 1967 the first automatic wire bonder for transistors was introduced into the marketplace by Shinkawa Ltd. [54], who, in 1970, introduced the first automatic wire bonder for ICs in Japan, with exports starting in 1976. A year later, in 1971, the first fully automatic wire bonder was introduced by Shinkawa Ltd. The extension to copper came a decade later in 1986 [54].

A year after Shinkawa Ltd., Texas Instruments Inc. [68] introduced the ABACUS II wire bonder in 1972, based on its in-house CPU TI-960A. ABACUS is an acronym for Alloy, Bond, Assembly Concept, Universal System. The bonder was sold for \$ 15,000 and could bond 375 16-pin chips per hour, and already placed bonds with a positional accuracy of 6  $\mu\text{m}$  [69].

The Swiss company ESEC was founded in 1968 with its first product, a die bonder, and as a relative latecomer, in 1973 they produced their first simultaneous transistor wire bonder capable of 2500 units per hour. In 1978 ESEC introduced a fully digital automatic wire bonder, and in 1989 the company introduced their "flying bondhead technolog" [52], which is based on a frictionless air bearing technology for the bondhead that enabled very high bonding speeds. In 2011, ESEC Ltd became part of BE Semiconductor Industries N.V. [70].

### **3. Unconventional Applications of Wire Bonding**

In this section, unconventional uses and applications of wire bonding are reviewed and discussed. These technologies are organized in three sub-sections. In the first sub-section, applications are discussed that make use of wire and substrate material combinations that are standard for electrical chip interconnections in chip packaging applications, so that the shape of the wire, and the application, makes it unusual. In the second sub-section, applications are discussed that departs from common wire and substrate material combinations. In the third sub-section, applications are discussed that explore wire and substrate material combinations that are not bondable in the conventional manner, so that the bonding process is unusual.

#### ***3.1. Unconventional Applications of Wire Bonding Using Standard Wire-Pad Material Combinations***

One of the key opportunities represented by the wire bonder is the ability to form micro-structures directly from micron-sized metal wire stock. Through the combination of wire stock and the kinematics of the bondhead and capillary, wire loops and indeed the rapid formation of solenoids are hence within the realm of the micro-technologist.

To date, a range of morphologies have been explored, mainly to achieve electrical coils, as exemplified in Table 2.

Without modification, the standard loops available from automatic ball-stitch wire bonder tools can already produce useful parts of on-chip solenoids. For example, [71] has produced a range of coil topologies with the axis of the coil lying parallel to the wafer surface (Table 2-l,m,n). By first preparing a wafer with metal tracks, each terminating in a bond pad, the formation of standard wire bond loops between select bond pads results in solenoidal topologies. In this way, a fairly tight winding pattern, merely limited by the capillary diameter, can be produced. By arranging the pattern in a star-like fashion, a toroidal topology was achieved (Table 2-m). By placing a high permeability ring core over the metallization pattern, a transformer with a completely closed flux path was achieved (Table 2-n). In an interesting variation, [72] has performed extensive modelling of spiral topology on-chip inductors formed from straight section wedge-wedge bonded wirebond loops, with each of the three windings in a triangular arrangement. In this way, 27 nH inductors with 1  $\Omega$  resistance were found to be feasible.

In [73], an on-chip process is described, which achieved reasonably high aspect ratio tightly wound solenoids, with standard gold wire wrapped around perfectly cylindrical posts (Table 2-a). The wire was ball-stitch bonded using an ESEC 3100+ automatic wire bonder to standard gold wire bond pads, thereby completing the electrical connection. The cylindrical cores of the solenoids, also called yokes, were formed from thick SU-8 that was lithographically patterned onto both silicon and pyrex wafers. A lower reliable limit coil size was found to be 100  $\mu\text{m}$  diameter, with an SU-8 yoke wall thickness of 30  $\mu\text{m}$ . Due to the induced bending moment at the base of the posts, 100  $\mu\text{m}$  diameter posts could be wound up to 200  $\mu\text{m}$  above the substrate before breaking, yielding solenoids with an aspect ratio of 2:1 at this small size.

Several issues were reported that pertain to the bondhead trajectory in combination with high-speed movement. For example, excess wire would be thrown in a lasso-like manner, yielding loosely-wound coils. In this way it was found that the capillary should follow the post at a distance no greater than 600  $\mu\text{m}$ . A further issue was the low number of coordinates provided by the machine's software, which limited the geometries that could be traversed. On the electrical side, the solenoids showed characteristic values for impedance that closely followed established theory. For example, 1 mm diameter coils with 5 windings showed a resonance at roughly 2.6 GHz. The inductance closely followed the formula of Wheeler [74].

Other papers [75, 76] report on posts of up to 1 mm height made of poly methyl acrylate (PMMA, or Plexiglas) through deep X-ray lithography via synchrotron radiation. Special structures comprising of four posts and integrating a vernier gauge were formed that, upon winding, would indicate the deformation and strain of the posts. Standard wire bonding settings caused the 1 mm high posts to each bend 2  $\mu\text{m}$  during winding.

Based on the above capability, [77, 78] presented the first application of wire-bonded coils for on-chip magnetic resonance imaging of tiny samples (Table 2-b). Wire-

bonded coils were produced, tuned and matched to 400 MHz for use in a 9.4 T Nuclear Magnetic Resonance (NMR) magnet as  $^1\text{H}$  proton spin resonance detectors. A distinct advantage for Nuclear Magnetic Resonance (NMR) and Magnetic Resonance Imaging (MRI) was the ability to place a low-noise amplifier chip in the direct neighbourhood of the coil, either by flip-chip bonding, or by pre-integration into the substrate below the coil. The mechanical robustness of the coils enabled the production of so-called inductively coupled magic angle spinning (MACS) NMR detectors [79, 80] (Table 2-c), which achieved a remarkable detection limit of  $10^{13}$  protons or 330 lp of sample dissolved in deuterated water ( $\text{D}_2\text{O}$ ).

By forming microcoils at three different heights above the substrate surface, it is possible to produce overlapping microcoil arrays. In [81, 82], an array of seven mutually overlapping microcoils, each of around 2 mm diameter, was produced (Table 2-d). Each microcoil was tuned to 400 MHz and matched to  $50\ \Omega$ . Due to the overlap, the coils have minimal ( $< 18$  dB) crosstalk, making them suitable as individual (NMR) channel receivers, or as members in a phased array arrangement. In this setup, it was possible to demonstrate both NMR spectroscopy of 7 separate micro compartments filled with analyte, as well as MRI of planarly extended (high aspect ratio) samples.

Instead of overlapping, it is possible to produce microcoils in a concentric arrangement. The main limitation in arrangement density is the space required for the wire bond capillary, which must be able to pass between support structures and the growing coil thickness during the winding process. In [83], two concentric microcoils were produced to form a micro-levitation actuator (Table 2-e). The inner coil, which has a higher density of magnetic field lines, was utilized to produce the lift force in a metallic micropart above the coil using Radio Frequency (RF) excitation in the coil, with induced eddy currents causing an opposing electromagnetic force and hence the onset of levitation. The second, larger concentric coil was used to produce a stabilizing field so that the part remained perfectly above the centerline of the coil arrangement.

For a smallest implementation with only 1.5 windings, it is currently possible to create wire-bonded microcoils with a fundamental radio-frequency resonance of 50 GHz, and higher modes approaching the THz range. This points the way towards unique metamaterial structures, as demonstrated by [84], reporting on a large and regular array of microcoil resonators (Table 2-f). Because of the chirality of each coil (which planar coils do not have), the metamaterial resonance constructively interferes with the incoming RF wave to cause a phase shift among the perpendicular electric and magnetic field phasors, so that the propagating wave is thereby circularly polarized.

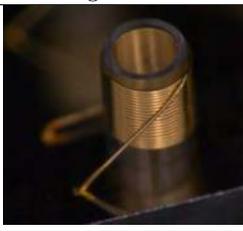
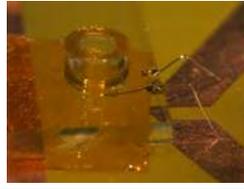
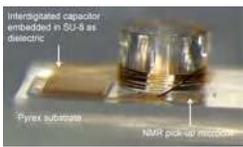
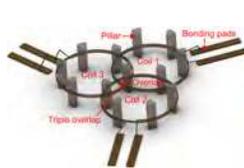
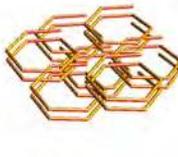
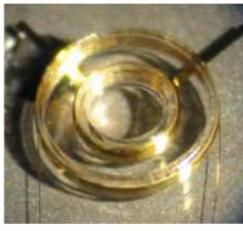
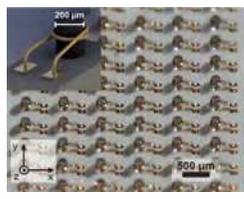
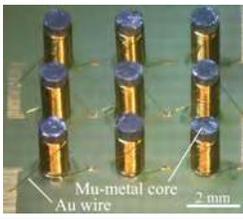
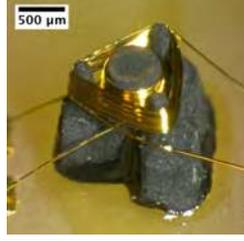
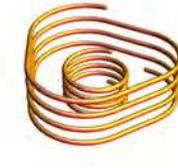
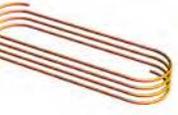
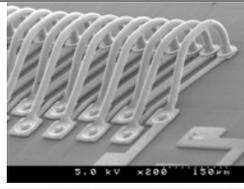
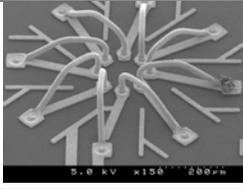
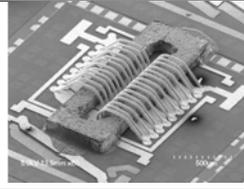
Microcoils have potential as electromagnetic devices, such as microtransformers or microactuators. However, in order to extend into this domain, it is essential to develop coil yokes, in this case also denoted cores, made of high permeability materials. In [85], a variety of cores were investigated, including iron and glass capillaries, which potentially could be filled (Table 2-g). Also, an array of iron-core coils was serially connected, so as to enhance the achievable voltage generated in an energy harvesting application. In a series of papers [86–89] the Shen group report various details of a wire bond based

on-chip monolithic buck converter. A ferrite epoxy mixture is formed and precisely dispensed onto wire-bonded solenoids formed by wire loops with closing conductors formed by on-chip metal patterns. The authors claim to achieve frequencies of up to 5 MHz for 2.5 V and current levels of up to 120 mA. Cho et al. [90] reports a similar topology, seven-wire air-core wire bond transformers with very low insertion loss of  $-1.54$  dB at 1.9 GHz, which outperforms spiral on-chip inductors of the same footprint of about  $0.5$  mm<sup>2</sup>, probably due to the low loss core. In [91] multilayered magnetic cores are used to create transformers with a coupling factor of 97 % and a transformer efficiency of 73 %. Lin et al. [92] created a transformer pair from two bowed parallel wire bond pairs, formed on a chip carrier so as to have an extended air core in order to achieve a reasonably low loss RF transformer for Ultra High Frequency (UHF) and Very High Frequency (VHF) signals. The paper reports quality factors below 15, and coupling factors below 0.5. On the other end of the spectrum, [93] produced a cast and laser-micromachined super-paramagnetic micro-core around which two concentric coils were wound, thereby achieving a fully functional transformer (Table 2-h). The digital performance of the transformer (130 Mb/s), as well as its power transfer capabilities in a DC-DC converter arrangement, points the way to on-chip digital isolation in a very low-cost implementation with back-end compatibility.

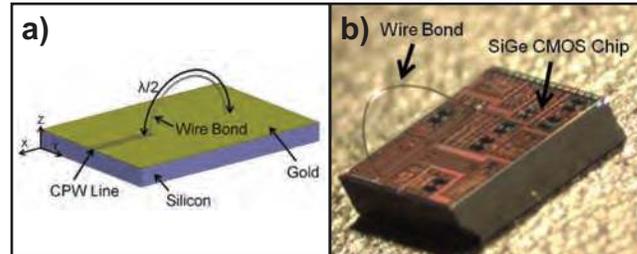
It is also possible to create non-circular solenoidal structures as exemplified in table 2. In principle, the posts around which the wire is wrapped and hence plastically deformed can be used to define other shapes. By lithographically forming SU-8 posts, [81] has formed hexagonal coils, [94] has produced a low self-capacitance basket coil (Table 2-j), and [95] has formed a longitudinal magnetic resonance microgradient coil (Table 2-k). In [96], PMMA is structured via laser to form a yoke around which a record 100 windings are wound (Table 2-i). A suspended magnet system vibrates in the core of the microcoil, thereby harvesting mechanical vibrations electromagnetically.

Because of the close tolerancing available, bond wire structures have also been explored for use as RF devices. As shown in figure 8, by forming a single semicircular loop between two separated bond-pads, Willmot [98–100] has created a half-wavelength loop antenna at 40 GHz for use in an on-chip radio. The CMOS and SiGe chip's surface is covered with a gold layer to form the ground-plane, and an antenna efficiency of up to 81% is reported. In a second paper, the same group reports a Yagi-Uda antenna array of multiple common-fed loops [101], also with high efficiency. Wu et al. [102] report an optimized bond-pad wire bond pair used as 60 GHz short distance radio link. The wire bond is formed between the chip and a substrate PCB, much as conventional wire bonding, but optimized for its antenna characteristics. The paper claims 1 Gb/s over 10 cm, with an error rate of less than  $10^{-12}$ , for communication between devices on the same PCB within the unlicensed band. Chen et al. [103] report on a CMOS integrated 43 GHz inter-chip data link with a 6 Gb/s data rate over 4 cm. Ndip et al. [104, 105] propose novel 3D electromagnetic models of bond wire antennas in order to study their radiation characteristics as well as the impact of process tolerances on the performance of

**Table 2.** Micro-inductors and micro-coils.

Coil image	Coil morphology	Data	Coil image	Coil morphology	Data
		a) MRI [97]; SU-8 and PMMA post, solid and tubular; round shape; helical winding, single layer.			b) MRI [77]; SU-8 post, tubular; round shape; helical winding, single layer.
		c) NMR-MACS [80]; SU-8 post, tubular; round shape; helical winding, single layer, with adjacent capacitor.			d) MRI, NMR [82]; SU-8 post, solid; hexagonal shape, overlapping in 3 layers; helical winding, single layer.
		e) Levitation [80]; SU-8 post, tubular; round shape, concentrically nested; helical winding, double layer.			f) THz meta-material [84]; SU-8 post, solid; round shape, large rectangular array, non-overlapping; helical 1.5 winding, adjacent capacitor.
		g) Energy harvester [85]; glass post, metal; round shape; helical winding, single layer.			h) Transformer, DC-DC converter [93]; Post Fe <sub>3</sub> O <sub>4</sub> ; concentric, inner round, outer triangular; helical winding, multilayer.
		i) Energy harvester [96]; PMMA post, movable magnet; shape racetrack; helical winding, multilayer, 100 windings.			j) Low-C inductor [94]; SU-8 post; helical 7-pointed star winding, 4 times.
		k) Gradient coil [95]; SU-8 post; meander shape; single layer and winding.			l) Inductor [71]; no post; metal core; shape wire bond.
		m) Inductor [71]; no post; metal core; shape wire bond.			n) Inductor with core [71]; No post; metal core; shape wire bond.

bond wire antennas. Chen et al. [106] form minimal inductances from a straight segment of a bond wire in an integrated contactless RF switch and tunable filter arrangement. The authors report a power isolation level of 10 dB, by using piezoelectric thin film driven capacitor plates to vary the air gap for a capacitance range of 4:1.



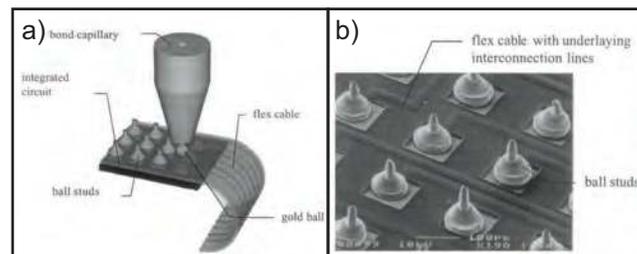
**Figure 8.** a) A wire bonded antenna integrated onto a SiGe chip. b) Diagram of simulated antenna and feeding structure, from [98].

In order to overcome the space limitations of on-chip waveguides, Lim et al. [107] have created slow wave structures for the lower GHz frequency range from co-planar on-chip capacitor plates connected via wire bonds to form a classical lumped LC transmission line structure. The authors claim to be a factor 1.6 better than comparable completely on-chip structures, and can achieve the required large inductance and capacitance at low footprint and low mask expense. Harkness et al. [108] theoretically investigate the case of the formation of closely spaced wire bonded parallel loops among adjacent or stacked chip dies, thereby forming coplanar transmission lines from the 3 mm diameter wire connections. The paper claims that losses below 2.2 dB for signals up to 20 GHz are achievable in a fully matched (to  $50 \Omega$ ) setup. In addition, a number of similar wire bonded antenna implementations have been reported [109–112].

Another productive area of wire-bond exploration is RF signal conditioning. Khatri et al. [113] employ two orthogonally placed sets of three chip-to-substrate wire bonds that connect to the RF electronics to form a band pass differential Butterworth filter structure for the lower GHz decade, exploiting the mutual inductance of adjacent wires and the accurate on-chip capacitors. Similarly, [106] uses patterned capacitors and wire bond lengths as inductors to form an RF structure, connected to an integrated MEMS RF switch. In order to achieve microwave filter tunability, Zhou et al. [114] have created a hierarchy of capacitive and inductive patches close to a three-pole microstrip filter on a low-loss substrate. The substrate can then be measured whilst clamped in the wire bonder. In order to tune the filter, sections of inductance or patches of capacitance can be added to shift the centre frequency of the filter, or match its input and output ports. The tunability range is reported to be 7%. Segura et al. [115] have studied the effect of tip-to-tip connections via wire-bonding for interdigitated, otherwise planar capacitors. Through this arrangement, the tips of the fingers of the same electrode are connected, thereby removing resonances associated with the length of the fingers and extending the useful frequency range of the capacitor. Wire bonding provides an inexpensive alternative to achieve the metallic connections without further mask-based

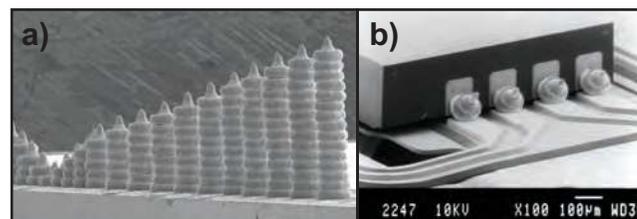
processing. In [116] an RF switch and tunable filter MEMS structure is reported that uses piezoelectric capacitors to drive the plates of a capacitor apart for tuning. To achieve low-value yet low-cost inductor, a wirebond connects two interdigitated contact pads to form the complete RF circuit. Values of 300 to 600 pH are reported. An unusual wire bonding process is reported in [117], who use an ultrasonic anvil to join a length of resin coated Cu wire simultaneously to two Sn bumps 600  $\mu\text{m}$  apart, formed on a ceramic substrate, so as to form an inexpensive yet accurate inductor.

One of the early unconventional uses of wire bonders was reported by Stieglitz et al. in [118–120], in which the ball bumps were used as rivets to attach, both mechanically and electrically, a flexible micro-ribbon to a microchip. The main target was for neural prosthesis applications. This idea was later picked up in [121], for use in implantable MEMS with an attached micromachined flex cable, achieving contact resistances below 1  $\text{m}\Omega$ .



**Figure 9.** a) Overview of the ball bonding Microflex technique. b) SEM micrograph of the contact array. All gold balls are aligned on the contact pads [118].

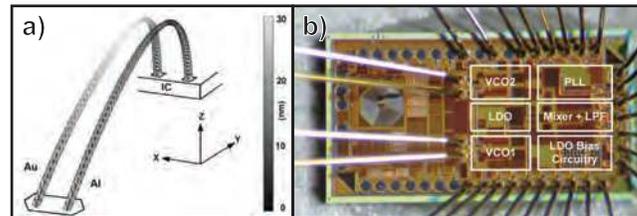
The ball bump can also be used as a complete printing platform, and Pai et al. [122] have combined wire bonding with imprinting in an interesting manner. By first forming a ball bump on a gold plated wafer substrate, it is then reshaped through plastic deformation using a previously prepared silicon microstructured stamps. As a result, the mirror image of the stamp is copied into the gold bump, which can then be used in the usual micro- or nanoimprint manner. The paper claims to achieve structure dimensions down to 400 nm.



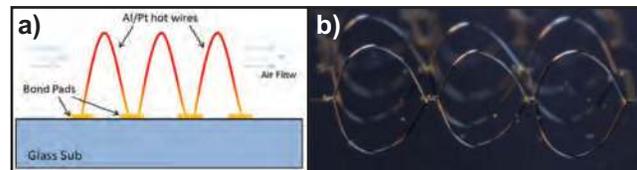
**Figure 10.** a) Stacked gold ball bumps, "The Great Wall of Bumps, 1 to 15", from [123]. b) An unusual application of ball bonding that forms an electrical connection between conductors in two different planes, from [3].

Vertical wire bond studs, out of the wafer or chip plane, are useful structures in their own right. Tonomura et al. [124] have created a chemical analysis chip that uses

an array of 16 wire bond stud wires, protruding above the chip surface and into a liquid channel formed above the chip. The wires can sense electrochemical potentials in the liquid over a distributed volume relative to a platinum counter electrode. The ball-stitch bond wires were formed between pads on the chip and pads on a frame structure. After wire bonding, the looped wires were laser cut, leaving wire studs connected to the chip surface. In another work, stacked ball bumps were used to build up entire metal pillars and walls as shown in figure 10 a [123] and ball bumps were used to contact pads that are situated on the sidewall of a chip by placing the ball bumps in an angle, as shown in figure 10 b [3].



**Figure 11.** a) FEM simulation of the bond wire deflection for 1g acceleration along the X-axis. b) A micrograph of the accelerometer IC [125].

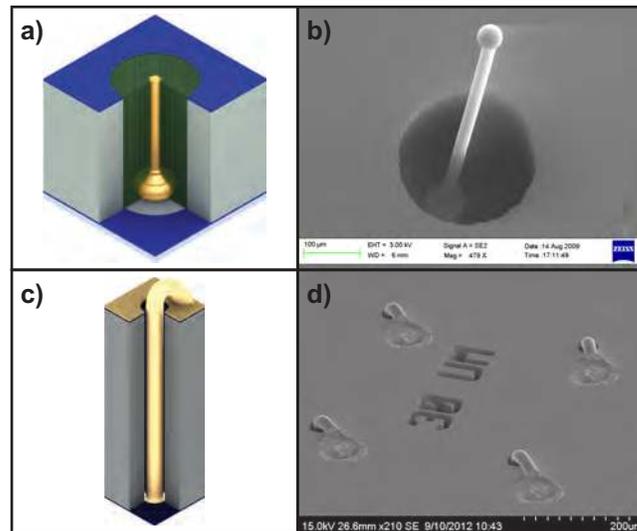


**Figure 12.** a) Schematic drawing of a hot-wire thermal flow sensor. b) Fabricated hot-wire sensors. The image shows bonded wires over the Cr/Au pads [126].

Another interesting application of wire bonding is the use of parallel bond wires as movable masses in an accelerometer for very-low-cost sensor applications, as shown in figure 11 [125, 127, 128]. Therefore, parallel bond wires are connected to the sensor read-out electronic circuit. The wire movement due to external acceleration forces changes their capacitance, which can then be measured as the sensor signal. Schröder et al. [129] have implemented a novel die attachment method based on wire bonding. In this approach, bond wires are used both as electrical interconnection and as mechanical fixation of the die in order to minimize thermal and mechanical stresses in the package. In another work, micro-scale hotwire anemometers for air-flow sensing have been fabricated by using wire-to-wire bonding of aluminum bondwires, as shown in figure 12 [126]. Wire-to-wire bonding of aluminum bondwires has also been used to fabricate electric solar wind sails for spacecraft propulsion applications [130].

Yet another application of wire bonding is the fabrication of through-silicon vias (TSVs) as shown in figure 13. Figure 13 a and b depict a TSV concept that has been optimized for applications with requirements for low capacitive coupling to the substrate.

The main feature of this TSV design is the metal core, which is a gold wire that is wire bonded to an aluminum pad at the bottom of the via hole. This concept is however limited to comparable low aspect ratios on the order of 1.5 : 1 [131]. In order to realize TSVs with higher aspect ratios (up to 20 : 1) another concept has been implemented by Schröder et al. [132]. As depicted in figure 13 c and d, a gold wire is fed into the via hole with the help of a wire bonder and then temporarily fixated by a stitch bond. In both concepts the remaining hollow space in the via hole is filled with a low- $\kappa$  polymer, which acts both as an electrical insulator resulting in low capacitive coupling towards the substrate and as a buffer for thermo-mechanical stress. Wire bonding easily enables the fabrication of high-quality and inherently void-free metal cores with high aspect ratios. Other variations of using wire bonding for the fabrication of TSV have also been proposed in [133–137]. Khandros et al. [138] propose to utilize wire bonds as flexible contact probes for probe cards that are used as an interface between an electronic test system and a semiconductor wafer that is to be tested. Standard wire bonding using gold wires has also been proposed to seal through substrate holes for the sealing of liquids in cavities [139–141]. This approach is described in detail in section 3.3.

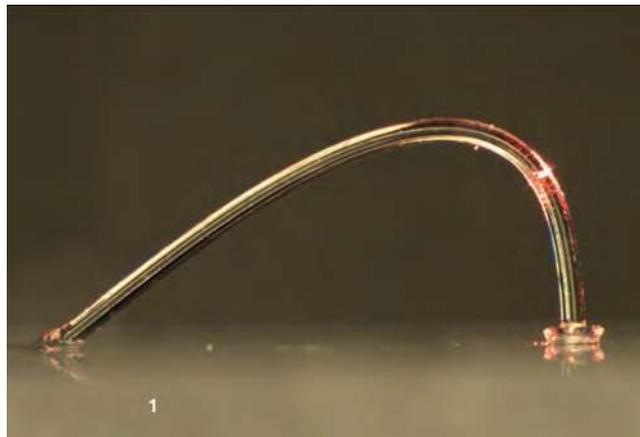


**Figure 13.** Through silicon via (TSV) concepts based on wire bonding technology: a) Conceptual CAD image of a wire-bonded through-silicon via with low capacitive substrate coupling. b) SEM image of the conductive core of the via, which consists of a gold wire that has been wire-bonded on a metal membrane on the bottom of the cavity [131]. c) Conceptual CAD image of a wire-bonded through-silicon via with high aspect ratios. d) SEM image of gold wires that have been inserted in via holes [132].

### ***3.2. Unconventional Applications of Wire Bonding Using Non-Standard Wire-Pad Material Combinations***

For many applications it is desirable to integrate nonstandard wire materials into a microsystem. This requires the implementation of specialized wire bonding processes



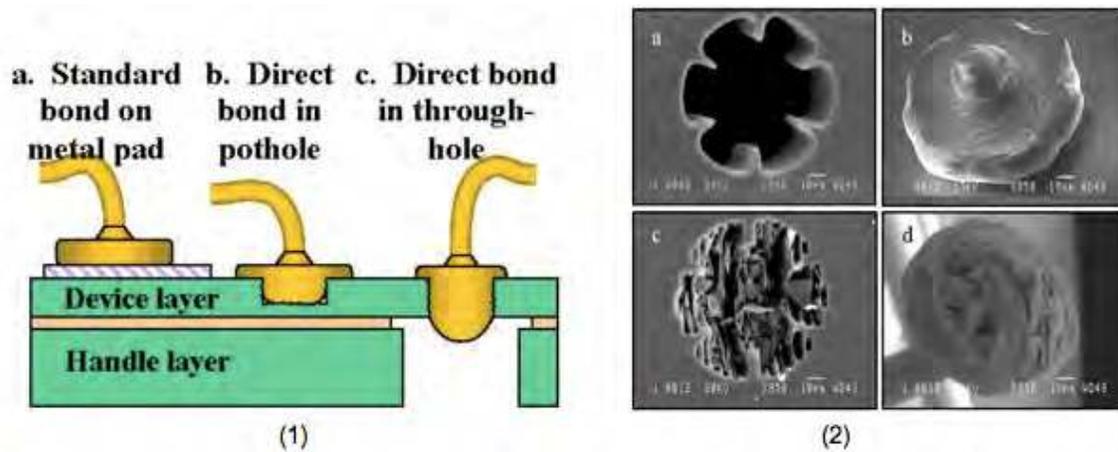


**Figure 15.** Ball-stitch bonded polymer light fiber [148].

Polymer wires for use in wire bonding have earned interest recently. Partly driven by a need, in silicon photonics, to route optical signals on-chip and between chips, different research groups have studied suitable interconnecting methods to couple light between electro-optical components. In a concept called optical wire bonds, flexible polymeric waveguides were used to carry the light. The waveguides, fabricated in polyimide by conventional microfabrication techniques, were manually transferred as wires and used to interconnect two laser diodes with a reported waveguide loss of 2 dB/cm [149]. In another study, optical wire bonding is realized through the use of optical probes of bimorph strips consisting of SU-8 and a flexible backbone of Polydimethylsiloxane (PDMS) [147]. The flexible optical probes were connected to single mode optical fibers at one end and pressed against on-chip waveguides at the other end, as shown in figure 14. Coupling efficiencies were reported that are sufficient to transfer light from the probes into the integrated waveguides. The authors suggested the probes as an optical wire bonding platform for optical coupling between fiber connectors to planar lightwave circuits [150]. The transfer of optical wire bonding to commercially available wire bonder tools was investigated by Schmitz et al. [151]. The group used a thick-wire bonder with a 60 kHz sonotrode to form wedge-wedge bonds of a polymeric wire (fiber) [148]. Similarly to conventional metallic wire bonding, both the wire and the substrate were locally melted by the applied energy causing the materials to fuse and bond. Ball-stitch bonding was also studied and realized by modifying the wire feed-through of a thin-wire bonder (figure 15). Also in this instance, ultrasonics was used to create the ball bond. For ball formation, the authors report that the best method, over other options such as laser and gas flame heating, was to mechanically move the wire tip onto a hot surface [148]. Although the bonding procedure was successful, it was reported that the typical loop shaping ability that was present for plastically deformable metallic wires was very limited. Sharp bends gave rise to cracks in the fiber, which caused distortions when used as an optical waveguide [151]. The light coupling capability was also verified and measured to 1 – 2 dB loss for out-of-plane ball bonds. Wedge bonds

were less suited for out-of-plane coupling but proved better for in-plane coupling, such as for edge emitters and special types of LEDs [148]. Related to this, photonic wires for optical chip-to-chip interconnections have also been fabricated by non-wire bonding techniques such as direct-write two-photon lithography [152].

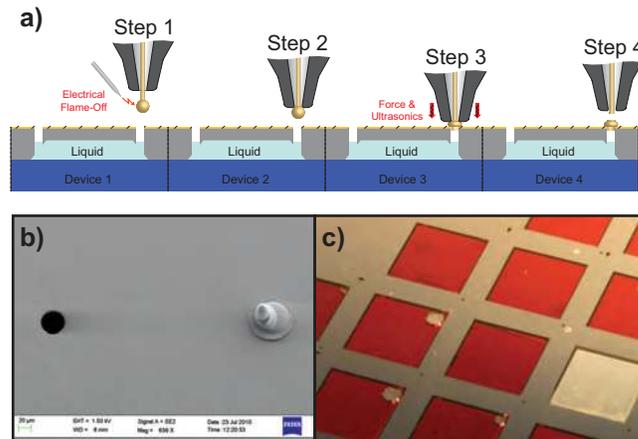
### 3.3. Applications Using Wire Bonding in Combination with Clamping and Anchoring Structures for Attachment of Innovative Non-Bondable Wire Materials



**Figure 16.** Method for wire bonding directly on a silicon surface: (1) a) Standard wire bond on metal pad as reference, b) Ball bond in a pothole, and c) bond-ball in a through-hole. (2) SEM images: a) Through-hole before direct-bonding. b) Ball bond directly bonded to the pothole in the silicon substrate. c) pothole after pull-test. d) The Si fins fractured in pull-test and remained fixed to the bond-ball [153, 154].

There are a number of wire materials and wire-pad material combinations that are very attractive for use in microsystem applications but that cannot be easily wire bonded with conventional technologies. Examples are the attachment of metal wires directly to Si surfaces, thus circumventing the use of bond pads; and wire bonding of wire materials such as NiCr or shape memory alloys (SMA) that have interesting properties for high-performance micro actuator applications. To extend the usefulness of wire bonding to a much wider range of materials, a number of approaches have recently been proposed that are either based on plastic or elastic deformation of the bond wire, or that employ special structures on the target substrate to clamp and fix the wire onto the substrate. For these cases, the ability of the wire material to fuse and bond to the target surface is not essential. Thus, the existing wire bonding infrastructure can in principle be used to integrate almost any type of wire material [153–157]. In one of these approaches, the free air balls of Au wires are mechanically pressed, with the help of a wire bond tool, into potholes and through-holes etched into a silicon substrate as illustrated in figure 16 [153, 154]. Thereby, the free air balls plastically deform and mechanically wedge into the opening on the substrate. The original aim of this work

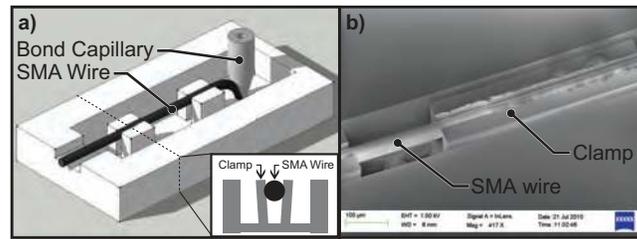
was to create reliable electrical and mechanical contacts to the Si substrate, without the need for depositing metal bond pads. The electrical conductivities and mechanical bond strengths that have been achieved in this work are comparable to those obtained by standard wire-bonds using conventional wire-pad material combinations.



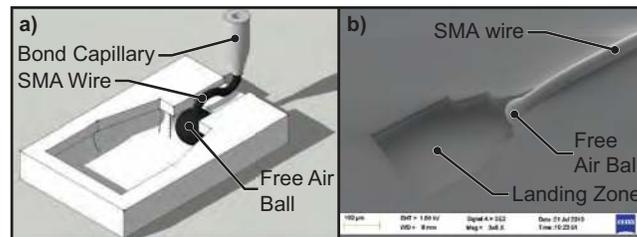
**Figure 17.** Hermetic sealing of liquids in cavities by wire bump bonding: a) Gold ball bumping is used to seal fluid access ports of cavities. b) Cross sectional view of a wire bonded plug in a 30  $\mu\text{m}$  diameter fluid access port. c) Cavities filled with red dye that is seen through the glass cap wafer. [139, 140].

In subsequent work, wire bonding was used to push free air balls of Au wires into access ports of micro-cavities that contain liquids as shown in figure 17 [139, 140]. The free air balls plastically deform and thereby hermetically seal the openings of the cavities. Room-temperature hermetic sealing of the liquid in cavities was demonstrated with extremely high throughput of more than 15 wire bonded plugs per second. In an extension of this work, hermetic encapsulation and sealing of vacuum atmospheres inside micro-cavities was demonstrated by a combination of wire bump bonding and subsequent wafer-level compression bonding in a vacuum chamber in order to seal the vacuum inside the cavities [141, 158]. In this process, gold bumps are bonded with an offset on the open access ports of vacuum cavities on a wafer. The offset is used in order to not fully cover and clog the access ports. Thereafter, a polished Si wafer is placed on the bumps of the wafer with the cavities and the wafer stack is placed in a wafer bonder. The chamber of the wafer bonder is evacuated to a pressure of  $10^{-5}$  mbar and the bumps are pushed into the holes, thereby plastically deforming the Au bumps and hermetically sealing the access ports and hence, the vacuum inside the cavities.

For wire materials that are very hard and brittle, such as shape memory alloys (SMAs) (e.g. TiNi or NiCr), it is not possible to use methods utilizing plastic deformation of the free air ball or the bond wire to connection to the bond pad material on the target substrate. Instead, elastically or plastically deformable structures can be created on the target substrate that allow wedging, mechanical clamping or interlocking of the rigid wire. Such an approach was demonstrated by employing compliant clamping structures that were etched from a Si substrate [155–157]. An SMA wire was then



**Figure 18.** a) Conceptual 3D drawing of a cantilever-based clamp, and b) SEM image of a single clamp with an integrated SMA wire. The wire is pushed in between a pair of cantilevers with the help of the wire bonder [155–157].



**Figure 19.** a) Conceptual 3D drawing of an anchor structure and b) SEM image of an anchor structure with an integrated SMA wire. A wire bonder is used to anchor SMA wires with a free air ball in a tapered and underetched silicon structure [155–157].

squeezed in the Si clamps using a wire bonding tool. The elastic deformation of the clamps reliably fixed the SMA wire by frictional forces as indicated in figure 18. Different types of generic clamping structures were proposed and successfully evaluated [155–157]. In the same report, the authors demonstrated mechanical interlocking structures that were etched into the Si target substrate. Free air balls can be formed even at the wire ends of extremely hard materials. They can then be placed and interlocked with the structures as shown in figure 19. This approach, together with the clamping structures shown in figure 18, allows the implementation of a conventional ball-stitch wire bond process flow [155–157]. To reinforce wires that are fixated by frictional forces from clamping structures, additional soft-metal wire bumps have been proposed that plastically deform and wedge with the bond wire that is placed in clamping structures [157].

The research reviewed in this section shows that it is possible to generate wire attachments by mechanical press, interlocking and wedge structures, which are largely independent of the wire materials used. This can be achieved either by plastically deforming the wire or free air ball while wedging it into a dedicated rigid or deformable structure on the target substrate during the wire bond process. Alternatively, the same effect can also be achieved by plastically or elastically deforming dedicated fixation structures on the target wafer when less ductile wire materials are used.

#### 4. Outlook

The applications reviewed in this paper reveal that wire bonding is a fast and flexible microstructuring tool, with growing potential for new applications, as new process capabilities are being explored. Wire bonding is a viable approach for efficiently integrating wire materials with interesting properties into micro-structures, and thereby enabling heterogeneous microsystems [159]. The flexibility of the wire bonding process has been probed by numerous groups, despite the fact that wire bonder kinematics are not generally available in "open access" format, and we have found reports on successful modifications to bonding, looping, feedstock, and choice of substrate.

A clear trend in all new applications is that the wire bond is no longer just an electrical connection, even though this application will probably dominate the scene. The wire feedstock is now also being used as a preformed micro-structural component, and this trend will certainly continue. We also see a clear trend towards rapidly produced on-chip and interconnected electrical passive components, formed with less effort and using less microchip real-estate than when lithographic techniques are employed. In this sense, the wire bonding process is moving from the back-end to the front-end of the manufacturing chain. Another interesting trend is the switch from conventional wire bonding metals (gold, copper, silver) to other materials (exotic metals, glass, polymers), which open the door to untold applications, including micro actuation and light transmission. We also expect wire bonded structures to be formed on unusual substrates, which will include new polymeric materials, as well as non-planar topographies. Taken together, the matrix formed by geometry, application domain, material, and substrate, all work together to create the potential for many unthought of new uses for wire-bonding technology.

#### 5. Conclusions

The maturity, low-cost and high speed of wire bonding makes it a versatile tool for wire integration in applications beyond electrical chip interconnections. In recent research publications, a variety of innovative microsystems have been implemented by using wire bonding technology, including coils, transformers, inductors, antennas, electrodes, through silicon vias (TSVs), plugs, liquid and vacuum seals, plastic fibers, shape memory alloy (SMA) actuators, energy harvesters, and various sensors. Many of these applications have significant technical and commercial potential. Furthermore, wire bonding provides new opportunities to implement and manufacture novel and innovative microsystems from microwire feedstock. Due to the existing infrastructure, easy access and low-cost, wire bonding may even enable commercial manufacturing of low and medium-volume microsystem devices that would otherwise not be economically viable. With increased efforts in developing flexible wire bonding processes and innovative device solutions beyond electronic packaging applications, wire bonding may become a generic manufacturing technology for many emerging and as yet unknown microsystem

applications.

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## References

- [1] W. J. Greig, *Integrated Circuit Packaging, Assembly and Interconnections*. Springer, 2007.
- [2] I. Lum, C. J. Hang, M. Mayer, and Y. Zhou, "In Situ Studies of the Effect of Ultrasound During Deformation on Residual Hardness of a Metal," *Journal of Electronic Materials*, vol. 38, pp. 647–654, May 2009.
- [3] G. G. Harman, *Wire Bonding in Microelectronics: Materials, Processes, Reliability, and Yield*, 3rd ed. McGraw-Hill Professional, 2010.
- [4] Y. Tian, C. Wang, I. Lum, M. Mayer, J. Jung, and Y. Zhou, "Investigation of ultrasonic copper wire wedge bonding on au/ni plated cu substrates at ambient temperature," *Journal of Materials Processing Technology*, vol. 208, no. 1-3, pp. 179 – 186, 2008.
- [5] S. K. Prasad, *Advanced Wirebond Interconnection Technology*, 1st ed. Kluwer Academic Publishers, 2004.
- [6] V. McTaggart, L. Levine, and G. Dunn, "Stud bumping and die attach for expanded flip chip applications," *Advanced Packaging*, September 2004.
- [7] L. Levine, "Ball bumping and coining operations for TAB and flip chip," in *Electronic Components and Technology Conference, 1997. Proceedings., 47th*, may 1997, pp. 265 –267.
- [8] J. Baron, "Stud bumping serves as TSV alternative for BSI image sensor in latest iPhone 4," Yole Developpement, Tech. Rep. 17, 2010.
- [9] C. Hang, C. Wang, M. Mayer, Y. Tian, Y. Zhou, and H. Wang, "Growth behavior of cu/al intermetallic compounds and cracks in copper ball bonds during isothermal aging," *Microelectronics Reliability*, vol. 48, no. 3, pp. 416 – 424, 2008.
- [10] K. Toyozawa, K. Fujita, S. Minamide, and T. Maeda, "Development of copper wire bonding application technology," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 13, no. 4, pp. 667 –672, dec 1990.
- [11] J. Lee, M. Mayer, Y. Zhou, J. Moon, and J. Persic, "Influence of gold pick up on the hardness of copper free air ball," *Microelectronics Reliability*, vol. 51, no. 1, pp. 30–37, 2011.
- [12] M. Mayer and Y.-S. Lai, "Copper wire bonding," *Microelectronics Reliability*, vol. 51, no. 1, pp. 1–2, 2011.
- [13] H. P. Thiede, "Bonding wire today and tomorrow," in *Electronics Packaging (IEPS), 2nd International Conference on*, 1982, pp. 686–705.
- [14] A. Bischoff, F. Aldinger, and W. Heraeus, "Reliability criteria of new low cost materials for bonding wires and substrates," in *IEEE Electronic Components, 34th Conference on*, 1984, pp. 411–417.
- [15] J. Mantese and W. Alcini, "Platinum wire wedge bonding: A new IC and microsensor interconnect," *Journal of Electronic Materials*, vol. 17, pp. 285–289, 1988, 10.1007/BF02652107.
- [16] R. Burla, L. Chen, C. Zorman, and M. Mehregany, "Development of nickel wire bonding for high-temperature packaging of SiC devices," *Advanced Packaging, IEEE Transactions on*, vol. 32, no. 2, pp. 564 –574, may 2009.
- [17] Q. Chen, A. Pagba, D. Reynoso, S. Thomas, and H. Toc, "Cu wire and beyond - Ag wire an alternative to Cu?" in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, dec. 2010, pp. 591 –596.
- [18] L. J. Kai, L. Y. Hung, L. W. Wu, M. Y. Chiang, D. S. Jiang, C. Huang, and Y. P. Wang, "Silver alloy wire bonding," in *Electronic Components and Technology Conference (ECTC)*, 2012, pp. 1163–1168.
- [19] N. Heuck, F. Baars, A. Bakin, and A. Waag, "Development of a wire-bond technology for SiC high temperature applications," *Materials Science Forum*, vol. 645-648, pp. 749–752, 2010.

- [20] R. Lyn, J. I. Persic, and Y. K. Song, "Overview of X-Wire insulated bonding wire technology," in *39th International Symposium on Microelectronics IMAPS*, 2006.
- [21] Z. Zhong, "Wire bonding using insulated wire and new challenges in wire bonding," *Microelectronics International*, vol. 25, no. 2, pp. 9–14, 2008.
- [22] J. Chen and Y. Lin, "A new approach in free air ball formation process parameters analysis," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 23, no. 2, pp. 116–122, 2002.
- [23] Y. Tan, B. Toh, H. Ho, and J. Tan, "Free air ball modeling for gold wire bonding for different wire diameters," in *Proc. 6th Electronic Packaging Technology Conference, Singapore*, Dec 2004, pp. 711–717.
- [24] W. Qin, I. Cohen, and P. Ayyaswamy, "Ball Size and HAZ as Functions of EFO Parameters for Gold Bonding Wire," *Advances in Electronic Packaging*, vol. 1, pp. 391–398, 1997.
- [25] Y. C. Tan, B. H. Toh, H. M. Ho, and J. Tan, "Free air ball modeling for gold wire bonding for different wire diameters," in *IMAPS Taiwan Technical Symposium*, 2006.
- [26] Z. Z. W. and K. S. Gon, "Analysis and experiments of ball deformation for ultra-fine-pitch wire bonding," *Journal of Electronics Manufacturing*, vol. 10, no. 4, pp. 211–217, 2001.
- [27] B. Chylak, S. Komar, and G. Perlberg, "Optimizing the wire bonding process for 35-um ultra-fine-pitch packages," in *Proceedings Semicon Singapore*, 2001, pp. A1–A7.
- [28] Y. Takahashi and M. Inoue, "Numerical study of wire bonding—analysis of interfacial deformation between wire and pad," *Journal of Electronic Packaging*, vol. 124, no. 1, pp. 27–36, 2002. [Online]. Available: <http://link.aip.org/link/?JEP/124/27/1>
- [29] D. Degryse, B. Vandefelde, and E. Beyne, "Mechanical FEM simulation of bonding process on Cu low k wafers," *IEEE Trans. Comp. Packaging*, vol. 27, pp. 643–650, 2004.
- [30] S. Murali, N. Srikanth, Y. M. Wong, and C. J. Vath, "Fundamentals of thermo-sonic copper wire bonding in microelectronics packaging," *Journal of Materials Science*, vol. 42, no. 2, pp. 615–623, Murali2007.
- [31] A. Viswanath, X. Zhang, V. Ganesh, and L. Chun, "Numerical study of gold wire bonding process on cu/low-k structures," *Advanced Packaging, IEEE Transactions on*, vol. 30, no. 3, pp. 448–456, 2007.
- [32] Y. Liu, S. Irving, and T. Luk, "Thermosonic wire bonding process simulation and bond pad over active stress analysis," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 31, no. 1, pp. 61–71, 2008.
- [33] ANSYS, Inc. website. [Online]. Available: <http://www.ansys.com>
- [34] Dassault systemes website. [Online]. Available: <http://www.simulia.com>
- [35] J. Lee, M. Mayer, Y. Zhou, and S. Hong, "Iterative optimization of tail breaking force of 1mil wire thermosonic ball bonding processes and the influence of plasma cleaning," *Microelectronics Journal*, vol. 38, no. 8-9, pp. 842–847, Aug. 2007.
- [36] J. Lee, M. Mayer, Y. Zhou, S. Hong, and S. M. Lee, "Tail breaking force in thermosonic wire bonding with novel bonding wires," *MATERIALS SCIENCE FORUM*, vol. 580/582, pp. 201–204, 2008.
- [37] A. Shah, M. Mayer, Y. Zhou, S. Hong, and J. Moon, "In situ ultrasonic force signals during low-temperature thermosonic copper wire bonding," *Microelectronic Engineering*, vol. 85, no. 9, pp. 1851 – 1857, 2008. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0167931708002694>
- [38] R. Osorio, M. Mayer, J. Schwizer, J. Korvink, and H. Baltes, "Simulation procedure to improve piezoresistive microsensors used for monitoring ball bonding," *Sensors and Actuators A: Physical*, vol. 92, no. 1–3, pp. 299 – 304, 2001,  $\text{\textit{Selected Papers for EuroSensors XIV}}$ . [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0924424701005878>

- [39] A. A. O. Tay, B. C. Seah, and S. H. Ong, "Finite element simulation of wire looping during wirebond fabrication," *ASME J. Elect. Packaging*, 1998.
- [40] B. Ng, A. Tay, and S. Ong, "Three dimensional finite element simulation of wire looping process in wirebonding," in *Electronics Packaging Technology Conference, 2002. 4th*, dec. 2002, pp. 334 – 337.
- [41] A. Tay, B. Ng, and S. Ong, "Dynamic and quasi-static three dimensional simulation of wire-looping process in wirebonding," in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*, 27-30, 2003, pp. 1330 – 1333.
- [42] Y.-L. Lo, T.-L. Ho, J.-L. Chen, and S.-L. Wu, "Profile design for wire bonding," US Patent US 6178540, 2001.
- [43] Y.-L. Lo, T.-L. Ho, J.-L. Chen, R.-S. Lee, and T.-C. Chen, "Linkage-spring model in analyzing wirebonding loops," *Components and Packaging Technologies, IEEE Transactions on*, vol. 24, no. 3, pp. 450 –456, sep 2001.
- [44] Y.-L. Lo, T.-C. Chen, and T.-L. Ho, "Design in triangle-profiles and t-profiles of a wirebond using a linkage-spring model," *Components and Packaging Technologies, IEEE Transactions on*, vol. 24, no. 3, pp. 457 –467, sep 2001.
- [45] Y.-L. Lo and C. Tsao, "Integrated taguchi method and neural network analysis of physical profiling in the wirebonding process," *Components and Packaging Technologies, IEEE Transactions on*, vol. 25, no. 2, pp. 270 –277, jun 2002.
- [46] D. Calpito, I. Qin, E. Pasamanero, E. Theint, and C. Tok, "Very long, ultra-low-loop testing for new bonding wire development," in *Proc. SEMICON Singapore*, 2006.
- [47] Saraswati, E. P. P. Theint, D. Stephan, F. W. Wulff, C. D. Breach, and D. R. M. Calpito, "Looping behaviour of gold ball bonding wire," in *6th Electronics Packaging Technology Conference*, 2004.
- [48] R. Groover, W. Shu, and S. Lee, "Wire bond loop profile development for fine pitch-long wire assembly," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 7, no. 3, pp. 393 –399, aug 1994.
- [49] H. Kung, C. Huang, and A. Chanyshev, "On the study of loop profiles in improving the sweep stiffness of wire bond," *9th Electronics Packaging Technology Conference, EPTC*, pp. 472–477, 2007.
- [50] J. Lee, M. Mayer, N. Zhou, and J. Persic, "Microelectronic wire bonding with insulated au wire- effects of process parameters on insulation removal and crescent bonding," *Materials Transactions, The Japan Institute of Metals*, vol. 49, no. 10, pp. 2347–2353, 2008.
- [51] D. Vischer, "Wire bonder," US Patent 7,159,751 B2, 2007.
- [52] S. Thuerlemann, "Bondhead for a wire bonder," US Patent 6,460,751, 2002.
- [53] Kulicke and Soffa Industries, Inc. website. [Online]. Available: <http://www.kns.com>
- [54] Shinkawa, ltd. website. [Online]. Available: <http://www.shinkawa.com>
- [55] ASM Pacific Technology, Ltd. website. [Online]. Available: <http://www.asmpacific.com>
- [56] Hesse and Knipps Semiconductor Equipment GmbH website. [Online]. Available: <http://www.hesse-knipps.com/>
- [57] Palomar technologies website. [Online]. Available: <http://www.palomartechnologies.com/>
- [58] Questar Products International, Inc. website. [Online]. Available: <http://www.questarproducts.com/>
- [59] West Bond Inc. website. [Online]. Available: <http://www.westbond.com/>
- [60] Hybond, Inc. website. [Online]. Available: <http://www.hybond.com/>
- [61] Tpt wire bonder website. [Online]. Available: <http://www.tpt-wirebonder.com/>

- [62] F and K Delvotec Bondtechnik GmbH website. [Online]. Available: <http://www.fkdelvotec.com/>
- [63] O. L. Anderson, H. Christensen, and P. Andreatch, "Technique for connecting electrical leads to semiconductors," *Journal of Applied Physics*, vol. 28, no. 8, pp. 923–923, 1957.
- [64] Sonobond ultrasonics, inc. website. [Online]. Available: <http://www.sonobondultrasonic.com>
- [65] A. Coucoulas, "Ultrasonic welding of aluminum leads to tantalum thin films," *Trans. Met. Soc. AIME*, vol. 236, pp. 587–589, December 1966.
- [66] J. W. Beams, *Structure and Properties of Thin Films*, C. A. Neugebauer, C. A. Newkirk, and D. A. Vermilyea, Eds. Wiley, New York, 1959.
- [67] Gaiser Tool Company website. [Online]. Available: <http://www.gaisertool.com>
- [68] Texas instruments, inc. website. [Online]. Available: <http://www.ti.com>
- [69] "Integrated-circuit wire bonder, international historic mechanical engineering landmark designated march 31," Texas Instruments Incorporated, Tech. Rep., 1992. [Online]. Available: <http://files.asme.org/asmeorg/Communities/History/Landmarks/1488.pdf>
- [70] BE Semiconductor Industries N.V. website. [Online]. Available: <http://www.besi.com>
- [71] J. J. Wang, "On-chip inductors and transformer," in *Applied Power Electronics Conference and Exposition, 2010. APEC 2010. Twenty-Fifth Annual IEEE*, 2010.
- [72] G. Villar, J. Delos, and E. Alarcon, "Bonding-wire triangular spiral inductor for on-chip switching power converters," in *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*, may 2011, pp. 817–820.
- [73] K. Kratt, M. Seidel, M. Emmenegger, U. Wallrabe, and J. Korvink, "Solenoidal micro coils manufactured with a wire bonder," in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2008, pp. 996–999.
- [74] H. Wheeler, "Simple inductance formulas for radio coils," *Proceedings of the Institute of Radio Engineers*, vol. 16, no. 10, pp. 1398–1400, oct. 1928.
- [75] K. Kratt, V. Badilita, T. Burger, J. Mohr, M. Börner, J. Korvink, and U. Wallrabe, "High aspect ratio PMMA posts and characterization method for micro coils manufactured with an automatic wire bonder," *Sensors and Actuators A: Physical*, vol. 156, no. 2, pp. 328–333, 2009.
- [76] V. Badilita, K. Kratt, T. Burger, J. Korvink, and U. Wallrabe, "3D high aspect ratio, MEMS integrated micro-solenoids and helmholtz micro-coils," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2009, pp. 1106–1109.
- [77] V. Badilita, K. Kratt, N. Baxan, M. Mohmmadzadeh, T. Burger, H. Weber, D. v. Elverfeldt, J. Hennig, J. G. Korvink, and U. Wallrabe, "On-chip three dimensional microcoils for MRI at the microscale," *Lab Chip*, vol. 10, pp. 1387–1390, 2010.
- [78] V. Badilita, K. Kratt, N. Baxan, J. Anders, D. Elverfeldt, G. Boero, J. Hennig, J. Korvink, and U. Wallrabe, "3D solenoidal microcoil arrays with CMOS integrated amplifiers for parallel MR imaging and spectroscopy," in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2011, pp. 809–812.
- [79] V. Badilita, B. Fassbender, O. Gruschke, K. Kratt, R. Meier, D. Sakellariou, J. Korvink, and U. Wallrabe, "Inductively coupled wirebonded microcoils for wireless on-chip NMR," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2011, pp. 2798–2800.
- [80] V. Badilita, B. Fassbender, K. Kratt, R. Meier, D. Sakellariou, J. Korvink, and U. Wallrabe, "Single chip probe for high resolution magic angle coil spinning NMR of biological samples," in *Proc. MicroTAS*, Oct 2011, pp. 1314–1316.
- [81] O. Gruschke, L. Clad, N. Baxan, K. Kratt, M. Mohmmadzadeh, D. von Elverfeldt, A. Peter, J. Hennig, V. Badilita, U. Wallrabe, and J. Korvink, "Multilayer phased microcoil array for magnetic resonance imaging," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2011, pp. 962–965.

- [82] O. G. Gruschke, N. Baxan, L. Clad, K. Kratt, D. von Elverfeldt, A. Peter, J. Hennig, V. Badilita, U. Wallrabe, and J. G. Korvink, “Lab on a chip phased-array MR multi-platform analysis system,” *Lab Chip*, vol. 12, pp. 495–502, 2012.
- [83] V. Badilita, S. Rzesnik, K. Kratt, and U. Wallrabe, “Characterization of the 2nd generation magnetic microbearing with integrated stabilization for frictionless devices,” in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2011, pp. 1456–1459.
- [84] S. Waselikowski, K. Kratt, V. Badilita, U. Wallrabe, J. G. Korvink, and M. Walther, “Three-dimensional microcoils as terahertz metamaterial with electric and magnetic response,” *Applied Physics Letters*, vol. 97, no. 26, pp. 261 105–261 105–3, dec 2010.
- [85] B. Mack, K. Kratt, M. Sturmer, and U. Wallrabe, “Electromagnetic micro generator array consisting of 3D micro coils opposing a magnetic PDMS membrane,” in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2009, pp. 1397–1400.
- [86] H. Jia, J. Lu, X. Wang, K. Padmanabhan, and Z. J. Shen, “Integration of a monolithic buck converter power ICw and bondwire inductors with ferrite epoxy glob cores,” *Power Electronics, IEEE Transactions on*, vol. 26, no. 6, pp. 1627–1630, june 2011.
- [87] J. Lu, H. Jia, X. Wang, K. Padmanabhan, W. Hurley, and Z. Shen, “Modeling, design, and characterization of multiturn bondwire inductors with ferrite epoxy glob cores for power supply system-on-chip or system-in-package applications,” *Power Electronics, IEEE Transactions on*, vol. 25, no. 8, pp. 2010–2017, aug. 2010.
- [88] J. Lu, H. Jia, A. Arias, X. Gong, and Z. J. Shen, “On-chip bondwire magnetics with ferrite-epoxy glob coating for power systems on chip,” *International Journal of Power Management Electronics*, vol. 2008, pp. 1–9, 2008.
- [89] J. Lu, H. Jia, A. Arias, X. Gong, and Z. Shen, “On-chip bondwire transformers for power SoC applications,” in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, feb. 2008, pp. 199–204.
- [90] E. Cho, S. Lee, J. Lee, and S. Nam, “A High-Efficient Transformer Using Bond Wires for Si RF IC,” *IEICE Transactions on Electronics*, vol. 93, pp. 140–141, 2010.
- [91] A. Moazen-zadeh, N. Spengler, and U. Wallrabe, “High-performance, 3d-microtransformers on multilayered magnetic cores,” in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2013, pp. 287–290.
- [92] K.-Y. Lin and M. El-Gamal, “Performance and modeling of bonding wire transformers in a package for RF IC’s,” in *Microelectronics, 2007. ICM 2007. International Conference on*, dec. 2007, pp. 347–350.
- [93] M. Raimann, A. Peter, D. Mager, U. Wallrabe, and J. Korvink, “Micro-transformer based isolated signal and power transmission,” *IEEE Transactions on Magnetics*, vol. 27, no. 5, 2012.
- [94] “private communication,” 2010.
- [95] “private communication,” 2011.
- [96] C. Cepnik and U. Wallrabe, “A micro energy harvester with 3D wire bonded microcoils,” in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2011, pp. 665–668.
- [97] K. Kratt, V. Badilita, T. Burger, J. Korvink, and U. Wallrabe, “A fully MEMS-compatible process for 3D high aspect ratio micro coils obtained with an automatic wire bonder,” *IOP Journal of Micromechanics and Microengineering (JMM)*, vol. 20, no. 1, p. 015021, 2010.
- [98] R. Willmot, D. Kim, and D. Peroulis, “High-efficiency wire bond antennas for on-chip radios,” in *Microwave Symposium Digest, 2009. MTT ’09. IEEE MTT-S International*, june 2009, pp. 1561–1564.

- [99] D. Kim, R. Willmot, and D. Peroulis, "A high-efficiency low-cost wire-bond loop antenna for CMOS wafers," in *Antennas and Propagation Society International Symposium, 2009. APSURSI '09. IEEE*, june 2009, pp. 1–4.
- [100] N. Varanasi, B. Jung, and D. Peroulis, "On-chip bond-wire antennas on CMOS-grade silicon substrates," in *Antennas and Propagation Society International Symposium, 2008. AP-S 2008. IEEE*, july 2008, pp. 1–4.
- [101] R. Willmot, D. Kim, and D. Peroulis, "A yagi uda array of high-efficiency wire-bond antennas for on-chip radio applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 12, pp. 3315–3321, dec. 2009.
- [102] H.-T. Wu, M. Tekle, C. Nallani, N. Zhang, and K. Kenneth, "Bond wire antenna/feed for operation near 60 GHz," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 12, pp. 2966–2972, dec. 2009.
- [103] W.-H. Chen, S. Joo, S. Sayilir, R. Willmot, T.-Y. Choi, D. Kim, J. Lu, D. Peroulis, and B. Jung, "A 6-gb/s wireless inter-chip data link using 43-ghz transceivers and bond-wire antennas," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 10, pp. 2711–2721, Oct. 2009.
- [104] I. Ndip, A. Öz, C. Tschoban, S. Guttowski, H. Reichl, K. D. Lang, and H. Henke, "Modelling the shape, length and radiation characteristics of bond wire antennas," *Microwaves, Antennas Propagation, IET*, vol. 6, no. 10, pp. 1187–1194, 2012.
- [105] I. Ndip, S. Guttowski, H. Reichl, and K.-d. Lang, "Systematic design and optimization of bond wire antennas using the m3-approach," in *Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), 2012 IEEE*, Dec. 2012, pp. 85–88.
- [106] S.-J. Chen, C.-Y. Lee, and E. S. Kim, "Integration of tunable capacitors and bonded-wires for contactless RF switch and tunable filter," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2009, pp. 545–548.
- [107] Y.-K. Lim and H.-Y. Lee, "Novel slow-wave structure using bond-wire for miniaturizing microwave devices," in *Microwave Conference, 2007. APMC 2007. Asia-Pacific*, dec. 2007, pp. 1–4.
- [108] S. Harkness, J. Meirhofer, and B. LaMeres, "Controlled impedance chip-to-chip interconnect using coplanar wire bond structures," in *Electrical Performance of Electronic Packaging, 2008 IEEE-EPEP*, oct. 2008, pp. 267–270.
- [109] J.-B. Yan and R. Murch, "Semi-helical bondwire on-chip antenna," in *Antennas and Propagation Society International Symposium, 2008. AP-S 2008. IEEE*, july 2008, pp. 1–4.
- [110] A. Ahmed, "Active-inductor-matched 6-GHZ duplexer-less LNA/PA design incorporated with a bondwire-antenna," *Microwave and Optical Technology Letters*, vol. 53, no. 4, pp. 761–766, 2011. [Online]. Available: <http://dx.doi.org/10.1002/mop.25823>
- [111] T. W. Kim and S. Jung, "A multi-antenna 60GHz CMOS transmitter using wire-bond antenna for high output power," in *Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on*, aug. 2011, pp. 1–4.
- [112] Y. Tsutsumi, T. Ito, S. Obayashi, H. Shoki, and T. Morooka, "Bonding wire loop antenna built into standard BGA package for 60 GHz short-range wireless communication," in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, june 2011, pp. 1–4.
- [113] H. Khatri, P. Gudem, and L. Larson, "Integrated RF interference suppression filter design using bond-wire inductors," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, no. 5, pp. 1024–1034, may 2008.
- [114] J. Zhou, G. Zhang, and M. Lancaster, "Passive microwave filter tuning using bond wires," *Microwaves, Antennas Propagation, IET*, vol. 1, no. 3, pp. 567–571, june 2007.
- [115] E. Marquez-Segura, F. P. Casares-Miranda, P. Otero, C. Camacho-Penalosa, and J. E. Page, "Analytical model of the wire-bonded interdigital capacitor," *Microwave Theory and Techniques IEEE Transactions on*, vol. 54, no. 2, pp. 748–754, 2006.

- [116] S.-J. Chen, C.-Y. Lee, and E. S. Kim, "Integration of piezoelectric tunable capacitors and bonded-wire inductors for contactless RF switch and tunable filter," *Sensors and Actuators A: Physical*, vol. 165, no. 1, pp. 73 – 78, 2011, [jce:title;Transducers 2009;ce:title; \[Online\]. Available: <http://www.sciencedirect.com/science/article/pii/S0924424709005524>](http://www.sciencedirect.com/science/article/pii/S0924424709005524)
- [117] I. Shohjia, T. Sakuraib, and S. Arai, "High-Speed Bonding of Resin-Coated Cu Wire and Sn Electrode with Ultrasonic Bonding for High-Frequency Chip Coil," *Key Engineering Materials*, vol. 297-300, pp. 2819–2824, November 2005.
- [118] T. Stieglitz, H. Beutel, and J. U. Meyer, "Microflex - a new assembling technique for interconnects," *Journal of Intelligent Material Systems and Structures*, vol. 11, no. 6, pp. 417–425, 2000.
- [119] W. Haberer, M. Schuttler, and B. H., "Method for producing an electrical and/or mechanical connection between flexible thin-film substrates," International Patent PCT/EP2001/008268, 2002.
- [120] M. Schuettler, C. Henle, J. S. Ordonez, W. Meier, T. Guenther, and T. Stieglitz, "Interconnection technologies for laser-patterned electrode arrays," in *Engineering in Medicine and Biology Society, 2008. EMBS 2008. 30th Annual International Conference of the IEEE*, aug. 2008, pp. 3212 –3215.
- [121] N. Jackson and J. Muthuswamy, "Flexible chip-scale package and interconnect for implantable MEMS movable microelectrodes for the brain," *IEEE/ASME Journal of Microelectromechanical Systems (JMEMS)*, vol. 18, no. 2, pp. 396 –404, april 2009.
- [122] P. Rekha, M. Crain, and K. Walsh, "Maskless shaping of gold stud bumps as high aspect ratio microstructures," *Microelectronic Engineering*, vol. 88, no. 1, pp. 135–139, 2011.
- [123] R. Yabuki and N. Tea, "Stacked contact bump," US Patent 7,378,734 B2, 2006.
- [124] W. Tonomura, K. Shimizu, and S. Konishi, "Spatially arranged microelectrodes using wire bonding technology for spatially distributed chemical information acquisition," in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2009, pp. 741 –744.
- [125] Y.-T. Liao, W. Biederman, and B. Otis, "A fully integrated CMOS accelerometer using bondwire inertial sensing," *Sensors Journal, IEEE*, vol. 11, no. 1, pp. 114 –122, jan. 2011.
- [126] M. Sadeghi, R. L. Peterson, K. Peterson, R. Fearing, and K. Najafi, "Air-flow sensing on autonomous mobile platforms using micro-scale hot-wire anemometry," in *Army Sciences Conference*, December 2010.
- [127] Y.-T. Liao, W. Biederman, and B. Otis, "A CMOS accelerometer using bondwire inertial sensing," in *VLSI Circuits, 2009 Symposium on*, june 2009, pp. 64 –65.
- [128] Y.-T. Liao, J. Shi, and B. Otis, "A CMOS wireless two-axis digital accelerometer using bondwire inertial sensing," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2011, pp. 68 –71.
- [129] S. Schröder, A. Nafari, K. Persson, E. Westby, A. C. Fischer, G. Stemme, F. Niklaus, and S. Haasl, "Stress-minimized packaging of inertial sensors using wire bonding," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2013, accepted.
- [130] H. Seppanen, S. Kiprich, R. Kurppa, P. Janhunen, and E. HÄggstrÅm, "Wire-to-wire bonding of um-diameter aluminum wires for the electric solar wind sail," *Microelectronic Engineering*, vol. 88, no. 11, pp. 3267 – 3269, 2011. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0167931711006162>
- [131] A. C. Fischer, M. Grange, N. Roxhed, R. Weerasekera, D. Pamunuwa, G. Stemme, and F. Niklaus, "Wire-bonded through-silicon vias with low capacitive substrate coupling," *IOP Journal of Micromechanics and Microengineering (JMM)*, vol. 21, no. 8, p. 085035, August 2011.
- [132] S. Schröder, A. C. Fischer, G. Stemme, and F. Niklaus, "Very high aspect ratio through silicon vias (tsv) using wire bonding," in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2013, accepted.

- [133] A. G. Wood, “Stacked semiconductor components with through wire interconnects (twi),” US Patent US 2008/0042247 A1, 2008.
- [134] D. R. Hembree, “Method and system for fabricating semiconductor components with through-wire-interconnects,” US Patent US2006/0228825 A1, 2006.
- [135] —, “Semiconductor components and systems having encapsulated through-wire-interconnects (TWI) and wafer level methods of fabrication,” US Patent US2007/0246819 A1, 2007.
- [136] —, “Semiconductor components and systems having encapsulated through-wire-interconnects (TWI),” US Patent US 7,659,612 B2, 2010.
- [137] R. T. Iwata, “Semiconductor chip device having through-silicon-via (TSV) and its fabrication method,” US Patent US2009/0127667 A1, 2009.
- [138] I. Y. Khandros, “Contact structure device for interconnections, interposer, semiconductor assembly and package using the same method,” US Patent 5,900,783, 1999.
- [139] M. Antelius, A. C. Fischer, F. Niklaus, G. Stemme, and N. Roxhed, “Hermetic integration of liquids using high-speed stud bump bonding for cavity sealing at the wafer level,” *IOP Journal of Micromechanics and Microengineering (JMM)*, vol. 22, no. 4, p. 045021, Apr. 2012. [Online]. Available: <http://dx.doi.org/10.1088/0960-1317/22/4/045021>
- [140] —, “Hermetic integration of liquids in MEMS by room temperature, high-speed plugging of liquid-filled cavities at wafer level,” in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2011, pp. 356–359.
- [141] M. Antelius, A. C. Fischer, N. Roxhed, G. Stemme, and F. Niklaus, “Room-temperature wafer-level vacuum sealing by compression of high-speed wire bonded gold bumps,” in *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, june 2011, pp. 1360–1363.
- [142] J. Fendrock and L. Hong, “Parallel-gap welding to very-thin metallization for high temperature microelectronic interconnects,” *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 13, no. 2, pp. 376–382, jun 1990.
- [143] K. A. Olver, “A new technique for wirebonding using indium spheres,” Adelphi, MD : Army Research Laboratory, Tech. Rep., 2010.
- [144] R. Lyn and W. Crockett, “Assembly using X-Wire insulated bonding wire technology,” in *Semicon Singapore 2007*, 2007.
- [145] R. Cauchois, M. Saadaoui, J. Legeleux, T. Malia, B. Dubois-Bonvalot, K. Inal, and J.-C. Fidalgo, “Wire-bonding on inkjet-printed silver pads reinforced by electroless plating for chip on flexible board packages,” in *Electronic System-Integration Technology Conference (ESTC), 2010 3rd*, sept. 2010, pp. 1–6.
- [146] D. Sameoto, S. W. Lee, and M. Parameswaran, “Electrical interconnection through optimized wirebonding onto su-8 structures and actuators,” *IOP Journal of Micromechanics and Microengineering (JMM)*, vol. 18, no. 7, p. 075023, 2008.
- [147] A. J. Zakariya, T. Liu, and R. R. Panepucci, “Experimental demonstration of a wafer-level flexible probe for optical waveguide testing,” *Opt. Express*, vol. 15, no. 24, pp. 16 210–16 215, Nov 2007. [Online]. Available: <http://www.opticsexpress.org/abstract.cfm?URI=oe-15-24-16210>
- [148] Fraunhofer, “Annual report 09/10,” Fraunhofer IZM, Germany, Tech. Rep., 2010.
- [149] C. Clark, J. Robinson, and R. Clayton, “Flexible polymer waveguides for optical wire bonds,” *Journal of Optics A: Pure and Applied Optics*, vol. 4, no. 6, p. S224, 2002. [Online]. Available: <http://stacks.iop.org/1464-4258/4/i=6/a=357>
- [150] R. R. Panepucci, A. J. Zackariya, and T. Liu, “Polymeric optical wire-bonding for planar lightwave circuit packaging,” in *Integrated Photonics and Nanophotonics Research and Applications*. Optical Society of America, 2008, p. ITuC2. [Online]. Available: <http://www.opticsinfobase.org/abstract.cfm?URI=IPNRA-2008-ITuC2>

- [151] S. Schmitz, H. Oppermann, H. Schröder, and H. Reichl, “New ways - wirebonding of optical polymer fibers,” in *Mikrosystemtechnik Kongress*, Berlin, Germany, October 2009.
- [152] N. Lindenmann, G. Balthasar, D. Hillerkuss, R. Schmogrow, M. Jordan, J. Leuthold, W. Freude, and C. Koos, “Photonic wire bonding: a novel concept for chip-scale interconnects,” *Opt. Express*, vol. 20, no. 16, pp. 17 667–17 677, Jul 2012.
- [153] A. Hirshberg and D. Elata, “Direct wire-bonding to silicon devices without the use of metallic layers,” *ASME Conference Proceedings*, vol. 2008, no. 48388, pp. 303–306, 2008.
- [154] —, “Direct wire-bonding of silicon devices without metal pads,” in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2009, pp. 757–760.
- [155] A. C. Fischer, H. Gradin, S. Schröder, S. Braun, G. Stemme, W. van der Wijngaart, and F. Niklaus, “Wire-bonder-assisted integration of non-bondable SMA wires into MEMS substrates,” *IOP Journal of Micromechanics and Microengineering (JMM)*, vol. 22, no. 5, p. 055025, May 2012. [Online]. Available: <http://stacks.iop.org/0960-1317/22/i=5/a=055025>
- [156] A. C. Fischer, H. Gradin, S. Braun, S. Schröder, G. Stemme, and F. Niklaus, “Wafer-level integration of niti shape memory alloy wires for the fabrication of microactuators using standard wire bonding technology,” in *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, jan. 2011, pp. 348–351.
- [157] H. Gradin, “Heterogeneous integration of shape memory alloys for high-performance microvalves,” Ph.D. dissertation, KTH, Microsystem Technology, 2012.
- [158] M. Antelius, A. C. Fischer, N. Roxhed, G. Stemme, and F. Niklaus, “Wafer-level vacuum sealing by coining of wire bonded gold bumps,” *IEEE/ASME Journal of Microelectromechanical Systems (JMEMS)*, 2013, accepted.
- [159] M. Lapisa, G. Stemme, and F. Niklaus, “Wafer-level heterogeneous integration for MOEMS, MEMS, and NEMS,” *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, no. 3, pp. 629–644, may-june 2011.