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Unconventional Transport through Graphene on $SrTiO_3$: A Plausible Effect of $SrTiO_3$ Phase-Transitions

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High-k dielectric oxides are supposedly ideal gate-materials for ultra-high doping in graphene and other 2D-crystals. Here, we report a temperature-dependent electronic transport study on chemical vapor deposited-graphene gated with $SrTiO_3$ (STO) thin film substrate. At carrier densities away from charge neutrality point the temperature-dependent resistivity of our graphene samples on both STO and SiO_2/Si substrates show metallic behavior with contributions from Coulomb scattering and flexural phonons attributable to the presence of characteristic quasi-periodic nano-ripple arrays. Significantly, for graphene samples on STO substrates we observe an anomalous 'slope-break' in the temperature-dependent resistivity for T = 50 to 100 K accompanied by a decrease in mobility above 30 K. Furthermore, we observe an unusual decrease in the gate-induced doping-rate at low temperatures, despite an increase in dielectric constant of the substrate. We believe that a complex mechanism is at play as a consequence of the structural phase transition of the underlying substrate showing an anomalous transport behavior in graphene on STO. The anomalies are discussed in the context of Coulomb as well as phonon scattering.

Graphene[1], a 2-dimensional (2D) sheet of carbon atoms in a honeycomb lattice, is poised to transform the electronic industry thus promising a unique platform for many novel device applications, such as, nanoelectronics, optoelectronics, and flexible transparent devices[2–4]. As a single-atom-thick layer, the transport property of graphene is highly influenced by the supporting substrate[1,5,6]. SiO_2/Si, a conventional substrate that provides an excellent optical contrast, has been extensively used to understand the charge transport phenomena in graphene in terms of momentum relaxation from charge impurities and interfacial phonons. Wafer-scale growth of graphene by chemical vapor deposition (CVD) methods[7] has made it increasingly feasible to explore a variety of novel functional substrates for engineering specific applications by means of tuning substrate-induced screening and by inducing strain[5,8–11].

Replacement of SiO_2/Si substrate by hexagonal boron nitride improves the carrier mobility by several orders of magnitude while limiting the maximum carrier density ($\sim 3 \times 10^{12}$ cm^{-2}). Interestingly, at ultra-high doping the possibility of superconductivity in graphene has been theoretically predicted[12,13] while experimentally the optimal doping has still not been achieved to explore such phenomena. In the process, introduction of substrates with high dielectric constant[6,8,9,14] or gating with polymer electrolyte[15] has increased the carrier density by one-to-two orders in magnitude with fascinating electronic transport that can be attributed to screening as well as many-body interactions. The inability to reach expected high carrier densities for graphene gated with high-k dielectrics remains a puzzle-[6,8,9,16,17] and points to the need to understand substrate-graphene interaction in detail beyond the expected crucial role of the electron-phonon scattering at the interface[17]. Non-linear temperature-dependence of resistance particularly at higher temperatures have been variously attributed to scattering from adatoms or defects, charge impurities, surface optical (SO) phonons of the underlying SiO_2/Si substrate and to the out-of-

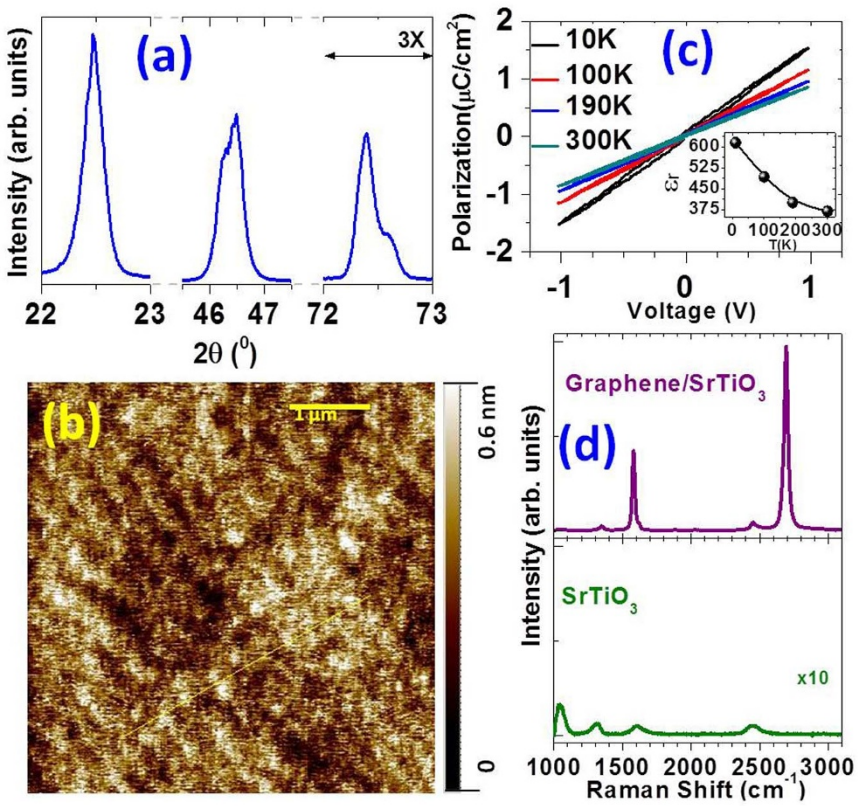

Figure 1 | (a) XRD data of $SrTiO_3$/Nb:$SrTiO_3$ thin film substrate, (b) Typical morphology (roughness) of the thin film substrates as measured by Atomic Force Microscopy, (c) The linear voltage-dependent polarization (P-Vg) of the thin films at a few temperatures measuring the dielectric constant (ε_r), shown in the inset, (d) Raman signatures of graphene on $SrTiO_3$ (STO) thin film and the STO substrate.

plane flexural phonons of graphene[17]. However, the strength of the coupling between SO phonons or the flexural modes and graphene electrons remains not well understood.

A high-k dielectric substrate (e.g. Al_2O_3, HfO_2, $Pb_{1-x}Zr_xTiO_3$, and STO to name a few) is an ideal platform to investigate several aspects relating to the electronic transport in graphene at ultra-high carrier densities. STO has a dielectric constant of ~300 at room temperature where softening of a low-energy phonon with decreasing temperature brings the material to ferroelectric instability thus dramatically increasing the dielectric constant to about 10^4 (in bulk) at very low temperatures which makes it a promising candidate as gate-dielectric in order to achieve ultra-high carrier densities. Surprisingly, the reported maximum carrier densities achieved in graphene field-effect transistor (FET) gated with STO is $\sim 1 \times 10^{13}$ cm^{-2}.[6] Similarly, graphene devices gated with the various high-k dielectrics are also limited to a range of 10^{12} to 10^{13} cm^{-2}.[9,18–22] Though it is believed to be the interfacial adsorbates and defect states that play an important role, the microscopic picture and the mechanism behind is still a matter of debate. In the present work we would like to address and bring out the microscopic details at the interface that may be held responsible for such limitations. We have performed temperature-dependent transport studies on STO-gated graphene FETs and observed an unusual slope-break in resistivity between ~ 50 to 100 K, in concomitant with a decline in the carrier injection at lower temperatures. We propose that in addition to the impurity scattering, the structural phase transitions of STO significantly change phonon density of states as well as the interface between graphene and the substrate which are expected to have a strong effect on doping of graphene as well as the transport properties.

Results

PLD grown thin films of STO on Nb:STO were examined by x-ray diffraction (XRD), atomic force microscopy (AFM) and dielectric measurements. As shown in Figure 1a, the XRD data suggest an epitaxial growth of the thin films while the AFM image in Figure 1b shows the typical roughness (<1 nm). The voltage-dependent polarization (P-Vg curve) of the thin films was measured at various temperatures as shown in Figure 1c for four different temperatures. The dielectric constant (ε_r) was extracted from the slope of P-Vg data: at room temperature $\varepsilon_r \sim 300$ and rises to ~600 by 10 K. However, the dielectric constant measured using graphene as an electrode is found to be lower than that actually measured using Au-electrode (see Figures S1 and S2) which may be due to contribution from quantum capacitance of graphene[23,24] or charge traps/impurities as well as surface dipoles at the graphene-STO interface[25]. The Raman spectrum of graphene on STO, shown in the top panel of Figure 1d, has the characteristic G and 2D bands with very weak D-band merged with weak signatures of STO Raman phonons, shown in the bottom panel of Figure 1d. The Raman signature of graphene, therefore, suggests the CVD-graphene to be a single layer with minimal defects.

A schematic of the Hall-bar geometry of graphene FET is depicted in Figure 2a (an SEM image of which is shown in the inset of Figure 2c). The typical gate dependence of graphene resistivity (at room temperature) is shown in Figure 2b. A carrier density of about $n = I(\Delta B/\Delta V_H)/e = 9 \times 10^{12}$ cm^{-2} can be achieved at nearly all temperatures, (where I is the current, B is the applied magnetic field, V_H is the Hall voltage and e is the electronic charge) while at low temperatures (below 50 K) it reaches to about 12×10^{12} cm^{-2}. However, surprisingly the carrier density saturates at this value ($\sim 12 \times 10^{12}$ cm^{-2}) at a gate-voltage of ~5 V (i.e. an electric field of ~150 $kVcm^{-1}$) and becomes unresponsive to any higher applied gate-voltage (as shown in Figure 2c). It is to be noted that a similar observation may be made from ferroelectric $Pb(ZrTi)O_3$ gated[9] as well as bulk-STO gated[6] graphene devices where the reported maximum carrier density is close to what is observed in our STO thin film

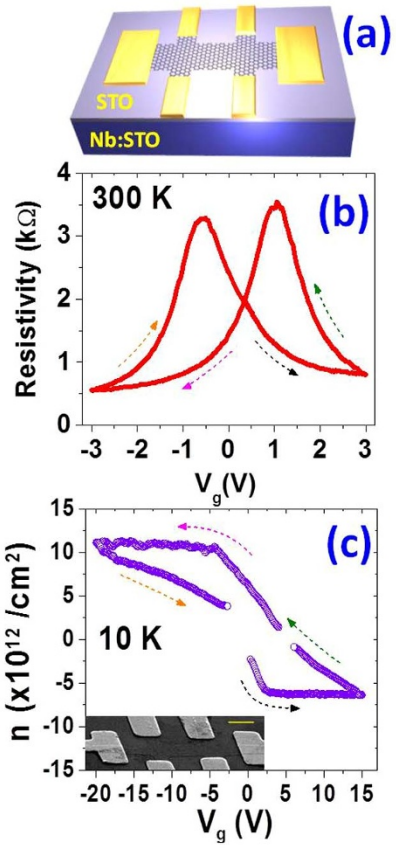

Figure 2 | (a) A schematic of the graphene FET on $SrTiO_3$/Nb:$SrTiO_3$ in Hall-bar geometry, (b) Gate-voltage-dependent resistivity of graphene on $SrTiO_3$ at 300 K, (c) Gate-voltage-dependent carrier density at 10 K. Inset shows an SEM image of a typical graphene FET on $SrTiO_3$. The (yellow colored) bar indicates a length-scale of 1 micron.

gated devices (Figure 2c). Such saturation may seem unexpected since the dielectric constant of STO (and also in our STO thin film) increases with decreasing temperature. Possible explanations for this process are discussed later. Temperature-dependent resistivity of STO gated graphene has been measured on six devices fabricated on three different substrates. Data from two different devices (samples), showing distinct characteristics are shown in Figure 3 over a temperature range of ~2 K to 300 K at various carrier densities. The resistivity at all carrier densities increases monotonically with increasing temperature in confirmation with the metallic nature of doped graphene. However, an unusual response that appears as a 'slope-break' in the temperature range of 50–100 K can be clearly noticed which is absent for devices gated with SiO_2/Si, as shown in Figure 3c (an AFM image of CVD graphene on SiO_2/Si is shown in Figure S3). In another representation, this unusual behavior may also be noted in the temperature-dependent Temperature-Coefficient-of-Resistivity (TCR), defined as: $TCR = 1/\rho(d\rho/dT)$. The normalized TCR (i.e., TCR/TCR_{Max}) as a function of temperature also shows a broad peak in the same temperature range (as shown in Figure S4) corroborating the 'slope-break' in resistivity.

These anomalies in the resistivity as well as TCR data may be associated with the structural phase transition of the underlying substrate, STO/Nb:STO, near 105 K and another at 55 K. At temperatures below ~ 50 K, the resistivity in our STO gated graphene devices is carrier dependent and shows metallic behavior down to the lowest temperature while in SiO_2 gated device it shows an upturn undergoing metal to insulator transition owing to activation of Coulomb impurities – viz. electron-hole puddles[26]. Figure 4 shows the temperature dependence of mobility at a few carrier (electron) densities (2×10^{12}, 3×10^{12}, and 4×10^{12}/cm^2). It can be seen that the mobility remains nearly independent of temperature from 2 to ~ 30 K and decreases with increasing temperature until ~ 150 K above which it again becomes nearly temperature-independent. We believe that the temperature dependence of mobility may be related to screening, structural phase transition and the SO phonons of STO.

The carrier density in graphene FET can be tuned by sweeping the gate-voltage which, however, depends on the dielectric constant of

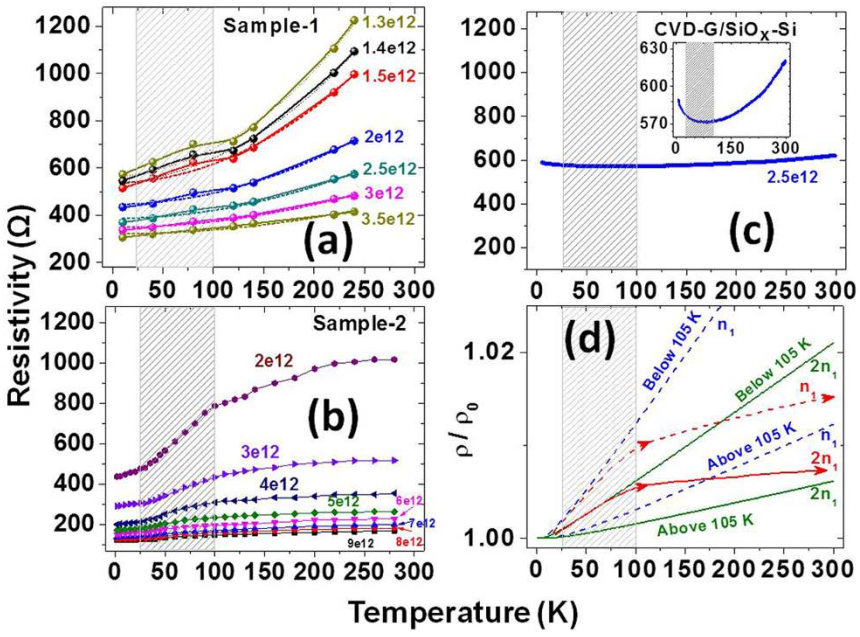

Figure 3 | Temperature-dependent resistivity (ρ) of CVD-graphene supported on STO (Sample-1 in (a) and Sample-2 in (b)) at a few electron densities and on SiO_2/Si substrate (c) at an electron density of 2.5×10^{12}/cm^2. The dashed lines in (a) represent the typical T^2-dependence. A clear 'slope-change' can be seen in STO-gated 'ρ vs T' data deviating from the T^2-dependence in the 50-100 K range, as shown by shaded-region, as also seen in the simulated data for two different carrier densities (n_1 by dashed lines and $2n_1$by solid lines) in (d), whereas no such 'slope-change' is observed in SiO_2/Si-gated device (see inset) in the temperature range.

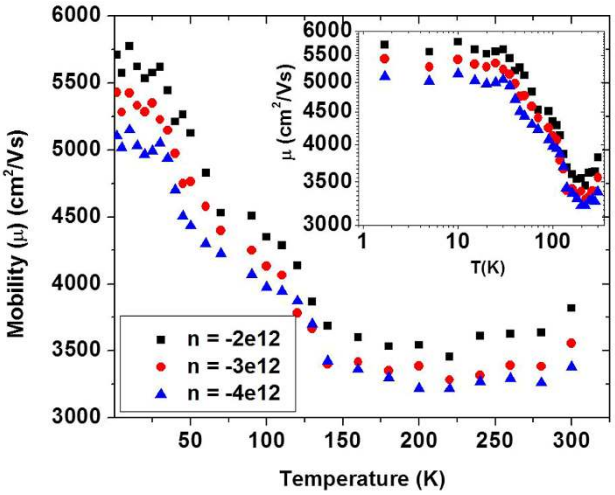

Figure 4 | Mobility as a function of temperature at a few typical carrier densities showing a nearly temperature-independent behavior in between ~105 K to 300 K but increases with lowering temperature. Inset shows the data in log-log scale.

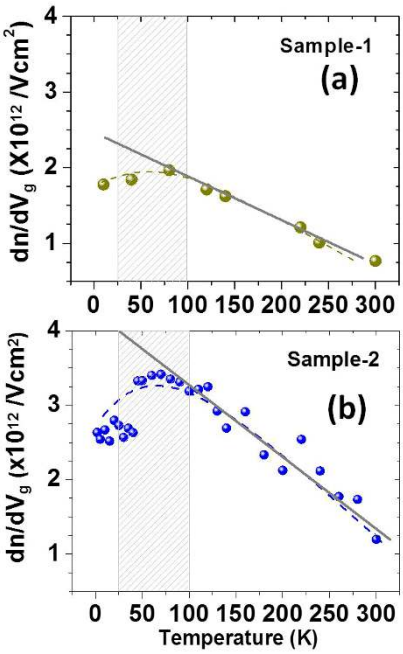

Figure 5 | The rate of carrier density injection (dn/dVg) as a function of temperature for the two different samples (1 in (a) and 2 in (b), respectively). The solid circles are experimental data while the dashed lines are guide to eye. The solid lines represent the expected dn/dV_g in proportion to the temperature-dependent dielectric constant of $SrTiO_3$ thin film.

the gate-dielectric. Unlike the case in conventional SiO_2/Si substrate where the dielectric constant (ε_r) is almost temperature-independent, the 'ε_r' of our STO thin film increases with decreasing temperature, even down to ~ 10 K (Figure 1c inset and Figure S2). This, in principle, should imply that the rate of carrier injection (i.e. $\alpha = dn/dV_g$) on to graphene should increase with decreasing temperature, down to the lowest temperature. The temperature dependence of the doping-rate (i.e. α vs T), shown in Figure 5a & 5b (for sample-1 & 2), shows an expected overlap with the 'ε_r vs T'-trend at higher temperatures but surprisingly reveals a decline at low temperatures with a peak in the temperature range of 50–100 K. The observed behavior of resistivity (Figure 3), mobility (Figure 4) and the doping rate (α) (Figure 5) as a function of temperature suggest a possible disruption of the interface between graphene and STO in the temperature range of 50–100 K which is driven by the structural phase transition of STO at ~105 K.

Discussion

The behavior of carrier transport in graphene has been variously attributed to resonant scatterers, long-range Coulomb impurities, acoustic and flexural phonons of graphene as well as the SO phonons of the underlying substrate. Unlike graphene on SiO_2/Si, the transport through graphene on STO in our devices show unique characteristic features, such as, (a) hysteresis and saturation in carrier density (Figure 2), (b) slope-break in 'ρ vs T' in the temperature range of 50–100 K for all carrier densities (Figure 3), (c) drop in mobility by ~40% at temperatures above ~30 K (Figure 4), and (d) reduction in the rate-of-carrier-doping (α=dn/dVg) at temperatures below ~100 K (Figure 5). These features suggest that a model based on any single scattering mechanism cannot fully explain the transport data. We will discuss the role of each of the mechanisms below to understand the transport through graphene on STO.

Resonant and Coulomb impurity scattering. In the light of the findings by Couto et al.[6] and the model later proposed by Das Sarma et al.[27], both resonant and Coulomb impurity scattering mechanisms are at play in the transport through graphene on STO at temperatures below 50 K down to 250 mK. The resonant scattering mechanism alone cannot explain the transport at carrier densities near charge neutrality point. Therefore, at carrier densities close to charge neutrality point, Coulomb impurity scattering dominates. Couto et al. observed a sublinear density-dependent conductivity which remains temperature-independent thus attributing to a combination of resonant and Coulomb impurity scattering. Our transport data as well reveal a sublinear density-dependent conductivity (see Figure S5) thus implying the role played by the resonant and Coulomb impurity scatterers. Furthermore, we observe a drop in mobility with increasing temperature which may partly be attributed to screening of the Coulomb scattering under the influence of the temperature-dependent dielectric constant of STO. However, surprisingly, our experimental data reveal a clear temperature-dependent resistivity right from the lowest temperature (~2 K). One would expect such a behavior in STO-gated graphene devices, as also pointed by Couto et al., as STO has very low energy (3–5 meV) SO phonons. We, therefore, believe that in addition to the short-ranged and long-ranged scatterers, the SO phonons play crucial role in our transport data at high carrier densities, away from neutrality point.

Phonon scattering. In conventional SiO_2 gated devices, the resistivity of mechanically exfoliated graphene shows linear-temperature-dependence with a universal slope of 0.1 ΩK^{-1} below ~150 K, which is independent of carrier density[17]. Such temperature dependence arises from scattering from acoustic phonon of graphene at low carrier densities and near charge neutrality point contributing a resistance change ($\Delta\rho$) of up to ~30 Ω from ~4 K to 300 K. However, we do not see such a universal behavior in our devices suggesting an insignificant contribution from acoustic phonon scattering and indicating a clear role of flexural phonons and/or SO phonons.

At room temperature, STO is in cubic phase having SO phonons[28] at 57 and 92 meV. However, STO undergoes a structural phase transition to tetragonal phase below ~105 K where low energy optical phonons are also excited due to the structural transition. The optical phonons of STO in low temperature phase as obtained from infrared and Raman spectroscopic studies[29] are at ~5 and 20 meV in addition to the high energy phonons observed at room temperature. Therefore, at low temperatures it may be anticipated

that the charge carriers in graphene will be scattered by the low energy optical phonons of STO as well as the charge impurities leading to an increase in resistivity right above ~10 K varying as $\rho \propto \sum_i \left[n^{-\alpha_i} g_i \Big/ \left(e^{\omega_i / k_B T} - 1 \right) \right]$ where g_i is the coupling strength with the phonon ω_i, n is the carrier density and $\alpha_i \cong 1$ is the fitting parameter[17]. The phonon density of state undergoes a change as STO undergoes a structural phase transition from low temperature tetragonal to high temperature cubic phase at ~105 K. The lowest energy phonon in tetragonal phase is ~5 meV while that in cubic phase is ~20 meV. The 'slope-break' observed in our 'ρ vs T' in between 50–100 K as shown in Figure 3 may be, therefore, attributed to the change in distribution of phonon density of states across the structural phase transition of STO. Furthermore, the change in resistivity over the entire temperature range (2–300 K) and the 'slope-break' near 105 K also show carrier density dependence, i.e., the resistivity change and the 'slope-break' become higher for lower carrier densities and lower for higher carrier densities thus indicating an effect of charge impurity scattering in addition to the SO phonon scattering. We have simulated the resistivity as a function of temperature considering the dependence on carrier density and optical phonons of STO (shown in Figure 3d) as stated above: $\rho \propto \sum_i \left[n^{-\alpha_i} g_i \Big/ \left(e^{\omega_i / k_B T} - 1 \right) \right]$. The dashed (blue) lines correspond to the temperature dependence of resistivity below and above 105 K at a carrier density of n_1 while at double the carrier density ($2n_1$) the resistivity behaviors are represented by solid (green) lines. The net resistivity across 105 K (STO phase transition) is represented by the dashed (red)/solid (red) arrows. A similar 'slope-break' in 'ρ vs T' can be seen in our simulation across the structural phase transition of STO (105 K) (for further details see supplementary information). The simulated resistivity and the 'slope-break' are found to be higher for low carrier density (n_1) and lower for high carrier density ($2n_1$), manifesting the effect of impurity and SO phonon scattering[17]. Here we have assumed that below 105 K the dominant phonons[29] are from 2–20 meV while above 105 K they are from 20–100 meV. Scattering from the optical phonons will suppress the carrier mobility as observed in exfoliated graphene on SiO_2-gated devices[17]. We have observed a decrease in the carrier mobility as a function of temperature as shown in Figure 4 above ~30 K, thus further indicating SO phonon scattering being at play in addition to the impurity scattering. Furthermore, we observe a sub-linear carrier density-dependent conductivity at both high (300 K) and low (10 K) temperatures, as shown in Figure S5, suggesting that impurity scattering as well as SO phonon scattering play crucial role in determining the transport through graphene on STO in our devices.

Reduction of doping-rate at low temperatures. As shown in Figure 1c (and also in Figure S2), the dielectric constant (ε_r) of our STO thin film increases with decreasing temperature, down to 10 K. It is, therefore, expected that the doping-rate ($\alpha = dn/dV_g$) will increase with lowering temperature, even down to the lowest temperatures. Surprisingly, we observe that the doping-rate declines as the temperature decreases below ~105 K. The decline in doping-rate cannot be attributed to Coulomb impurities as we do not observe any unusual change in impurity concentration with decreasing temperatures (Figure S6). Furthermore, it is to be noted that the 'ε_r' of STO is known to undergo a small decrease or saturation at low temperatures under high electric fields arising from electrostriction caused by alignment/rotation of tetragonal domains leading to a small decrease or saturation of total available charge for injection[22,30]. However, we observe a similar 'α vs T' at various electric fields ranging from ~0 $kVcm^{-1}$ to 150 $kVcm^{-1}$ thus ruling out any role of the electric field-induced decrease in dielectric constant (see Figure S7 in supplementary information). The origin of this decline, therefore, is not very clear at present. However, the drop in doping-rate may be due to a possible disruption at the graphene-substrate interface. In a recent experimental report[31] on x-ray reflectivity, x-ray diffraction and atomic force microscopy studies of STO single crystal presents the observation of surface-rumpling (surface becomes wavy) of more-than-micron length scales upon cooling below 105 K which is correlated with the structural phase transition. At the same time, the roughness gradually increases up to about 200% as the temperature decreases well below 105 K which is associated with a severe degradation of the mosaic quality of the substrate-surface. These changes are notably reversible upon heating back to room temperature. It is possible that the unusual behavior of 'α vs T' in our data may arise due to a partial suspension of graphene in nanoscale dimensions owing to an increase in surface roughness at temperatures below STO structural phase transition. Further experimental evidences probing the morphology at the Graphene-STO interface at low temperatures will be necessary to understand the anomalous transport and is beyond the scope of this work.

Furthermore, other important observations are the hysteresis of graphene-resistance (Figure 2b) and carrier density as well as saturation of carrier density (~12×10^{12} cm^{-2}) beyond an applied electric field of ~150 $kVcm^{-1}$, i.e., a gate-voltage of ~5 V (shown in Figure 2c). In high quality SiO_2 on silicon one can observe trapped charge states of the order of ~10^{11} cm^{-2} while on the STO surface this hysteresis translates to a trapped charge state of the order of ~10^{12} cm^{-2}. Therefore, the possible candidates that are likely to contribute to the observed hysteresis are the trapped charge states and surface dipoles[23] of STO. These may pre-screen the field-induced surface polarization change leading to the observed hysteresis in graphene-resistance as well as carrier density (as shown in Figure 2b&c), similar to that seen in carbon nanotube and graphene FETs gated by SiO_2[32] and ferroelectrics[21,33]. However, the interfacial impurities should not lead to the observed 'slope-break' in resistivity. We find that the total charge impurity density at the interface remains nearly independent of temperature (see Figure S6) with minimal change thus suggesting that the structural phase transition of STO does not have any significant effect on the charge traps, STO surface dipoles and the adsorbates at the interface. We, therefore, logically rule out any significant role of these interfacial impurities in the observed 'slope break' in resistivity and the other anomalies (Figures 3, 4, & 5).

Conclusion

In conclusion, we have observed an anomalous 'slope-break' in the temperature-dependent resistivity of CVD-graphene on STO/Nb:STO substrates in the range of 50–100 K, concomitant with a decrease in the gate induced field-effect at lower temperatures. We further observe temperature-dependent mobility dropping at temperatures above ~30 K. These anomalies may be attributed to a change in the SO phonon scattering as a consequence of the structural phase transition of STO at 105 K. In addition, at low temperatures STO surface is known to become significantly rumpled with a gradual increase in roughness[31] which may lead to a partial detachment of graphene from the substrate-surface thus reducing the gate-induced field-effect at low temperatures. However, further experimental evidences will be necessary to understand the morphology change-induced effects in graphene transport. We believe that our experimental observations demonstrate the sensitivity of electronic properties of graphene to structural phase transitions of the underlying substrate and its changing morphology and motivate further experimental and theoretical studies.

Methods

Substrate preparation. Thin films of epitaxial STO (thickness ~300 nm ± 10%) have been grown using Pulsed Laser Deposition (PLD) technique on Nb (0.05%):STO (100) single crystal substrates at an oxygen partial-pressure of 100 mTorr and

substrate-temperature of 700°C at a repetition rate of 5 Hz following a deposition at 1 Hz to improve the surface roughness down to less than 1 nm. Subsequently, the films were annealed at 400°C in oxygen ambience at a pressure of 500 Torr for 1 hour to minimize oxygen vacancy. The films have been characterized using x-ray diffraction and atomic force microscopy followed by measurement of the dielectric constant using a Ferroelectric tester (Radiant Technologies). The films were found to have a dielectric constant of about 300 at room temperature.

Device fabrication and measurement. CVD-graphene grown on Cu substrates has been transferred on to the STO/Nb:STO substrates using the standard wet process where Cu is etched away using ammonium persulfate solution[7]. A two-step electron beam lithography, oxygen-plasma etching and thermal evaporation techniques have been used to fabricate devices in standard Hall-bar geometry. The resistance of the graphene channel has been measured at low frequency (~13 Hz) using SRS-380 lock-in amplifier while the gate-voltage was swept using Keithley-6430 Source Meter. The samples were first cooled down to the lowest temperature without any applied gate voltage and then were gate-swept (from 0 V to +5 V, then from +5 V to −5 V and then return to 0 V, at a step of 0.04 V) at every fixed temperatures from 2 K to 300 K. The maximum voltage during gate-sweep was kept at ± 5 V as otherwise the carrier density saturates at higher gate voltages.

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Author contributions

S.S. & O.K. designed the experiments, prepared the samples and performed the AFM, ferroelectric, Raman and transport measurements. A.S. & A.A. assisted in PLD, XRD & AFM. characterizations. M.J., A.P., C.T. & J.B. assisted in data analysis. J.B. fabricated and measured the SiO_2/Si based device. Insight of the physical mechanism was provided by S.S., O.K., M.J., A.P., T.V. & B.O. The manuscript was prepared by S.S., O.K., M.J., T.V. & B.O. with assistance from B.H. & J.A. All authors reviewed the manuscript.

Additional information

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