Unified Compact Model for Gate All Around FETs- Nanosheets, Nanowires, Multi Bridge Channel MOSFETs

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ABSTRACT

A unified compact model for gate-all-around (GAA) FETs is discussed. This single unified model can accurately model different shapes of GAA FETs. In this work, we present its validation with the reported GAA FETs: stacked GAA nanosheet, stacked nanowire MOSFETs, Multi-bridge-channel MOSFETs and Twin silicon nanowire MOSFETs. This study shows that the BSIM-CMG unified multi-gate MOSFET model is ready for production design of silicon GAA based circuits and technology-product co-development for future technology nodes.

Keywords: GAA, Nanowire, Nanosheet, Compact Model, BSIM-CMG.

1 Introduction

FinFET is in mass production for its capability of scaling below 20nm. Thin silicon Fin surrounded by gate provides a superior channel electrostatics resulting in higher on current (I_{on}) and better subthreshold swing [1, 2]. The same thin body concept was also implemented in planar fully depleted silicon-on-insulator (FDSOI) transistors [3–5]. Both solutions have a very thin body which has solved the problem of sub-surface leakages and poor gate control over the channel [6]. In FinFET, the thin body is obtained by etching the silicon into thin fin shape [7]. In every generation, semiconductor companies have made this fin thinner to have fin thickness (T_{fin}) nearly one-third of the gate lengths L_g [8]. To achieve higher electrical width per device footprint, the fin height is increased in every generation. Below 5nm technology node, it may not be possible to make this fin any thinner and taller because of cleaning and etching issues during manufacturing [9]. In such condition, gate-all-around (GAA) FET may become the preferred choice. Due to its gate all around structure, it offers better electrostatic control which enables continued CMOS device scaling [10].

GAA structures may take different shapes. IRDS-2016 (ITRS 2.0) roadmap shows that vertically stacked nanowires (source at the bottom and drain at the top) will be suitable for logic applications at 5nm technology node and beyond as shown in Figure 1. For past several years, world's leading fabrication companies are working on GAA FETs to meet IRDS prediction for advanced nodes. Samsung was the first who introduced multi-bridge-channel FET in 2003 [11] and twin silicon nanowire with a 10nm diameter in 2006 [12]. Recently IMEC has fabricated vertically stacked horizontal Si nanowire FET at scaled dimensions: 8nm diameter, 45nm lateral pitch, and 20-nm vertical separation [13, 14]. These devices show excellent subthreshold swing at a performance level comparable to FinFET devices. IBM has demonstrated it's horizontally stacked GAA nanosheet structure as replacement of FinFET at 5nm technology node and beyond [15]. Thus, GAA is one of the most promising device for logic applications for future technology nodes. Hence it is important to have a compact model for such GAA structures. Here we have discussed the industry standard BSIM-CMG model [16] and its validation in Section 2 and Section 3, respectively. The conclusions are drawn in Section 4.

Figure 1: Device architecture roadmap for logic device technologies [9]. Different device architectures are Fully-Depleted Silicon-On-Insulator (FDSOI), Lateral Gate-All-Around-Device (LGAA), Vertical GAA (VGAA) and Monolithic-3D (M3D).

2 Unified Compact Model for GAA FETs

From the solution of Poisson's equation, the analytical solution for the double gate (DG) FinFET is known [17] which can be expressed as (1) in BSIM-CMG model [18].

$$V_G - V_{FB} + \frac{1}{2}\frac{Q_{d,dg}}{C_{ins,dg}} - V = -\frac{1}{2}\frac{Q_{e,dg}}{C_{ins,dg}} + v_t \cdot ln\frac{Q_{e,dg}(Q_{e,dg}+Q_{d,dg})/(4v_t\epsilon_{si}/W_{si})}{q\frac{ni^2}{N_{si}}W_{si}\left[1-exp\left(\frac{W_{si}}{4v_t\epsilon_{si}}(Q_{e,dg}+Q_{d,dg})\right)\right]} \quad (1)$$

Similarly, for the cylindrical gate (CG) GAA FinFETs, the analytical solutions becomes [17]:

$$V_G - V_{FB} + \frac{Q_{d,cg}}{C_{ins,cg}} - V = -\frac{Q_{e,cg}}{C_{ins,cg}} + v_t \cdot ln\frac{-Q_{e,cg}}{q\frac{n_i^2}{N_{si}}\pi v_t R^2} + v_t \cdot ln\left[\frac{-(Q_{e,cg}+Q_{d,cg})/4\epsilon_{si}\pi}{1-exp\left(\frac{Q_{e,cg}+Q_{d,cg}}{4\epsilon_{si}\pi v_t}\right)}\right] \quad (2)$$

where $Q_{e,dg}$ and $Q_{d,dg}$ are the total mobile electron and depletion charge per unit area, respectively. $Q_{e,cg}$ and $Q_{d,cg}$ denote the total mobile electron and depletion charge per unit length. By comparing these two equations, terms by the term, we found that these two equations are exactly the same. For example, the first right term is the multiplication of insulator capacitance (C_{ins}) and inversion change (Q_e) in both the equations. Both equations have used different ways to represent their insulator capacitance C_{ins}, channel width W_{ch}, channel doping N_{ch} and channel cross-sectional area A_{ch} as listed in table 1.

Table 1: Key Model Parameters

Param	DG	TG	QG	CG
W_{ch}	$2H_{fin}$	$2H_{fin}$+T_{fin}	$2(H_{fin}$+$T_{fin})$	2πR
C_{ins}	$W_{ch}\frac{\epsilon_{ox}}{T_{ox}}$	$W_{ch}\frac{\epsilon_{ox}}{T_{ox}}$	$W_{ch}\frac{\epsilon_{ox}}{T_{ox}}$	$\frac{2\pi\epsilon_{ox}}{ln(1+\frac{T_{ox}}{R})}$
A_{ch}	$H_{fin}T_{fin}$	$H_{fin}T_{fin}$	$H_{fin}T_{fin}$	πR^2
N_{ch}	N_{body}	N_{body}	N_{body}	N_{body}

We have developed a unified model (new normalized charge model) from the solutions of the Poisson equation for DG and CG-GAA FinFETs [19]. This model can be expressed in terms of mobile charge and the applied terminal voltages as

$$v_G - v_o - v_{ch} = -q_m + ln(-q_m) + ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) \quad (3)$$

where v_o and q_t are expressed as

$$v_o = v_{FB} - q_{dep} - ln\left(\frac{2qn_i^2 A_{ch}}{v_t C_{ins} N_{ch}}\right) \quad (4)$$

$$q_t = (q_m + q_{dep})\frac{A_{ch}C_{fin}}{\epsilon_{ch}W_{ch}^2} \quad (5)$$

where $v_G(=\frac{V_G}{v_t})$, $v_{ch}(=\frac{V_{ch}}{v_t})$ are the normalized gate and channel potentials. $q_m(=\frac{Q_e}{v_t C_{ins}})$ and $q_{dep}(=\frac{-qN_{ch}A_{ch}}{v_t C_{ins}})$ are the normalized mobile and depletion charges. C_{ins} is the insulator capacitance per unit length. In (3), we no longer have the expression for radius of wire or thickness of fin. Instead, we have the term for total charge q_t shown in right hand side of (3). q_t is a function of C_{ins} and A_{ch}. Therefore this unified GAA model can capture any cross section like nanosheet, nanowire, non-circular

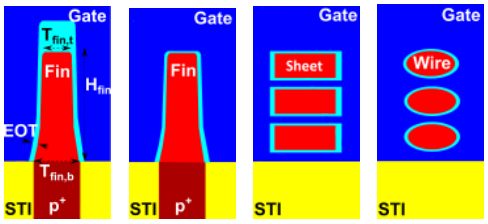


Figure 2: Schematic channel cross-section of various shapes of FinFET/GAA that can be modeled by this unified GAA Compact Model. (a) Double-Gate (DG) (b) Triple-Gate (TG) (c) Nanosheet/Quadruple Gate (QG) (d) Nnaowire/Cylindrical Gate-All-Around (CG-GAA).

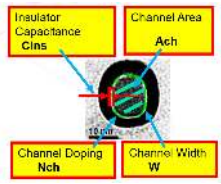


Figure 3: Cross section of a silicon nanowire (SiNW) indicating four key model parameters.

wire. Some of the example cross sections are shown in Figure 2. Four key parameters for GAA device are extracted as shown in Figure 3.

The BSIM-CMG compact model has two parts. First is the unified core derived from Poisson solution for long channel device that we have already discussed. Second is the various real-device effect sub-modules which are needed for accurate modeling of a real device. These sub-modules include effects like short channel effect (SCEs), channel length modulation (CLM), Quantum mechanical effects (QMEs), poly depletion effect, vertical and horizontal electric-field dependent mobility, length, and width scaling, temperature dependence, current saturation, impact ionization, self-heating [20], thermal and flicker noise models, gate induced drain leakage (GIDL), gate leakage, geometrically scalable parasitic models etc. as shown in Figure 4. We have represented the BSIM-CMG model validation results in Section III.

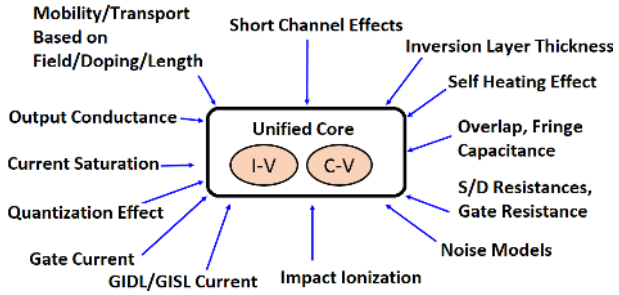
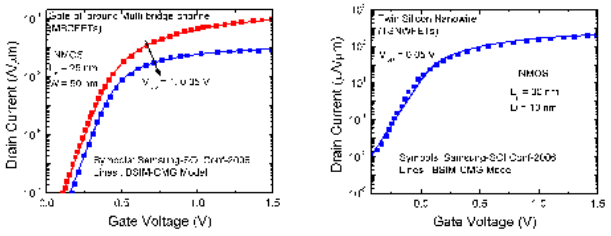
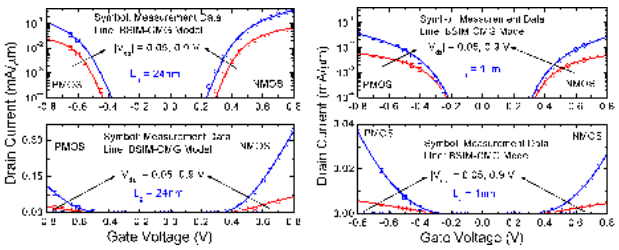


Figure 4: The structure of BSIM-CMG model is illustrated. The middle portion is the unified core and rest blocks are showing some of the real device sub-modules.



(a) (b)

Figure 5: (a) Vertically stacked multi-bridge channel FET (MBCFET) (b) Twin silicon nanowire MOSFET [11, 12].



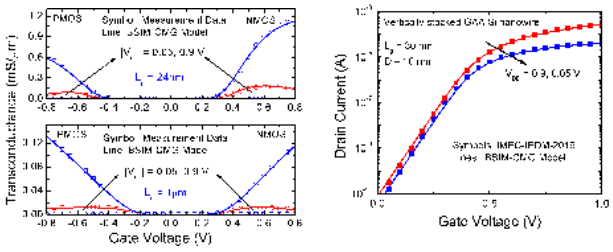
(a) (b)

Figure 6: Vertically stacked silicon GAA FETs fabricated by IMEC [13]. Drain current vs gate voltage characteristics for two values of $|V_{ds}| = 0.05, 0.9$V. (a) short channel device ($L_g = 24$nm, D = 8nm) (b) long channel device ($L_g = 1\mu$m, D = 8nm).

3 Unified GAA Model Validation

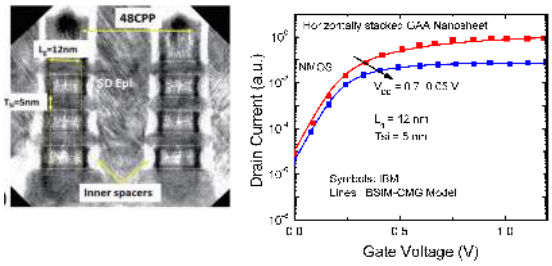
The unified model shows good agreement with 25nm channel length multi-bridge-channel FET as well as with 10nm diameter twin-silicon nanowire FET [11, 12] as shown in Figure 5(a) and Figure 5(b). The unified model accurately emulates the device behavior for vertically stacked GAA FET fabricated by IMEC [13, 14] as shown in Figure 6 and Figure 7. Furthermore, Figure 6(a) and Figure 6(b) are showing model's scaling capability results for n- and p-channel nanowire FETs. The model has shown good agreement with short and long channel length devices for NMOS and PMOS both. The BSIM-CMG model has the continuous behavior of transconductance (g_m) for different channel lengths as shown in Figure 7(a) and shows excellent agreement with the experimental data. Good agreement of g_m with experimental data ensures the robustness of mobility module. Figure 7(b) shows model results for silicon nanowire with diameter 10nm which shows model's scalability over different diameters.

Figure 8 shows that the unified model is also able to model the correct behavior of 5nm channel thickness nanosheet fabricated by IBM [15]. From Figure 5 to 8, it's clear that we have a flexible model for capturing correct behavior for different shapes of GAA FETs. To test the model's predictability for different geometries of the channel, we have finally validated our unified



(a) (b)

Figure 7: (a) Transconductance vs gate voltage characteristics for short and long channel devices. (b) Vertically stacked silicon GAA FETs fabricated by IMEC. Device dimension: L_g = 30nm, D = 10nm. [14]



(a) (b)

Figure 8: (a) Horizontally stacked GAA nanosheet fabricated by IBM [15]. Structures feature 3 sheets, inner spacer, gate length L_g=12nm, and T_{si}=5nm. (b) Stacked Nanosheet NMOS devices: drain current vs gate voltage characteristics for two drain voltages.

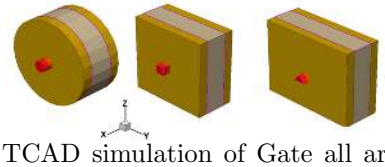


Figure 9: TCAD simulation of Gate all around FETs with of different cross sections with channel length $L_g = 12nm$ and width $W_g = 18nm$: Circular GAA FET ($A_{ch} = 28nm^2$, $C_{ins} = 0.86nF/m$), Square GAA FET ($A_{ch} = 22nm^2$, $C_{ins} = 0.76nF/m$), Triangular GAA FET ($A_{ch} = 14nm^2$, $C_{ins} = 0.73nF/m$).

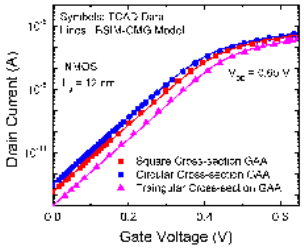


Figure 10: Unified model validation with 3D TCAD GAA devices.

model with 3D TCAD GAA devices of different cross-sections as shown in Figure 9 [21]. We have studied three GAA structures with same oxide thickness, channel length, and width except for different shapes of the channel. Only parameters changed in these devices are the cross-sectional area and corresponding insulator capacitance. The model shows excellent agreement with these TCAD GAA devices (see Figure 10) which shows that this model has significant predictive capability.

4 Conclusion

BSIM-CMG unified model can accurately model GAA FETs of different shapes including nanosheets, circular and non-circular wires and multi-bridge-channel FETs. It has the significant predictive capability which will be useful for modeling the manufacturing variation as well as device-circuits co-development. Our model has shown good agreement with silicon GAA FETs with 5nm thin film for sub-7nm technology node. According to IRDS, the diameter of vertical GAA FET will remain no less than 5nm till 1.5nm technology node. This unified model can be used for GAA device-circuits co-development and GAA circuit designs.

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REFERENCES

[1] H.-Y. Chen *et al.*, "Scaling of CMOS FinFETs towards 10 nm," *International Symposium on VLSI Technology, Systems and Applications*, pp. 46–48, Oct 2003.

[2] F.-L. Yang *et al.*, "5nm-gate nanowire FinFET," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 196–197, June 2004.

[3] Y.-K. Choi *et al.*, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 254–255, May 2000.

[4] C. Mazur *et al.*, "FDSOI: From substrate to devices and circuit applications," *Proceedings of ESSCIRC*, pp. 45–51, Sept 2010.

[5] R. Carter *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," *IEEE International Electron Devices Meeting*, pp. 2.2.1–2.2.4, Dec 2016.

[6] Y. K. Lin *et al.*, "Modeling of subsurface leakage current in low VTH short channel MOSFET at accumulation bias," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1840–1845, May 2016.

[7] D. Hisamoto *et al.*, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec 2000.

[8] J. Kedzierski *et al.*, "Extension and source/drain design for high-performance FinFET devices," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 952–958, 2003.

[9] IRDS Report, *http://irds.ieee.org/reports*, 2016.

[10] K. J. Kuhn, "Considerations for ultimate cmos scaling," *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1813–1828, July 2012.

[11] S.-Y. Lee *et al.*, "A novel multibridge-channel MOSFET (MBCFET): Fabrication technologies and characterization," *IEEE Trans. Nanotechnology*, vol. 2, no. 4, p. 253257, Dec. 2003.

[12] D. Park, "3 Dimensional GAA Transitors : twin silicon nanowire MOSFET and multi-bridge-channel MOSFET," *Proceedings of IEEE international SOI Conference*, pp. 131–134, Oct. 2006.

[13] H. Mertens *et al.*, "Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates," *IEEE Symposium on VLSI Technology*, pp. 1–2, June 2016.

[14] ——, "Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates," *IEEE International Electron Devices Meeting*, pp. 19.7.1–19.7.4, Dec 2016.

[15] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," *Symposium on VLSI Technology*, pp. T230–T231, June 2017.

[16] "Chapter 3 - Core model for FinFETs," in *FinFET Modeling for IC Simulation and Design*, Y. S. Chauhan *et al.*, Eds. Oxford: Academic Press, 2015, pp. 71 – 98.

[17] J. P. Duarte *et al.*, "A Universal Core Model for Multiple-Gate Field-Effect Transistors. Part I: Charge Model," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 840–847, Feb 2013.

[18] "Technical Manual of BSIM-CMG 109.0.0 Multi-Gate MOSFET Compact Model," Nov. 2015. [Online]. Available: http://bsim.berkeley.edu/models/bsimcmg/

[19] J. P. Duarte *et al.*, "BSIM-CMG: Standard FinFET compact model for advanced circuit design," in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, Sept 2015, pp. 196–201.

[20] B. K. Kompala *et al.*, "Modeling of nonlinear thermal resistance in FinFETs," *Japanese Journal of Applied Physics*, vol. 55, no. 4S, p. 04ED11, 2016.

[21] I. Avci *et al.*, "Three-dimensional tcad process and device simulations," in *2006 16th Biennial University/Government/Industry Microelectronics Symposium*, June 2006, pp. 41–46.