Unified Three-terminal Switch Model for Current Mode Controls

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Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

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November 8th, 2010
Blacksburg, Virginia

Keywords: current-mode control, modeling,
three-terminal switch model, equivalent circuit

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(Abstract)

Current-mode control architectures with different implementation approaches have been an indispensable technique in many applications, such as voltage regulator, power factor correction, battery charger and LED driver. Since the inductor current ramp, one of state variables influenced by the input voltage and the output voltage, is used in the modulator in current-mode control without any low pass filter, high order harmonics play important role in the feedback control. This is the reason for the difficulty in obtaining the small-signal model for current-mode control in the frequency domain. A continuous time domain model was recently proposed as a successful model for current-mode control architectures with different implementation. However, the model was derived by describing function method, which is very arithmatically complicated, not to mention time consuming. Although an equivalent circuit for a current mode control Buck converter was proposed to help designers to use the model without involving complicated math, the equivalent circuit is not a complete model. Moreover, no equivalent circuit for other topologies is available for designers. In this thesis, the primary objective is to develop a unified three-terminal switch model for current-mode control with different implementation methods, which are applicable in all the current mode control power converters.

First, the existing model for current mode control is reviewed. The limitation of average models and the discrete time model for current-mode control is identified. The continuous time model and its equivalent circuit of Buck converter is introduced. The deficiency of the equivalent circuit is discussed.

After that, a unified three-terminal switch model for current mode control is presented. Based on the observation, the PWM switch and the closed current loop is taken as an invariant sub-circuit which is common to different DC/DC converter topologies. A basic small signal relationship between terminal currents is studied and the result shows that the PWM switch with current feedback preserves the property of the

PWM switch in power stage. A three-terminal equivalent circuit is developed to represent the small signal behavior of this common sub-circuit. The proposed model is a unified model, which is applicable in both constant frequency modulation and variable frequency modulation. The physical meaning of the three-terminal equivalent circuit model is discussed. The model is verified by SIMPLIS simulation in commonly used converters for both constant frequency modulation and variable frequency modulation.

Then, based on the proposed unified model, a comparison between different current mode control implementations is presented. In different applications, different implementations have their unique benefit on extending control bandwidth. The properties of audio susceptibility and output impedance are discussed. It is found that, for adaptive voltage positioning design, constant on-time current mode control can simplifies the outer loop design.

Next, since multiphase interleaving structure is widely used in PFC, voltage regulator and other high current applications, the model is extended to multiphase current mode control. Some design concerns are discussed based on the model.

As a conclusion, a unified three-terminal switch model for current mode controls is investigated. The proposed model is quite general and not limited by implementation methods and topologies. All the modeling results are verified through simulation and experiments.

Acknowledgments

For their support and direction over years, I would like to express my heartfelt gratitude to all my professors at Virginia Tech, without whom my research and this thesis would not have been possible. In particular, I am very grateful to my advisor and committee chair, Professor Fred C. Lee, his kind help not only with research but also with my life at Virginia Tech. He is always generous to give me suggestions and ideas to help me focus on some unknown areas. His logical thoughts and earnest attitude gave me courage when I met problems. He often shares his philosophy with me, which is the most beneficial to me. His help has become my life-long heritage. I would also like to give specific appreciation to Professor Paolo Mattavelli, whose teaching, support, and critical insights influenced me in many ways. I have learned a lot from him. Dr. Mattavelli's rich knowledge and suggestions inspires me a lot. Both of them have a great impact on my life and my future career. I also wish to thank the other members of my advisory committee, Dr. Dushan Boroyevich, for his support, suggestions and encouragement throughout this entire process.

I am especially indebted to my colleagues in the VRM Group and Digital Control Group. In particular, I would like to thank Dr. Jian Li for his help and time on my research. It has been a great pleasure to work with the talented, creative, helpful and dedicated colleagues. I would like to thank all the members of our teams: Dr. Authur Ball, Mr. Pei-Hsin Liu, Dr. Yang Qiu, Dr. Junlu Sun, Dr. Shuo Wang, Mr. Jim Chen, Dr. Feng Zheng, Mr. Clark Person, Mr. Chanwit Prasantanakorn, Dr. Chuanyun Wang, Dr. Dianbo Fu, Dr. Yan Jiang, Mr. Doug Sterk, Mr. David Reusch, Mr. Zheng Luo, Dr. Fanghua Zhang, Dr. Yuling Li, Dr. Shaojun Xie, Mr. Weiyi Feng, Dr. Ke Jin, Dr. Brian Cheng, Dr. Xiaoyong Ren, Dr. Yan Dong, Mr. Zhiqiang Wang, Mr. Haoran Wu, Mr. Mingkai Mu, Mr. Yi Sun, Dr. Pengju Kong, Mr. Yipeng Su, Mr. Daocheng Huang, Mr. Qiang Li, Mr. Wei Zhang, Mr. Pengjie Lai, Mr. Zijian Wang, Mr. Qian Li, Mr. Feng Yu, Mr. Li Jiang and Mr. Shuilin Tian. My thanks also go to all of the other students I have met in CPES, especially to Mr. Jing Xue, Ms. Zhuxian Xu, Ms. Ying Lu, Dr. Michele Lim, Dr. Rixin Lai, Dr. Honggang Sheng, Mr. Dong Dong, Dr. Di Zhang, Mr. Puqi Ning, Ms. Zheng Zhao, Mr. Ruxi Wang and Mr. Dong Jiang. It has been a great pleasure, and I've had fun with them.

I would also like to give special mention to the wonderful members of the CPES staff who were always willing to help me out, Ms. Teresa Shaw, Ms. Linda Gallagher, Ms. Teresa Rose, Ms. Marianne Hawthorne, Ms. Linda Long, Mr. Robert Martin, Mr. Doug Sterk, Mr. Jamie Evans, Mr. Dan Huff, and Mr. David Fuller. Moreover, I owe a debt of the deepest gratitude to Ms. Suzanne Farmer, who offered me a great help in polishing my writing.

My deepest appreciation goes toward my parents, and my parents-in-law, who have always provided support and encouragement throughout my further education.

Last but not least, with deepest love, I dedicate my appreciation to my wife, Leshi Zhang, who has always been there with her love, support, understanding and encouragement for all my endeavors. Your love and encouragement has been the most valuable thing in my life!

This work was supported by the power management consortium(AcBel Polytech, Chicony Power, Crane Aerospace, Delta Electronics, Emerson Network Power, Huawei Technologies, International Rectifier, Intersil Corporation, Linear Technology, Lite-On Technology, Monolithic Power Systems, National Semiconductor, NXP Semiconductors, Richtek Technology and Texas Instruments), and the Engineering Research Center Shared Facilities supported by the National Science Foundation under NSF Award Number EEC-9731677. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect those of the National Science Foundation.

This work was conducted with the use of SIMPLIS software, donated in kind by Transim Technology of the CPES Industrial Consortium.

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Chapter 1. Introduction

1.1 Research Background: Current-Mode Control

Current-mode control has been widely used in the power converter design for several decades [1][2][3][4][5][6][8][9][10]. In current-mode control, as shown in Figure 1.1 the sensed inductor-current ramp, which is one of the state variables, is used in the PWM modulator. Generally speaking, two-loop structure has to be used in current-mode control.

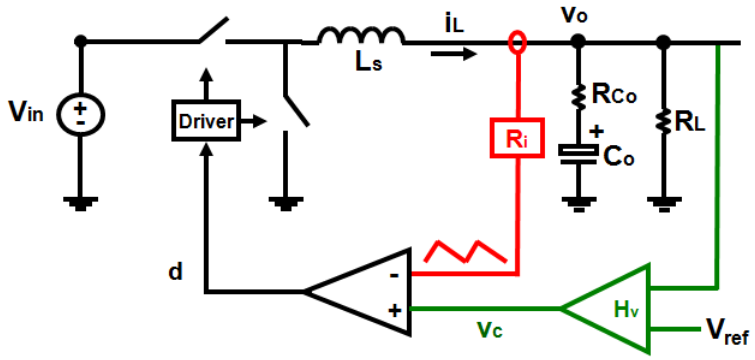


Figure 1.1 Control structure of Current-mode control

There are many different ways to implement current-mode control. One of the earliest implementations is "standardized control module" (SCM) implementation [4]. The inductor-current ramp is obtained by integrating the voltage across the inductor. Essentially, only the AC information of the inductor current is maintained in this implementation. Later, the "current injection control" (CIC) implementation was proposed in [5]. The active switch current, which is part of the inductor current is sensed usually with a current transformer or resistor. During the on-time period, the active switch current is the same as the inductor current, so peak current protection can be achieved by the limited value of the control signal v_c. Except the DC operation, systems behave the same as the SCM implementation.

Different modulation schemes in current-mode control were summarize in [6], including peak current-mode control, valley current-mode control, constant on-time control, constant off-time control. The first two schemes belong to the constant-frequency modulation, and the rest belong to the variable-frequency modulation. Charge control [7] is also an implementation of constant frequency current mode control. The implementations are shown in Figure 1.2.

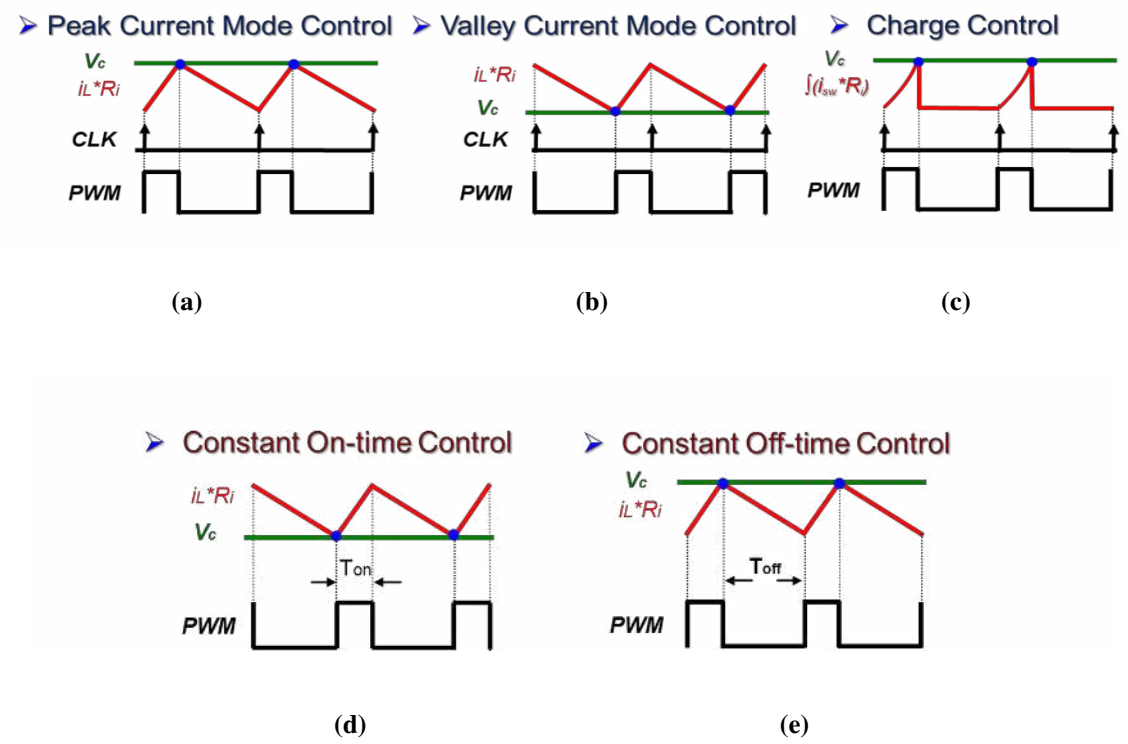


Figure 1.2. Different modulation schemes in current-mode control: (a) peak current-mode control, (b) valley current mode control, (c) constant on-time control, (d) constant off-time control, and (e) charge control

Other than those current-mode controls mentioned above, the "average current-mode control" is somewhat different [8][9]. A low-pass filter is added into the feedback path of the inductor current in order to control the average inductor current and improve the noise immunity.

1.2 Applications of Current-Mode Control in Commonly Used Topologies

Due to its unique characteristics, current-mode control is indispensable to power converter design in almost every aspect. A few applications of current-mode control are introduced in the following paragraphs.

1.2.1 Voltage Regulator Application

With the development of information technology, telecom, computer and network systems have become a large market for the power supply industry [11]. Power supplies for the telecom, computer and network applications are required to provide more power with less size and cost [12][13]. To meet these requirements, the distributed power system (DPS) is widely adopted. As shown in Figure 1. 3, the distributed power system is characterized by distribution of the power processing functions among many power processing units [14]. DPS system has many advantages, such as less distribution loss, faster current slew rate to the loads, better standardization and ease of maintenance[17][18].

The paralleling module approach for point-of-load (POL) converters has been successfully used in various power systems. The multi-phase buck converter topology can be treated as an example to demonstrate the benefits of this approach in terms of thermal management, reliability and power density. However, the difference between paralleled modules will cause the current imbalanced, resulting in some units operating with higher temperature -- a contributor to reduced reliability. Therefore, the challenge in paralleling modular supplies is to ensure predictable, uniform current sharing.

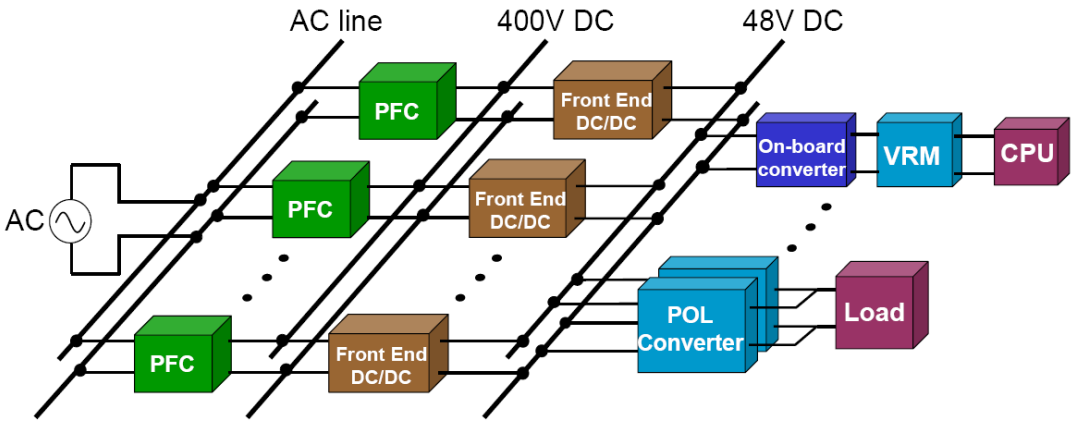


Figure 1. 3. A typical distributed power system

There are many methods to achieve current sharing among different modules (phases). One of the most popular methods is the active current sharing method with current-mode control [19]. As shown in Figure 1. 4, a current sharing bus is easily built by the control signal in peak current-mode control. It usually provides a common current reference. Each phase then adjusts its own control to follow this common reference thus the load current will finally evenly distributed among these phases.

In order to provide power to a microprocessor with high current and low voltage demand, a dedicated power supply named voltage regulator (VR) is used. Multi-phase buck converters are widely used in VRs because of their simple structure, low cost and low conduction loss. Current VR faces the stringent challenge of not only high current but also a strict transient response requirement. Figure 1.5 shows the VR output load line from the Intel VRD 11.1 specification. The vertical axis is the VR output impedance, and the horizontal axis is frequency.

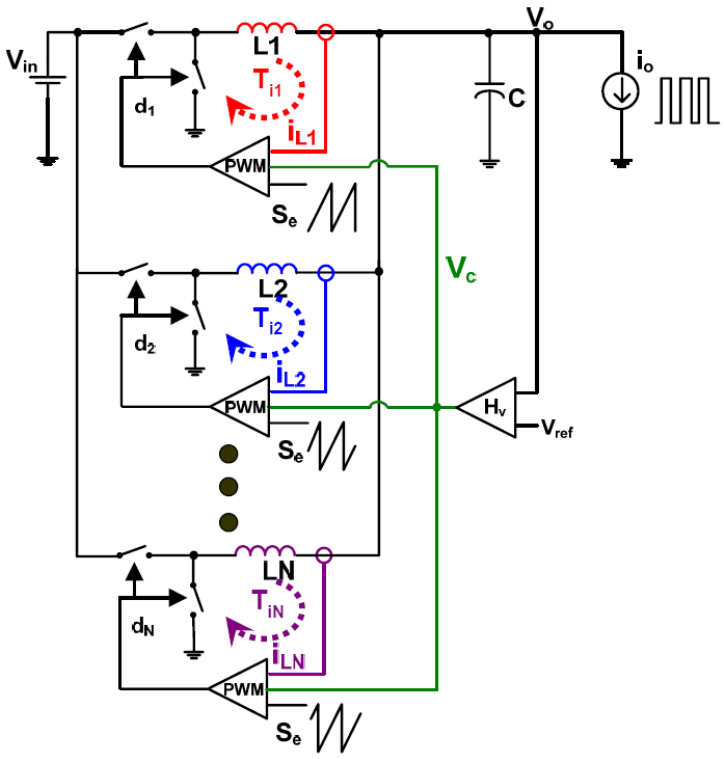


Figure 1. 4. A multi-phase buck converter with peak current-mode control

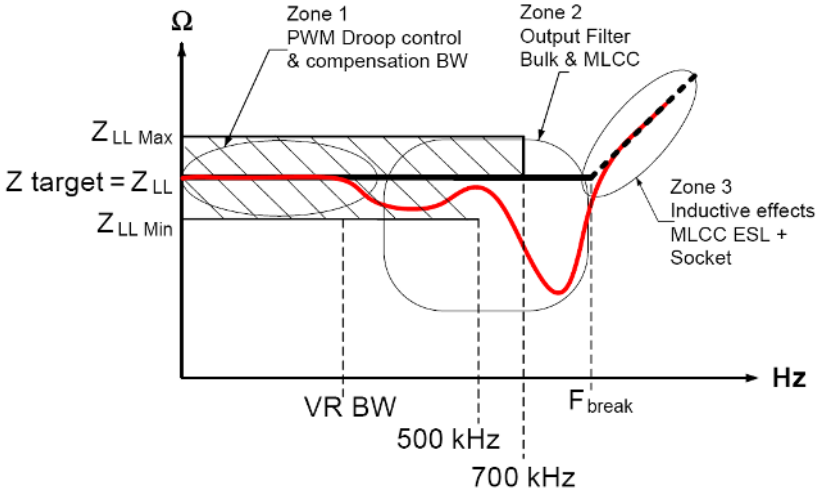


Figure 1.5. Output impedance specification of Intel VRD 11.1

Current-mode control architecture is widely used to achieve constant-output impedance design to meet the load-line requirement [20][21][22][23][24][25]. Current-mode control architecture is endowed with the capabilities of controlling both

the output voltage and the inductor current, which is one of key factors to achieve AVP control.

1.2.2. Power factor correction

Due to the ever-increasing requirement for improved power quality, the use of the power factor correction (PFC) circuit for off line power supplies has been dramatically increased. The high frequency switch mode power factor correction converter is called a PFC stage and, it is usually inserted in the equipment to shape the line input current into a sinusoidal waveform and its line current is in phase with the line voltage.

Boost converter with current mode control is one of the most popular solutions for PFC stage. To shape input current, peak current mode control is a simple control scheme [26].

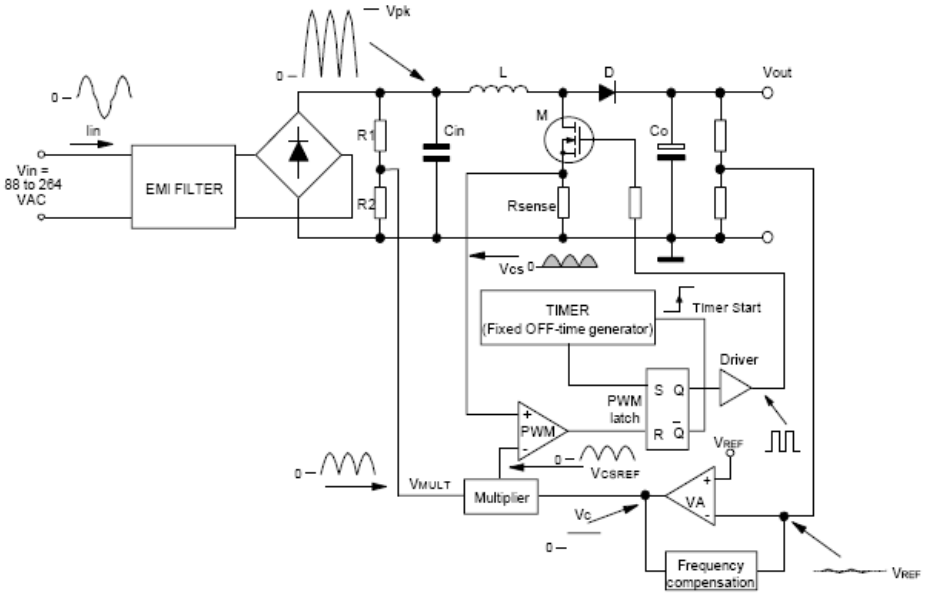


Figure 1.6. Constant off-time current mode control CCM Boost PFC

To avoid the sub-harmonic oscillation issue, [27] [28]suggest a constant off-time current mode control as the implementation of the current loop, as shown in Figure

1.6. Constant off-time control is a variable frequency control scheme, so it also helps to reduce the peak energy of the noise generated and simplifies the ability to comply with EMI regulations.

For low power applications, the Flyback converter is more attractive than the boost converter because of its simplicity. To control the average value of the pulsating input current of the Flyback converter, charge control scheme is used in [7]. By employing charge control, a Flyback converter operating in CCM can achieve a unity power factor.

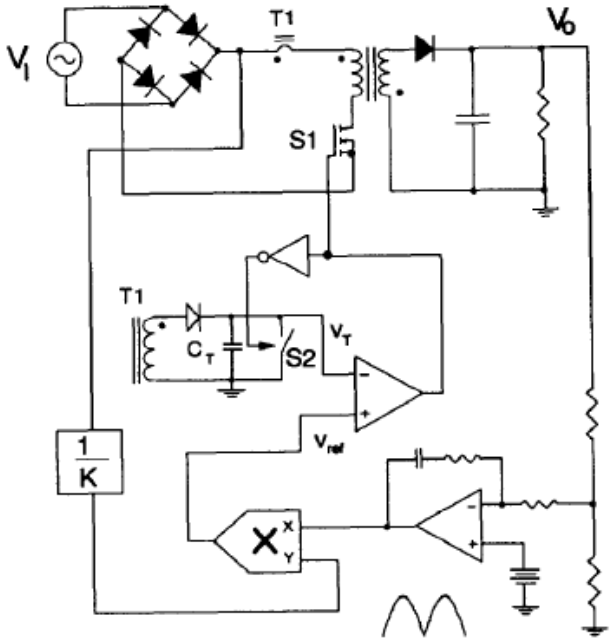


Figure 1.7. Charge control Flyback PFC

1.2.3. Battery Charger

Batteries are commonly used in renewable generation systems, electrical vehicles, communications systems and computer systems as electrical energy storage elements. The major rechargeable batteries readily available today are nickel-cadmium (NiCd), nickel-metal-hydride (NiMH), sealed-lead-acid (SLA) and lithium-ion (Li-Ion).

Different battery chemistries have different charge requirements. NiCd and

NiMH batteries are charged with a constant-current profile. SLA and Li-Ion batteries can be charged with a constant-voltage, current-limited supply. A typical Li-Ion battery charge cycle begins when the voltage at battery voltage exceeds the under voltage lockout threshold level and the IC is enabled. If the battery has been deeply discharged and the battery voltage is less than 2.7V, the charger will begin with the programmed trickle charge current.

When the battery exceeds 2.7V, the charger begins the constant-current portion of the charge cycle with the charge current equal to the programmed level. As the battery accepts charge, the voltage increases. When the battery voltage reaches the recharge threshold, the programmable timer begins. Constant-current charging continues until the battery approaches the programmed charge voltage of 4.1V or 4.2V/cell at which time the charge current will begin to drop, signaling the beginning of the constant-voltage portion of the charge cycle. The charger will maintain the programmed preset float voltage across the battery until the timer terminates the charge cycle.

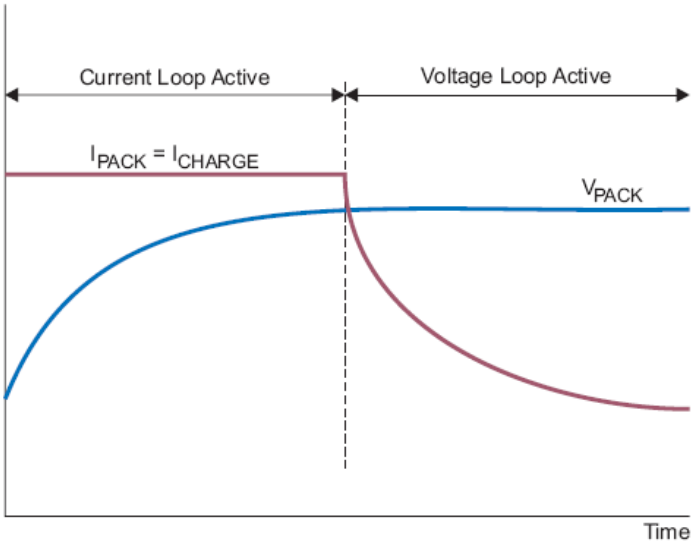


Figure 1.8. Typical charge current and voltage profile

To improve efficiency, switching mode power converters are widely used in battery charger application. To provide constant current/ constant-voltage, current mode control power source, current mode control is the key technique in charger

controller.

The typical operation of the battery charger can be separate into two periods [29]. The charge current-regulation loop is in control as long as the battery voltage is below the set point. When the battery voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. The typical charge current and voltage profile is shown in Figure 1.8.

In smaller area and lower cost solution, charger and DC/DC converter can be integrated in a bi-directional power converter circuit, as shown in Figure 1.9. When the adapter presents, the power flows from adapter to battery. When the device is powered by battery, power flows from battery to system load. To achieve such a function, a Flyback converter with current mode control is an alternative solution [30]. In this application, current mode control serves two goals: to control the charging current in charger mode and improve the dynamic response in the converter mode.

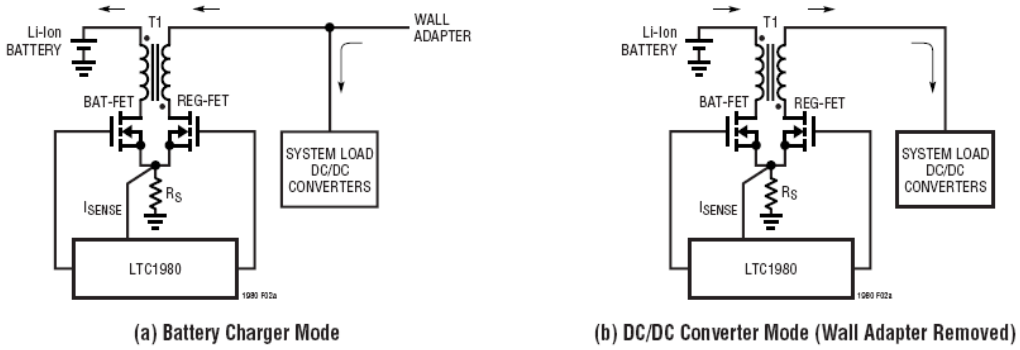


Figure 1.9. Bi-directional Flyback charger and DC/DC converter

1.2.4. LED Driver

LED technology has emerged as a promising lighting technology to replace the energy-inefficient incandescent lamps and mercury-based fluorescent lamps [31]. LEDs are current-driven devices whose brightness is proportional to their forward current. Also, some solutions use the LED V-I curve to determine what voltage needs to be applied to the LED to generate the desired forward current. However, using this

method, any change in LED forward voltage creates a change in LED current. At the same time, the voltage drop and power dissipation across the ballast resistor waste power and reduce battery life.

Most of the high performance LED drivers drive the LED with a constant-current source. In this way, forward voltage does not affect LED brightness. Many applications, such as display backlighting, need more than one LED to provide enough brightness. In these applications, multiple LEDs should be connected in a series configuration to keep an identical current flowing in each LED.

Since Buck converter output current is an inductor current, a non-pulsating current, Buck converter without output capacitor is widely used as a LED driver due to its simple structure, low cost and fast response. In a Buck converter without output capacitor, controlling inductor current is controlling the LED forward current. So, current mode control is a natural choice for Buck LED driver.

Based on the characteristics of LED, all LEDs have a relationship between their luminous flux and forward current, IF, that is linear up to a point. Beyond that point, increasing IF causes more heat than light. High ripple current forces the LED to spend half of the time at a high peak current, putting it in the lower lm/W region of the flux curve. Usually, absolute maximum ratings for peak current are close to or often equal to the ratings for average current, as shown in Table 1.1 [32]. High current density in the LED junction lowers lumen maintenance, providing yet another incentive for keeping the ripple current under control.

To achieve a constant forward current ripple, adaptive on time and constant off-time current mode control implementation is a common solution. Adaptive on time control changes the top switch on-time to be proportional to Vin-Vout, so that the current ripple is kept constant with input voltage variation.

Table 1.1 Typical high power LED specification

Parameter	White/Green/ Cyan/Blue/ Royal Blue	Red/ Red-Orange/ Amber
DC Forward Current (mA)[1]	1000	1540
Peak Pulsed Forward Current (mA)	1000	2200
Average Forward Current (mA)	1000	1400
LED Junction Temperature (°C)	135	135
Storage Temperature (°C)	-40 to +120	-40 to +120
Soldering Temperature (°C)[2]	260 for 5 seconds max	260 for 5 seconds max
ESD Sensitivity [3]	±16,000V HBM	±16,000V HBM

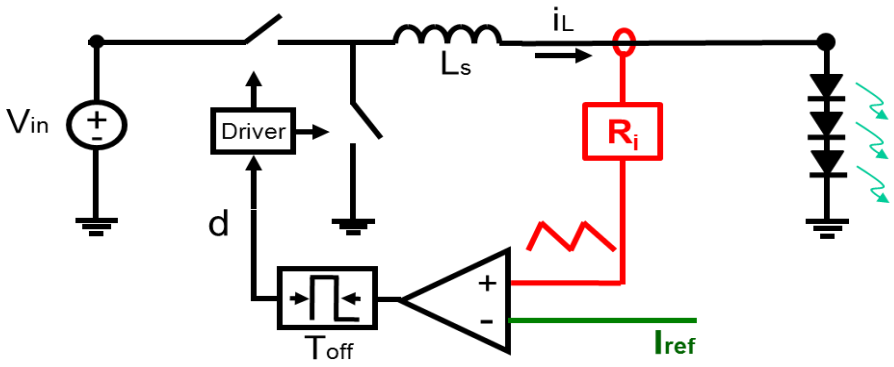


Figure 1. 10. Current mode control Buck LED driver

Constant off-time implementation is simpler than adaptive on-time [33]. Forward voltage is a fix voltage under certain forward current levels, so the inductor current down slope is determined by the output current level. By fixing the off-time of the top switch, the inductor ripple is expressed as:

$$I_{ripple} = V_{fwd} \cdot T_{off} = Const. \quad (1.1)$$

Besides Buck, other current mode control converters are also widely used in the LED driver design. Many of today's portable electronics require LED-driver solutions. Lithium-ion battery output voltage is 2.7~5.2V while typical forward voltage of each white LED is about 3~4 volt. So, for converters designed for a single LED, such as a digital camera flash light application, a Buck-boost converter is used [34]. In

backlighting application, to drive a series of white LEDs with a constant current source, a popular solution is to use a Boost or Buck-boost converter with current mode control [35].

1.3 Thesis Outline

Current-mode control architectures with different implementation approaches have been an indispensable technique in many applications, such as voltage regulator, power factor correction, battery charger and LED driver. Since the inductor current ramp, one of state variables influenced by the input voltage and the output voltage, is used in the modulator in current-mode control without any low pass filter, high order harmonics play important role in the feedback control. This is the reason for the difficulty in obtaining the small-signal model for current-mode control in the frequency domain. A continuous time domain model was recently proposed as a successful model for the current-mode control architectures with different implementation. However, the model was derived by describing function method, which is very complicated arithmetically, not to mention time consuming. Although an equivalent circuit for the current mode control Buck converter was proposed to help designers to use the model without involving complicated math, the equivalent circuit is not a complete model. Moreover, no equivalent circuit for other topologies is available for designers. In this thesis, the primary objective is to develop a unified three-terminal switch model for current-mode control with different implementation methods which are applicable in all the current mode control power converters. First, the existing model for current mode control is reviewed. After that, a unified three-terminal switch model for current mode control is proposed. Then, based on the proposed unified model, a comparison between different current mode control implementation is presented. At last, the model is extended to multiphase current mode control. Some design concerns are discussed based on the model. In the end, conclusions are given.

The detailed outline is elaborated as follows.

Chapter 1 is the review of the background of current-mode control and the application of current-mode control. Current-mode control architectures with different implementation approaches have been an indispensable technique in many applications, such as voltage regulator, power factor correction, battery charger and LED driver. An accurate model for current-mode control is indispensable to system design. However, available models can only solve partial issues. The primary objective of this thesis is to develop a unified three-terminal switch model for current-mode control with different implementation methods which is applicable in all the current mode control power converters.

In Chapter 2, the existing model for current mode control is reviewed. The limitation of average models and discrete time model for current-mode control is identified. The continuous time model and its equivalent circuit of Buck converter is introduced. The deficiency of the equivalent circuit is discussed.

In Chapter 3, a unified three-terminal switch model for current mode control is presented. Based on the observation, the PWM switch and the closed current loop is taken as an invariant sub-circuit which is common to different DC/DC converter topologies. The Basic small signal relationship is studied and the result shows that the PWM switch with current feedback preserves the property of the PWM switch in power stage. A three-terminal equivalent circuit is developed to represent the small signal behavior of this common sub-circuit. The proposed model is a unified model, which is applicable in both constant frequency modulation and variable frequency modulation. The physical meaning of the three-terminal equivalent circuit model is discussed. The model is verified by SIMPLIS simulation in commonly used converters for both constant frequency modulation and variable frequency modulation.

In Chapter 4, based on the proposed unified model, a comparison between different current mode control implementation is presented. In different applications,

different implementations have unique benefit of extending control bandwidth in different applications. The properties of audio susceptibility and output impedance are discussed. It is found that, for adaptive voltage positioning design, constant on-time current mode control can simplified the outer loop design.

In Chapter 5, since multiphase interleaving structure is widely used in PFC, voltage regulator and other high current application, the model is extended to the multiphase current mode control. Some design concerns are discussed based on the model.

Chapter 6 is conclusions with the summary and the future work.

Chapter 2. Review of Existing Models for Current Mode Controls

2.1 Complexity of Current-Mode Control Modeling

Current-mode control's modulation is based on the inductor current ramp, a state variable. Essentially, for any PWM converter with a small signal perturbation f_m, the PWM modulator generates multiple frequency components, including the fundamental component (f_m), the switching frequency component (f_s) and its harmonic ($n*f_s$), and the sideband components ($f_s \pm f_m$, $nf_s \pm f_m$). All these frequency components exist in the state variable of the switching circuit. In current mode control case, inductor current is fed back to the modulator, and there is no enough attenuation on the high frequency components. All frequency components are coupled through the modulator, so neither the sideband components nor the switching frequency components can be ignored. As a result, frequency domain analysis shows its obvious limitation in analysis of current loop. Previous average models for current-mode control failed to consider high frequency components.

It is relatively easy for the outer voltage loop of the current mode control converter, since high frequency components can be attenuated due to the low pass filter of the power stage and feedback compensation.

2.2 Existing Model of Current-Mode Control

Due to the popularity of the current-mode control and the complexity of the current mode control, the research on modeling current-mode control has over 30 years of history and is still on going.

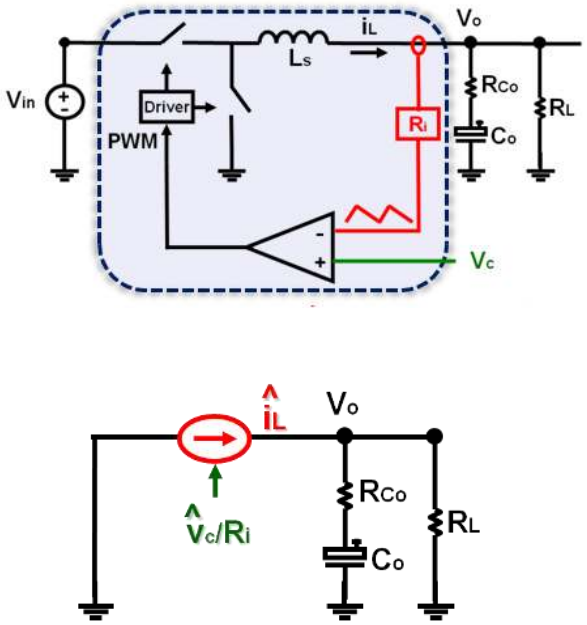
Most of the early work on current mode control modeling focuses on peak current mode control due to its popularity. In recent decades, variable frequency

current mode control, for example constant on-time control, is widely used because of its unique advantage, such as high light load efficiency and simple implementation. The modeling of variable frequency current mode control has gained more attention recently.

To review the previous modeling work for current mode control, the modeling methodologies can be categorized into several groups and listed as follows.

A. "Current source" model

The purpose of the current loop is to make the inductor current follow the control signal. Based on this physical interpretation, the "current-source" concept is the simplest model for model current-mode control [36]. In this model, the inductor current is treated as a well-controlled current source, as shown in Figure 2.1. However, it is too simple to predict subharmonic oscillations and the audio susceptibility.



(a)

Figure 2.1. current-mode control: (a) control structure, (b) "current source" concept

B. Average model

Under purturbation, although a switching converter generates many side band components, since there must be a low-pass filter in the power stage, the average

concept, which only capture the modulation frequency information, can be sucessfully used in the modeling of the switching converter[37][38][39][55][40][41][42][43]. Based on average models for power stage, the average models for peak current-mode control are developed[44] [45][46][47][48][49][50][51][52][53][54].

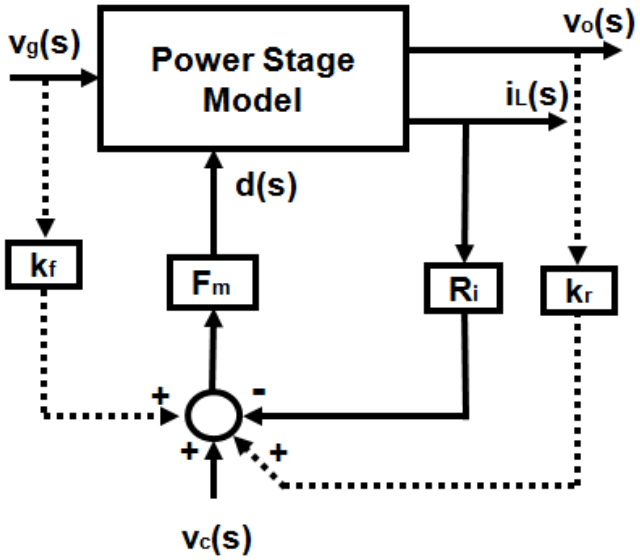


Figure 2.2. Average model for current-mode control with two additional feed forward gain and feedback gain

In the current loop, averaged inductor-current information is fed back to the modulator with pure sensing gain. Modulator gain F_m, is derived by geometrical calculations, assuming a constant inductor current ramp and an external ramp. In order to model the effect of the variation of the inductor current ramp, two additional feed forward gain and feedback gain are added [45].

The low-frequency response can be well predicted by the average models. However, one common issue of the average models is that they can't predict subharmonic oscillations in peak current-mode control, as shown in Figure 2.3.

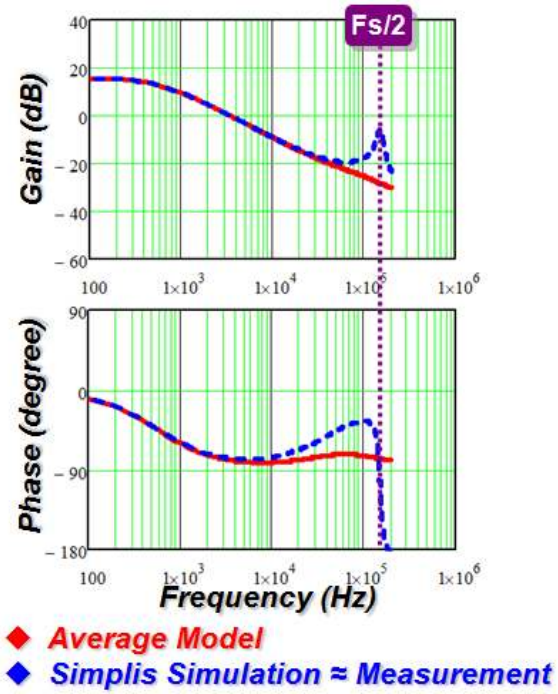
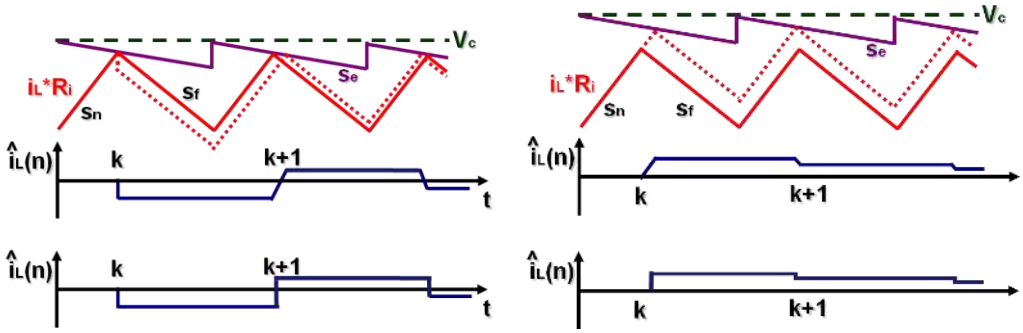


Figure 2.3. Control-to-output transfer function comparison (D=0.45)

C. Discrete-time model and sample data model



(a)

Figure 2.4. Discrete-time analysis: (a) natural response, and (b) forced response

In peak current-mode control, the inductor current error stays the same for one switching cycle, until the next sampling event occurs. This behavior is similar to a discrete time system. Based on this concept, the discrete-time model for current mode control is proposed by D. J. Packard [55] and A. R. Brown [56]. The analytical

prediction of the current loop instability in peak current-mode control was first achieved.

Based on the time-domain waveform of the inductor current, as shown in Figure 2.4, the response of the inductor current is divided into two parts, including the natural response and the forced response. The discret-time expression can be found as:

Natural response:
$$\hat{i}_L(k+1) = -\alpha \cdot \hat{i}_L(k) \tag{2.1}$$

Forced response:
$$\hat{i}_L(k+1) = (1+\alpha)/R_i \cdot \hat{v}_c(k+1) \tag{2.2}$$

where $\alpha = (s_f - s_e)/(s_n + s_e)$, s_n is the magnitude of the inductor current slope during the on-time period, s_f is the magnitude of the inductor current slope during the off-time period, s_e is the magnitude of the external ramp, and R_i is the sensing gain of the inductor current.

Based on the combination of two parts, the control-to-inductor current transfer function in the discrete-time domain can be calculated as:

$$H(z) = \frac{\hat{i}_L(z)}{\hat{v}_c(z)} = \frac{1+\alpha}{R_i} \frac{z}{z+\alpha} \tag{2.3}$$

The discrete-time transfer function shows that there is a pole located at α. The system stability is determined by the absolute value of α, which is a function of s_n, s_f, and s_e. The absolute value of α has to be less than 1 to guarantee system stability. For example, when s_e=0 and s_n<s_f (D>0.5), the absolute value of α is larger than 1, which means the system is unstable. This model can accurately predict subharmonic oscillations and the influence of the external ramp in peak current-mode control and valley current-mode control.

In order to model peak-current mode control in the continuous-time domain instead of the discrete-time domain, sample-data analysis by A. R. Brown [56] is performed to explain the current-loop instability in the s-domain.

Although the discrete-time model and sampled-data model can precisely predict the high-freqeuncy response, it is hard to use, just like the discrete-time model.

D. Modified average model

In order to extend the validation of the averaged models to the high-frequency range, several modified average models are proposed based on the results of discrete-time analysis and sample-data analysis [57][58][59][60][61][62][63][64][65].

One of popular models is investigated by R. Ridley [59], which provided both the accuracy of the sample-data model and the simplicity of the three-terminal switch model. Essentially, R. Ridley's modeling strategy is based on the hypothesis method. In this method, first, the control-to-inductor current transfer function is obtained by transferring previous accurate disctrete-time transfer function (2.3) into its continuous-time form:

$$\frac{i_L(s)}{v_c(s)} = \frac{1}{R_i}\frac{1+\alpha}{sT_{sw}}\frac{e^{sT_{sw}}-1}{e^{sT_{sw}}+\alpha} \tag{2.4}$$

Then, "sample and hold" effects are equivalently represented by the $H_e(s)$ function which is inserted into the feedback path of the inductor current in the continuous avarge model, as shown in Figure 2.5. Another form of the control-to-inductor current transfer function can be calculated based on this assumed average model:

$$\frac{i_L(s)}{v_c(s)} = \frac{F_m F_i(s)}{1+F_m F_i(s) R_i H_e(s)} \tag{2.5}$$

Finally, based on (2.4) and (2.5), the $H_e(s)$ function is obtained as

$$H_e(s) = \frac{sT_{sw}}{e^{sT_{sw}}-1} \tag{2.6}$$

Following the same concept used in [45], the complete model is completed by adding two additional feed-forward gain and feedback gain. Due to its origination from the discrtete-time model, there is no doubt that this model can accurately predict

subharmonic oscillations in peak current-mode control and valley current-mode control. According to the control-to-output transfer function, as shown in Figure 2.6, the position of the double poles at high frequency is determined by the duty cycle value.

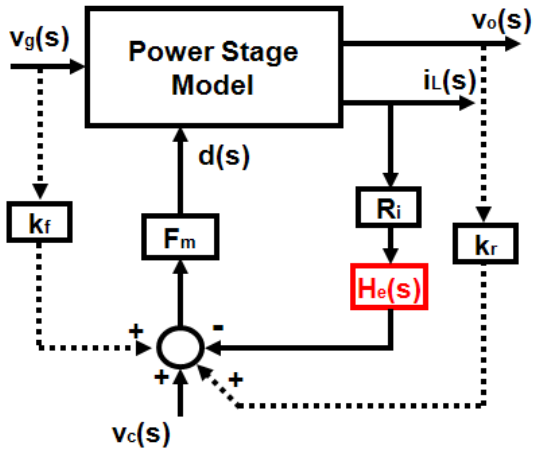


Figure 2.5. R. Ridley' model for peak current-mode control

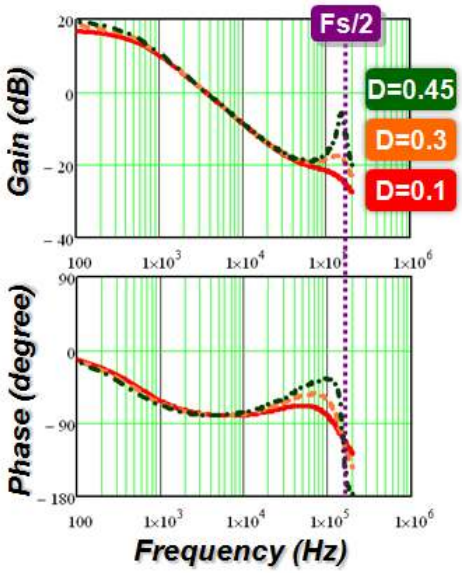


Figure 2.6. Control-to-output transfer function based on R. Ridley' model ($s_e = 0$)

Another modified models is proposed by F. D. Tan and R. D. Middlebrook [61]. In order to consider the sampling effects in the current loop, one additional pole needs

to be added to a current-loop gain derived from the low-frequency model, as shown in Figure 2.7.

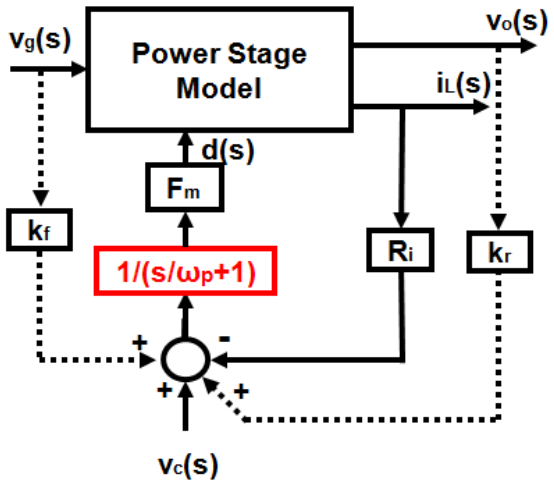


Figure 2.7. F. D. Tan and R. D. Middlebrook's model for peak current-mode control

Further analysis based on the modified models above is discussed for peak current-mode control [63][64][65]. The models for average current-mode control and charge control are obtained by extending the modified average model [66][67][68].

So far, R. Ridley's model is the most popular model for system design.

E. Continuous time model

In constant frequency peak current-mode control, the inductor current error varies at switch off instant and stays the same for one switching period. This is called the "sample and hold" effect.

For variable frequency modulation current mode control, the current-loop behavior is different from that in peak current-mode control. For example, in constant on-time control, as shown in Figure 2.8, the inductor current goes into steady state in one switching period. No "sample and hold" effects exist in constant on-time conrol.

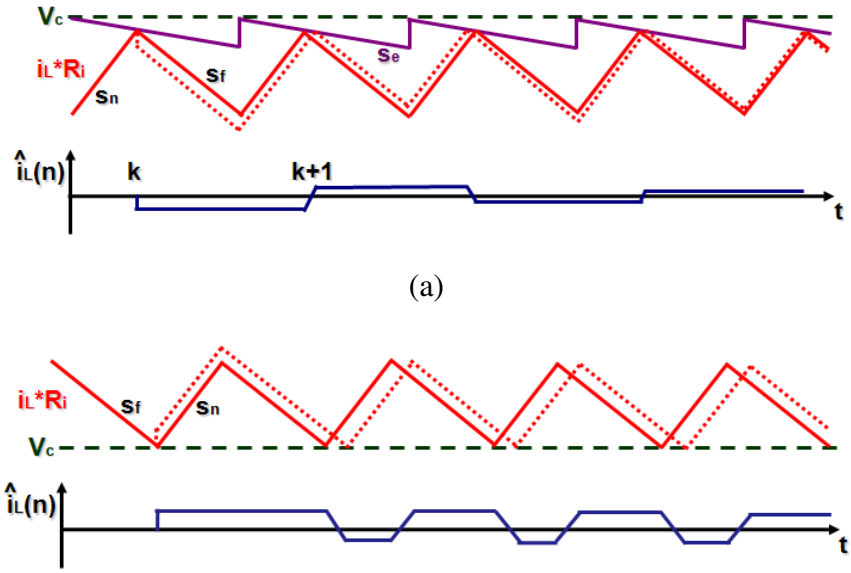


Figure 2.8. Perturbed inductor current waveform: (a) in peak current-mode control, and (b) in constant on-time control

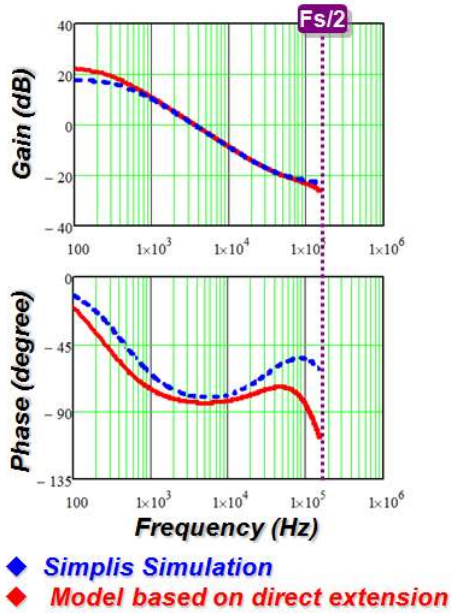


Figure 2.9. Discrepancy in the extended model

Discrete-time analsys and sample-data analysis is only applicable to a constant frequency sampling system. They can't be applied to variable frequency current mode control. Figure 2.9 shows that R. Ridley's extended model to constant on-time control [69] is not very good at predicting the small signal behavior of the switching circuit.

To solve this issue, a continuous time model is proposed in [70]. The inductor, the switches and the PWM modulator are treated as a single entity to model instead of breaking them into parts to do it. As shown in Figure 2.10, a sinusoidal perturbation with a small magnitude at frequency f_m is injected through the control signal v_c; then, based on the perturbed inductor current waveform, the describing function [71] from the control signal vc to the inductor current i_L can be found by mathematical derivation. The same method is applied two derive two additional terms that represent the influence from the input voltage v_{in} and the output voltage v_o.

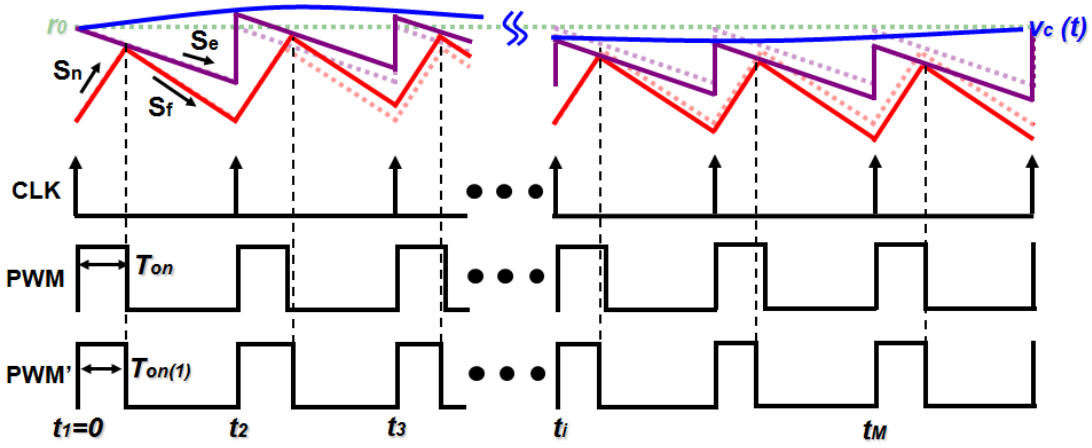


Figure 2.10. Perturbed inductor current waveform in peak current-mode control

This approach can be applied not only to constant-frequency modulation but also to variable-frequency modulation. The accuracy of the model is not limited by the frequency range. The fundamental difference between different current-mode controls is elaborated based on the models obtained from the new modeling approach.

Essentially, the current mode control converter is an infinite order system. For practical design purposes, the system can be simplified as a third order system. In

control to output transfer function, a single pole determined by load is at low frequcny and a pair of high frequency double poles are located at high freqency. The position of the double pole located at the high frequency is different for constant frequency modulation and variable frequency cases. For constant frequency modulation, the location of the double poles locate is at 1/2 f_{sw} and it is possible for them to move to the right half plane. For variable frequency modulation, the double poles location is determined by T_{on} or T_{off}, and the double poles never move to the right half plane. That means the variable frequency modulation current loop is always stable.

Although the continous time model using the describing fucntion method provides an accurate enough model, the mathmatical derivation is too complicated for practical use.

For a current mode control Buck converter, to simply represent the output voltage transfer function $\hat{v}_o / \hat{v}_c$ and input to output transfer function $\hat{v}_o / \hat{v}_{in}$ and output impedance, an equivalent circuit is proposed, as shown in Figure 2.11. The resonant of the equivalent capacitor C_e and L_s characterize the high frequcny double pole and R_e represents the damping effect.

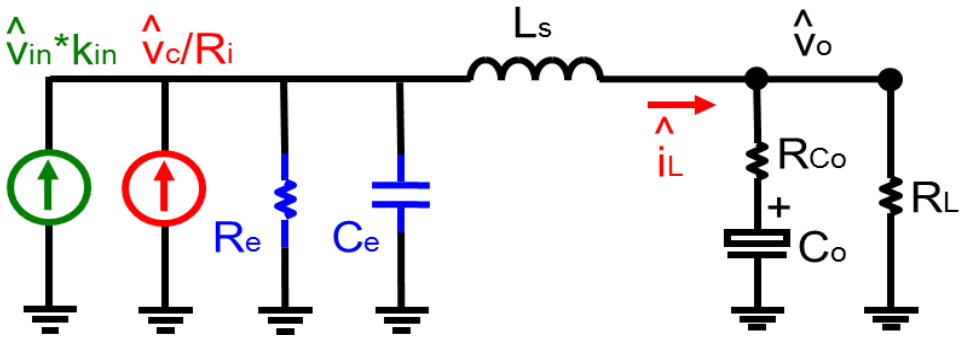


Figure 2.11. Equivalent circuit for current mode control Buck converter

However, this equivalent circuit is not a complete model for a current mode control Buck converter since the input current property is lost. Moreover, no equivalent circuit of other current mode control converters are available.

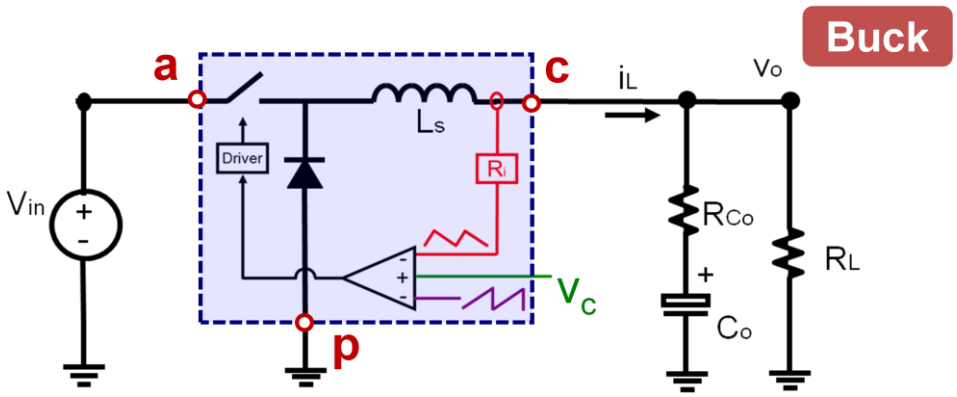
2.3 Summary

In this chapter, the existing model for current mode control is reviewed. The limitation of current source model, average models, discrete time model and modified average model for current-mode control is identified. The continuous time model and its equivalent circuit of Buck converter are introduced. The deficiency of the equivalent circuit is discussed.

Chapter 3. Proposed Unified Three-terminal Switch Mode for Current Mode Controls

This chapter introduces a new unified three-terminal switch mode for current-mode controls. The proposed model takes the active switch, passive switch and the closed current loop as an invariant entity, which is a common sub-circuit for different topologies, and uses the three-terminal equivalent circuit to represent the small signal behavior of this common sub-circuit in current mode control power converter. The derivation process utilizes the small signal relationship between the terminal voltage and the current, which are obtained from describing function method. The proposed model is a unified model, which is applicable to constant frequency peak current mode control, valley current mode control and charge control, and variable frequency constant on-time control and constant off-time control. Small signal model for commonly used topologies with current mode control can be easily obtained by replacing the three-terminal switch with the current feedback loop, by the three-terminal small signal equivalent circuit point by point.

3.1 Common Invariant Structure in Current Mode Control Power Converters



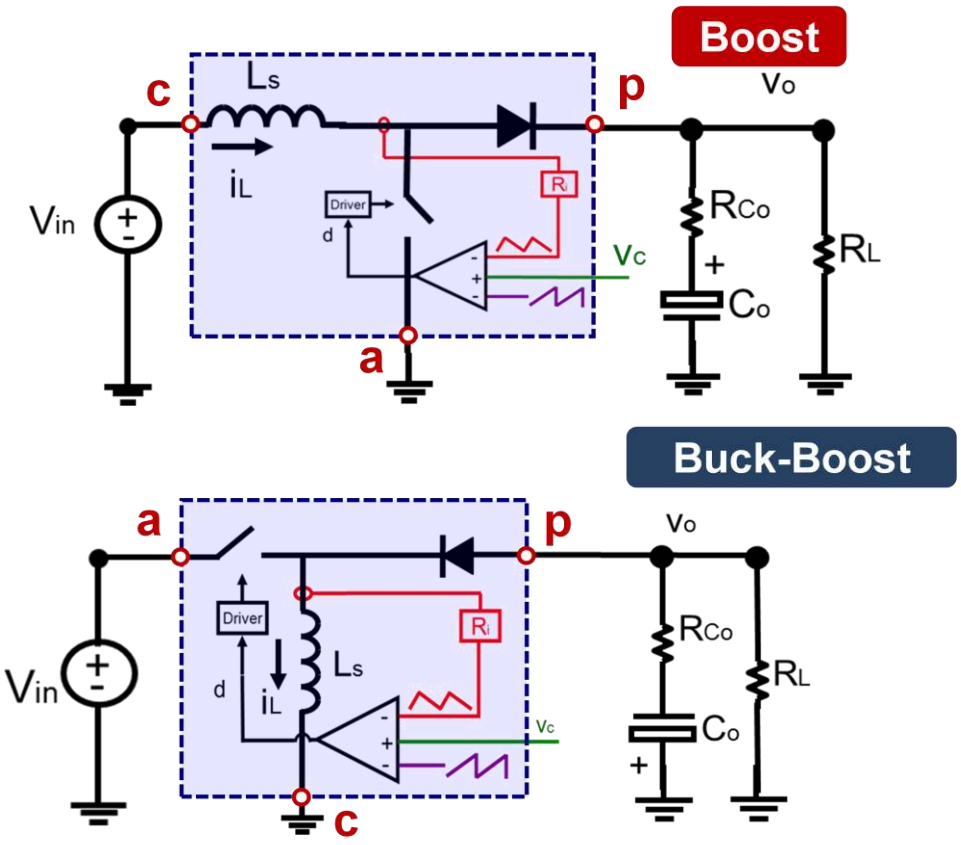


Figure 3.1 Current mode control DC/DC converters

Current-mode control has unique advantages over voltage mode control, such as fast dynamic response and inherent current limit. It is also an indispensable technique to achieve current sharing and, AVP control. As a result, current mode control has been widely used in the power converter design. The most commonly used power converter topologies are Buck, Boost, Buck-boost, Flyback, forward and some other topologies derived from these basic ones.

Basic current mode control power converters are shown in Figure 3.1. Although topologies are different, they have basic structure in common. It consists of an active switch, a passive switch, inductor and a closed current loop. The common node active switch and passive switch connects to the inductor. The terminal designations a,p,c refer to active, passive, and common respectively. v_c is the control signal, which is the output of the voltage loop compensator. The common three-terminal structure is shown in Figure 3.2.

This three-terminal structure is an extension of the three-terminal switch of power

stage. It is the only non-linear device of the power converter. Take the three-terminal structure as a basic building block of current mode control converters, then converters can be obtained by a simple cyclic permutation of the three-terminal switch and connecting external linear components to it. All the ports of the three-terminal switch should be connected to voltage ports as indicated in Figure 3.2. By modeling this common building block with an equivalent circuit, small signal equivalent circuits for current mode control power converters can be obtained by substituting the three-terminal switch with its equivalent circuit point-to-point.

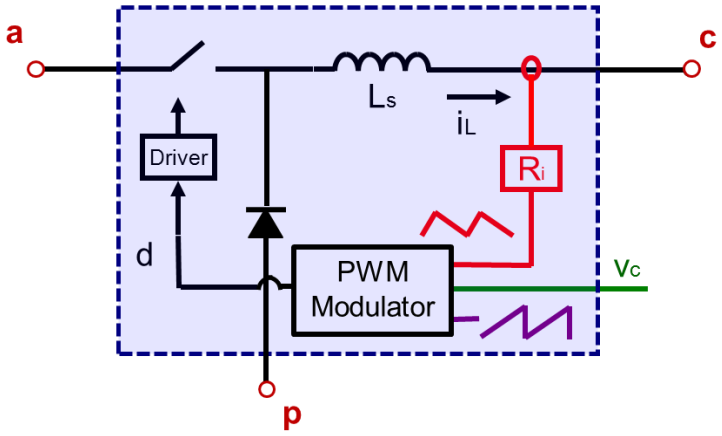


Figure 3.2 Common invariant structure in current mode control power converters

3.2 General Small Signal Relationship for Three-terminal Switch

A three-terminal switch with current feedback loop, as mentioned in section 3.2, is an extension of three-terminal switch of power stage. The closed current loop is added to the power stage three-terminal common structure and the inductor is included into the common block.

In [42], a small signal relationship is derived based on instantaneous voltage and current waveform. Current in the active terminal is always the same as the current in the common terminal during the switch ON-interval DT, and equals to zero during the switch OFF-interval. The expression of active switch current is given by Eq.(3.1). The waveform is shown in Figure 3.3. This description is true no matter which

configuration the switch is implemented in.

$$\bar{i}_a(t) = \begin{cases} \bar{i}_c(t), & \mathbf{0} \le t \le DT_s \\ \mathbf{0}, & DT_s \le t \le T_s \end{cases} \tag{3.1}$$

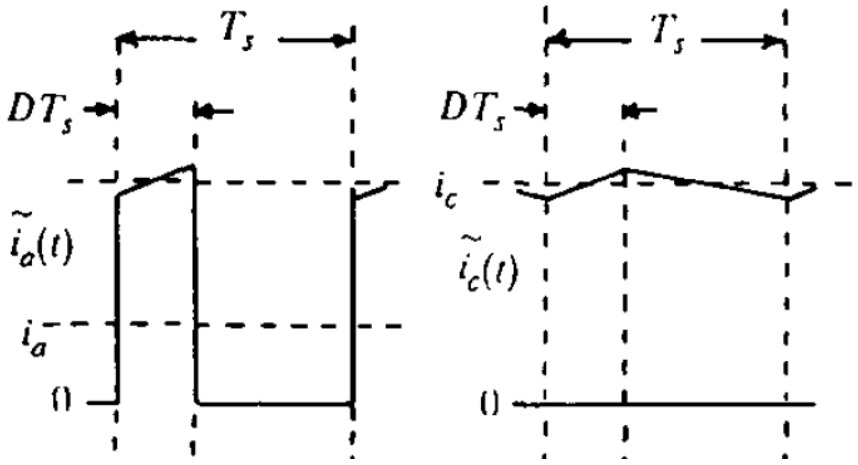


Figure 3.3 Basic waveform of PWM switch

Using average concept, average terminal currents i_a, and i_c, we have from very simple relations:

$$i_a = d \cdot i_c \tag{3.2}$$

Perturb the Eq.(3.2) and neglect the high order term, a small signal relationship between i_a and i_c is derived as Eq.(3.3).

$$\hat{i}_a = D \cdot \hat{i}_c + \hat{d} \cdot I_c \tag{3.3}$$

Essentially, the Eq. is an average model and it can be proved that is it accurate up to 1/2 f_{sw}. The instantaneous current relationship is given by Eq.(3.3) is valid as long as the PWM power converter works in continuous current mode, regardless of the implementation of the pulse-width modulator.

For the three-terminal switch under current mode control, since all the assumption used in deriving Eq.(3.1) is not violated, the small signal given by Eq.(3.3) is also true. This conclusion is verified by the Simplis simulation. Using peak current

mode control as an example, d to i_a transfer function obtained from simulation and average model are compared. From Eq.(3.3), an average model is written as:

$$\frac{\hat{i}_a}{\hat{d}} = D \cdot \frac{\hat{i}_c}{\hat{d}} + I_c \tag{3.4}$$

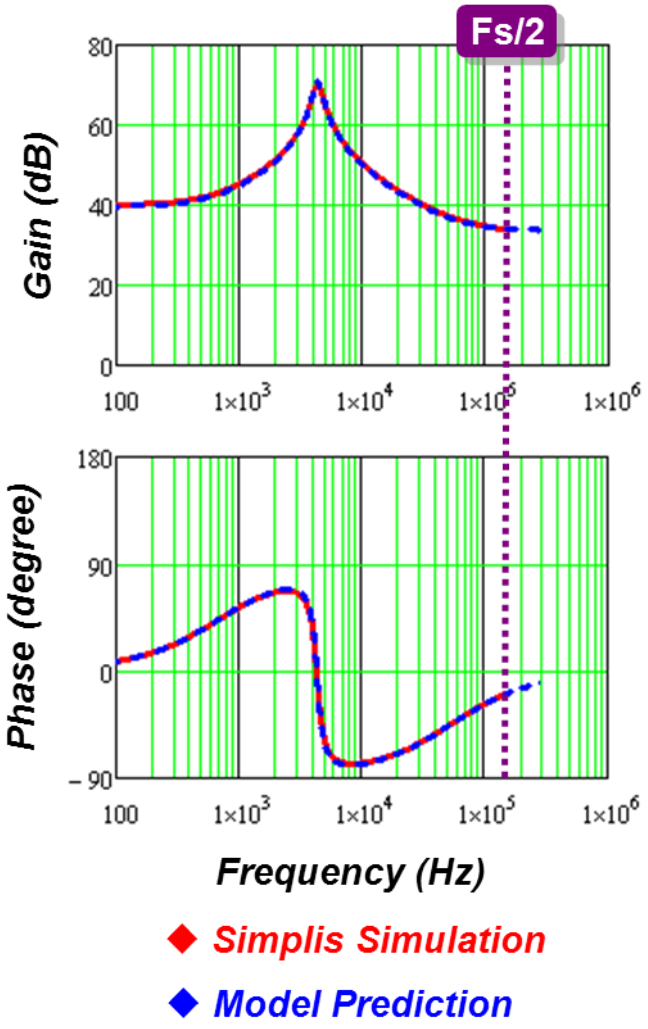


Figure 3.4 Duty cycle to switch current transfer function (fixed frequency modulation)

A similar comparison for constant on-time current mode control is shown in Figure 3.5.

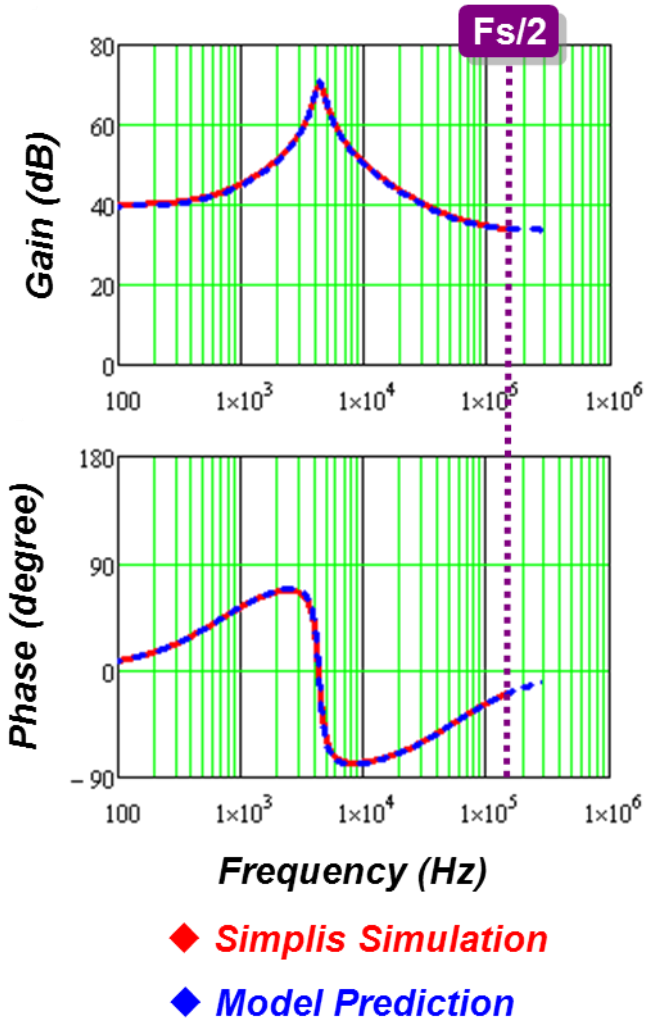


Figure 3.5 Duty cycle to switch current transfer function(variable frequency modulation)

From Figure 3.4 and Figure 3.5, it is shown that up to half of the switching frequency, small signal relationship Eq.(3.4) is a good approximation, including constant frequency modulation and variable frequency modulation current mode control.

3.3 Three-terminal Switch Model for Peak Current Mode Control

The small signal characteristic of the three-terminal switch is independent of the power converter topology. In this section, a Buck converter with peak current mode

control (Figure 3.6) is chosen as an example to illustrate development of the three-terminal switch model.

3.3.1 Review of Equivalent Circuit for Current Mode Control Buck Converter without Input Current Property

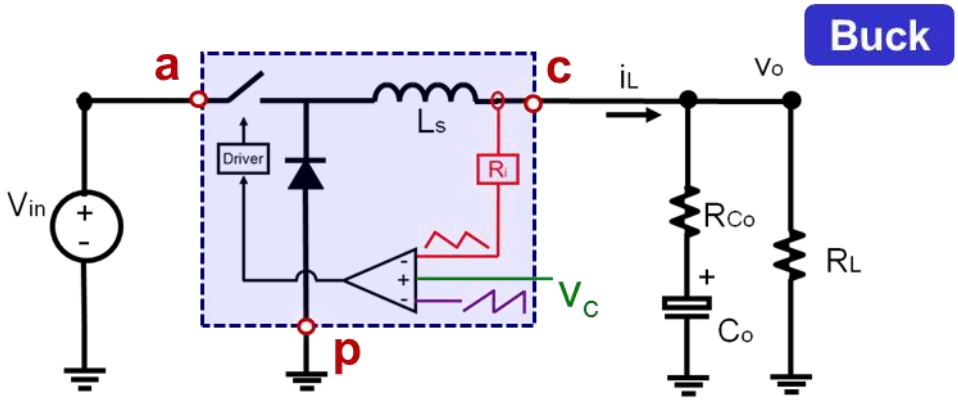


Figure 3.6 Current mode control Buck converter

Literature [70] proposes a modeling strategy that models a current mode control DC/DC converter based on continuous time model. It takes the Buck converter power stage and the closed current loop as an single entity, and uses describing function method to derive control to the output voltage transfer function $\hat{v}_o / \hat{v}_c$ and input to output transfer function $\hat{v}_o / \hat{v}_{in}$. This method is applicable not only to a constant frequency modulation current mode control, but also to a variable frequency modulation current mode control. The exact model derived by this method is accurate beyond the switching frequency.

For simplicity, literature [70] proposes an equivalent circuit to represents the control to output voltage transfer function $\hat{v}_o / \hat{v}_c$ and input to output transfer function $\hat{v}_o / \hat{v}_{in}$ for a current mode control Buck converter. The equivalent circuit model is good up to half of the switching frequency.

The equivalent circuit is shown in Figure 3.7.

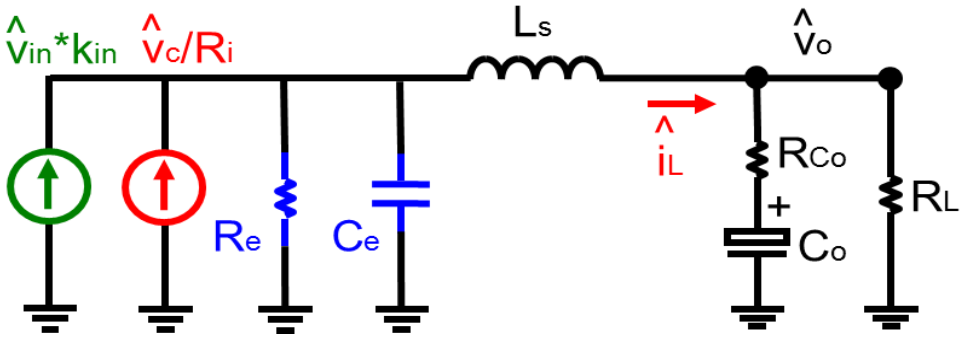


Figure 3.7 Equivalent circuit for current mode control Buck converter

In Figure 3.7, the parameters are defined as Table 3. 1:

Table 3. 1. Parameters Definition of Equivalent Circuit (Figure 3.7)

Peak current mode control		
$R_e = L_s / [T_{sw}(\frac{s_n + s_e}{s_n + s_f} - 0.5)]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{in} = \frac{D}{L_s}[\frac{1}{Q_2 \omega_2} - \frac{T_{off}}{2}]$
Valley current mode control		
$R_e = L_s / [T_{sw}(\frac{s_f + s_e}{s_n + s_f} - 0.5)]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{in} = \frac{D}{L_s}[\frac{1}{Q_2' \omega_2} + \frac{T_{on}}{2}]$
Charge control		
$R_e = L_s / [T_{sw}(\frac{L_s I_L}{V_{cp} T_{sw}} - \frac{D}{2} + \frac{s_e}{s_f}\frac{C_T}{T_{sw}})]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{in} = \frac{D}{L_s}[\frac{1}{Q_c \omega_2} + \frac{T_{on}}{2}]$
Constant on-time control		
$R_e = 2L_s / T_{on}$	$C_e = T_{on}^2 / (L_s \pi^2)$	$K_{in} = T_{on} / (2L_s)$
Constant off-time control		
$R_e = 2L_s / T_{off}$	$C_e = T_{off}^2 / (L_s \pi^2)$	$K_{in} \approx 0$

This equivalent circuit correctly represents the inductor current property under control signal perturbation and input voltage and output voltage perturbation, but switch current and diode current properties are lost.

To correctly represent the small signal behavior of the three-terminal structure (Figure 3.2), the equivalent circuit should have three terminals corresponding to the switch model. In such a three-terminal structure, if two terminal currents are correctly represented, the accuracy of the third terminal current is guaranteed by Kirchhoff's Current Law. Since the equivalent circuit in Figure 3.7 represents the inductor property, it is a good starting point when building the three-terminal equivalent circuit.

3.3.2 Complete Equivalent Circuit for Current Mode Control Buck Converter

The equivalent circuit Figure 3.7 accurately represents the property of the common terminal current. The strategy of deriving a three-terminal equivalent circuit is modifying the equivalent circuit in Figure 3.7, keeping the inductor current and adding a proper part to represent the active switch current. The correctness of the passive switch current property is guaranteed by Kirchhoff's Current Law.

The equivalent circuit is redrawn in Figure 3.8 with the introduction of a DC transformer with turns ratio D, which is the steady state duty cycle. On the secondary side, the inductor terminal is defined as c corresponding to the circuit diagram. On the primary side, the terminal a and p are defined by the corresponding circuit diagram. The $\hat{v}_{in}$ controlled current source $\hat{v}_{in} \cdot k_{in}$ in Figure 3.7 is equivalently represented by input voltage $\hat{v}_{in}$ together with an input voltage controlled voltage source $\hat{v}_{in} \cdot K_{ap}$, where K_{ap} is defined as:

$$K_{ap} = \frac{K_{in} \cdot R_e}{D} - \mathbf{1} \tag{3. 5}$$

Since C_e forms double poles with L_s at half the switching frequency, at low

frequency range, the DC transformer secondary side current ire is approximately equal to i_L. As a result, the primary side current is given by:

$$\hat{i}_{pri} \approx D \cdot \hat{i}_c \tag{3. 6}$$

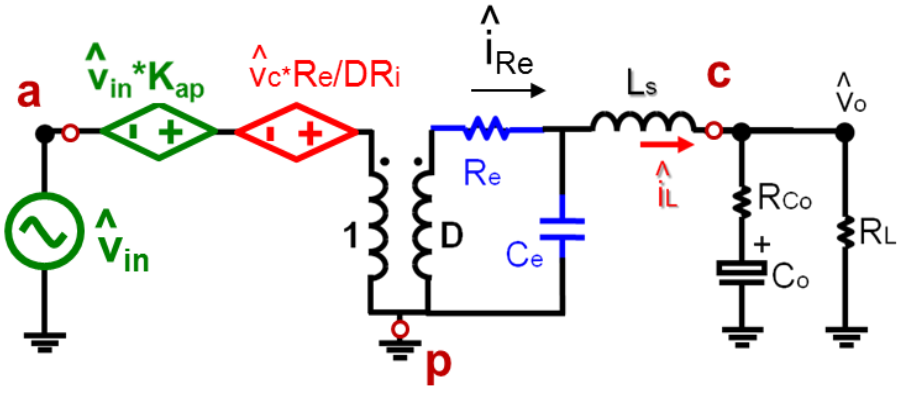


Figure 3.8 Equivalent circuit with DC transformer

Compare this equivalent circuit with the universal relationship between i_a and i_c, the term $D \cdot \hat{i}_c$ is represented by the DC transformer, but the missing term $\hat{d} \cdot I_c$ is not shown in the circuit. To correctly represent this relationship, a current source should be added between terminal a and p.

Under the small signal perturbation of control voltage $\hat{v}_c$ and the small signal perturbation of input voltage $\hat{v}_{in}$, as a response, the output voltage has a small signal perturbation $\hat{v}_o$. Using the modeling strategy used in [70], the three-terminal switch is taken as an entity. The describing function method is used to model control to the duty cycle transfer function. The duty cycle small signal modulation can be expressed by:

$$\hat{d} \approx v_c(s) \cdot \frac{L_s}{R_i \cdot V_{ap}} \cdot \frac{s}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} + v_{ap}(s) \cdot \frac{1}{V_{ap}} \frac{-D \cdot [1 + (T_{off}/2) \cdot s + s^2/\omega_2^2]}{1 + s/Q_2\omega_2 + s^2/\omega_2^2}$$
$$+ v_{cp}(s) \cdot \frac{1}{V_{cp}} \cdot \frac{1}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} \tag{3.7}$$

$$\text{where} \quad \omega_2 = \pi / T_{sw}, Q_2 = \frac{1}{\pi(\frac{s_n + s_e}{s_n + s_f} - 0.5)}$$

Based on Eq.(3.7), the $\hat{d} \cdot I_c$ term is expressed by:

$$\hat{d} \cdot I_c \approx v_c(s) \cdot \frac{L_s \cdot I_c}{R_i \cdot V_{ap}} \cdot \frac{s}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} + v_{ap}(s) \cdot \frac{I_c}{V_{ap}} \frac{-D \cdot [1 + (T_{off}/2) \cdot s + s^2/\omega_2^2]}{1 + s/Q_2\omega_2 + s^2/\omega_2^2}$$
$$+ v_{cp}(s) \cdot \frac{I_c}{V_{ap}} \cdot \frac{1}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} \tag{3.8}$$

In the small signal equivalent circuit Figure 3.8, under small signal perturbation of control voltage $\hat{v}_c$, and the small signal perturbation of input voltage $\hat{v}_{ap}$, the output voltage small signal perturbation is $\hat{v}_{cp}$. Then, the inductor voltage small signal response $\hat{v}_L$ can be easily obtained:

$$\hat{v}_L = v_c(s) \frac{L_s}{R_i} \cdot \frac{s}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} + v_{ap}(s)[\frac{[1/Q_2\omega_2 - (T_{off}/2)\cdot]D \cdot s}{1 + s/Q_2\omega_2 + s^2/\omega_2^2}]$$
$$+ v_{cp}(s) \cdot [\frac{1}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} - 1] \tag{3.9}$$

When compare Eq.(3.8) and Eq.(3.9), it is found that they have similar dynamic terms. So, the equation for $\hat{d} \cdot I_c$ can be rearranged and expressed by $\hat{v}_L$ in a simple way:

$$\hat{d} \cdot I_c = \frac{I_c}{V_{ap}} \{v_c(s) \cdot \frac{L_s}{R_i} \cdot \frac{s}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} + v_{ap}(s) \frac{[1/Q_2\omega_2 - (T_{off}/2)\cdot]D \cdot s}{1 + s/Q_2\omega_2 + s^2/\omega_2^2}$$
$$+ v_{cp}(s) \cdot [\frac{1}{1 + s/Q_2\omega_2 + s^2/\omega_2^2} - 1]\} + v_{cp}(s) \cdot \frac{I_c}{V_{ap}} + v_{ap}(s)/(-\frac{V_{ap}}{D \cdot I_c})$$
$$= \hat{v}_L \cdot G_L + \hat{v}_{cp} \cdot G_{cp} + \hat{v}_{ap}/R_{ap} \tag{3.10}$$
$$\text{where} \quad G_L = G_{cp} = \frac{I_c}{V_{ap}}, R_{ap} = -\frac{V_{ap}}{DI_c}$$

According to Eq.(3.10), the equivalent circuit Figure 3.8 is modified to represent the switch current. Three branches corresponding to the terms in Eq.(3.10) are added

between terminal a and terminal p. The complete equivalent circuit for the peak current mode control Buck converter is Figure 3.9.

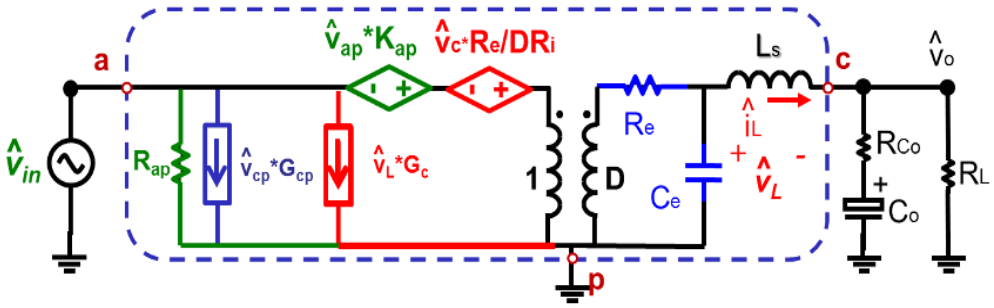


Figure 3.9 Complete equivalent circuit for peak current mode control Buck converter

3.3.3 Three-terminal Switch Mode for Peak Current Mode Control

Comparing the circuit diagram with the small signal equivalent circuit, the linear part in the circuit is kept the same as in the equivalent circuit, and the common three-terminal structure is replaced by a three-terminal equivalent circuit. Since the previous derivation is independent of topology, this three-terminal equivalent circuit is the small signal equivalent circuit for the common structure. The three terminal equivalent circuit model for the peak current mode control is shown in Figure 3.10.

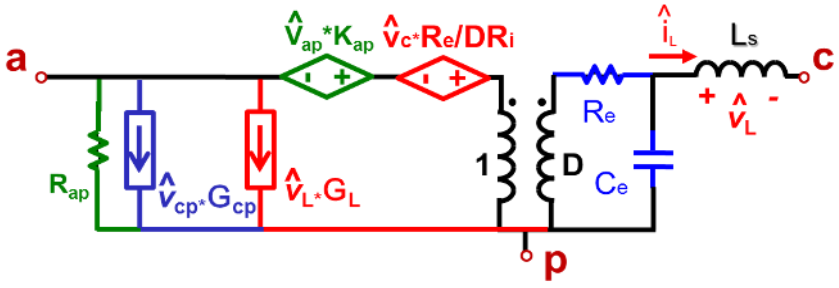


Figure 3.10 Three terminal equivalent circuit model for peak current mode control

3.4 Discussion on Physical Meaning of Three-Terminal Switch Model

Clear physical meaning can be found based on the equivalent circuit model. In practical design range (with small external ramp), R_e is a relatively large resistor. The power stage double poles formed by L_s and C_o are split. One pole moves to a lower frequency. That's the reason why the system behaves like a first order system in low-frequency range. The other pole moves to high-frequency and combines with a high-frequency pole, resulting in a double pole at half of the switching frequency. For a duty cycle larger than 0.5 case, R_e becomes negative which makes the double move to the right half of the plane and predicts sub-harmonic oscillations.

If a large external ramp is added to the current loop, the current control effect is weakened. For the external ramp $s_e >> s_n, s_f$, R_e is reduced to a negligible value (3.12). High frequency double poles split and the power stage filter double poles recover. Since R_e is very small, the pole related to R_e and C_e is much higher than 1/2 the switching frequency. As a low frequency model, C_e is negligible in this case.

$$R_e \approx \frac{L_s}{T_{sw}} \frac{s_n + s_f}{s_e} \approx \mathbf{0} \tag{3.11}$$

With $s_e >> s_n, s_f$, parameters K_{ap}, $\hat{v}_c \cdot \frac{R_e}{D \cdot R_i}$ and the primary current branch $\frac{\hat{v}_{ap}}{R_{ap}} + \hat{v}_{cp} \cdot G_{cp} + \hat{v}_L \cdot G_L$ can be simplified as Eq.(3.12)~Eq.(3.14).

$$K_{ap} = -\frac{D'}{\mathbf{2}T_{sw}} \frac{s_n + s_f}{s_e} \approx \mathbf{0} \tag{3.12}$$

$$\hat{v}_c \cdot \frac{R_e}{D \cdot R_i} \approx (\hat{v}_c \cdot \frac{\mathbf{1}}{T_{sw} s_e}) \frac{V_{in}}{D} = \hat{d} \cdot \frac{V_{in}}{D} \tag{3.13}$$

$$\frac{\hat{v}_{ap}}{R_{ap}} + \hat{v}_{cp} \cdot G_{cp} + \hat{v}_L \cdot G_L = \hat{d} \cdot I_c \tag{3.14}$$

Based on Eq.(3.12)~Eq.(3.14), an important property is revealed: the equivalent

circuit is a unified model showing the unification of the current mode control and voltage control. With the external ramp increase, the current control effect is weakened. If $s_e >> s_n, s_f$, current feedback information is negligible, the three-terminal switch mode for current mode control degenerates to a three-terminal switch mode for the power stage [42], as shown in Figure 3.11.

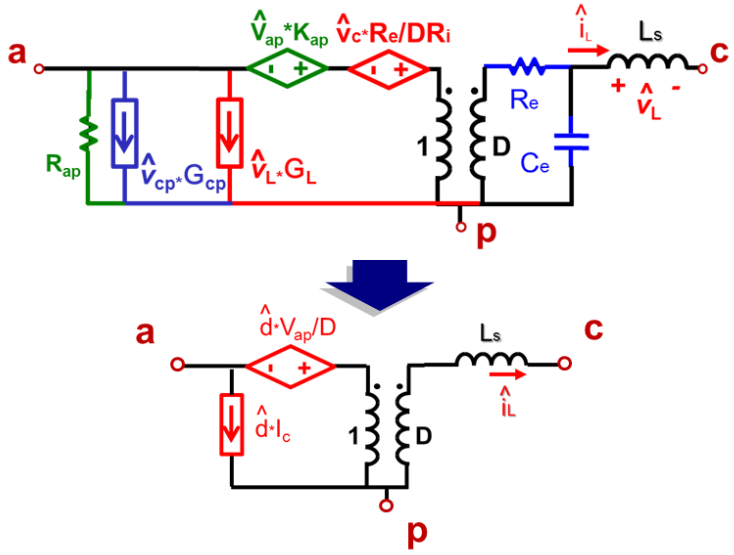


Figure 3.11 Three terminal equivalent circuit model degenerates to three-terminal switch mode for the power stage when $s_e >> s_n, s_f$

3.5 Model Extension to Other Current Mode Controls

The proposed modeling strategy can be used for other types of current-mode control structures, including valley current-mode control, charge control and constant on-time control and constant off-time control structures. For constant frequency modulation, an external ramp with slope s_e is added to help stabilize the current loop. For constant on-time control and constant off-time control, since no external ramp is needed to stabilize the current loop, the external ramp is not considered in the model. The circuit parameters are shown in Table 3. 2.

For constant frequency modulation current mode controls, the resonant frequency of L_s and C_e is located at half of the switching frequency, and the resistance of R_e

could be positive or negative, depending on the duty cycle and load current. Negative R_e indicates that the current loop is unstable, suffer to sub-harmonic oscillation. Using an external ramp can help to stabilize the current loop and achieve a proper damping of the double poles at half of the switching frequency.

For variable frequency modulation current mode control, the resonant frequency of L_s and C_e is located at a certain frequency higher than half of the switching frequency, which is determined by T_{on} or T_{off}, and the resistance of R_e is always positive. This circuit can be used to illustrate the instability of the current loop. The key transfer functions, including the control-to-output transfer function, the audio susceptibility, and the input impedance and output impedance, can be easily calculated based on the equivalent model.

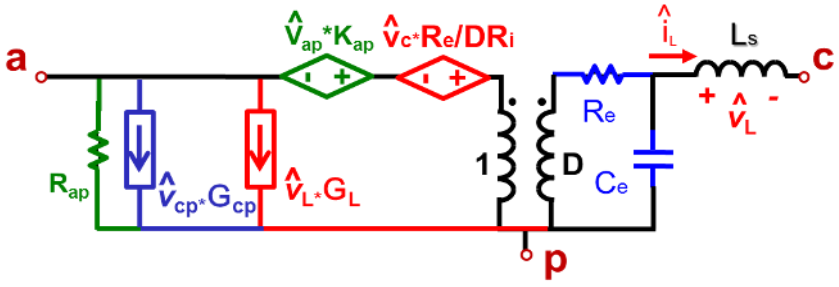


Figure 3.12 Unified three terminal equivalent circuit model for current mode controls

Table 3. 2 Parameters Definition of Three-terminal Switch Model (Figure 3.12)

Peak current mode control		
$R_e = L_s / [T_{sw}(\frac{s_n + s_e}{s_n + s_f} - 0.5)]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = -\frac{T_{off}}{2L_s} R_e$
Valley current mode control		
$R_e = L_s / [T_{sw}(\frac{s_f + s_e}{s_n + s_f} - 0.5)]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = \frac{T_{off}}{2L_s} R_e$
Charge control		

$R_e = L_s / [T_{sw}(\frac{L_s I_L}{V_{cp} T_{sw}} - \frac{D}{2} + \frac{s_e}{s_f}\frac{C_T}{T_{sw}})]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = \frac{T_{on}}{2L_s} R_e$
Constant on-time control		
$R_e = 2L_s / T_{on}$	$C_e = T_{on}^2 / (L_s \pi^2)$	$K_{ap} = T_{off} / T_{on}$
Constant off-time control		
$R_e = 2L_s / T_{off}$	$C_e = T_{off}^2 / (L_s \pi^2)$	$K_{ap} \approx -1$

3.6 Simulation Verification of the Proposed Model

The proposed small signal model is verified in this section. The SIMPLIS simulation tool is used to verify the proposed model.

3.6.1 Constant Frequency Modulation Current Mode Control

A. Peak current mode control Buck converter

The parameters of the peak current-mode control buck converter are as follows: V_{in} = 12V, V_o = 5V, f_s = 300KHz, C_o = 8×560μF, R_{Co} = 6/8mΩ, and L_s =300nH. The control-to-output transfer function and the audio susceptibility are shown in Figure 3.13 while input and output impedance comparisons are shown and Figure 3.14. The proposed model can accurately predict the system response up to half of the switching frequency.

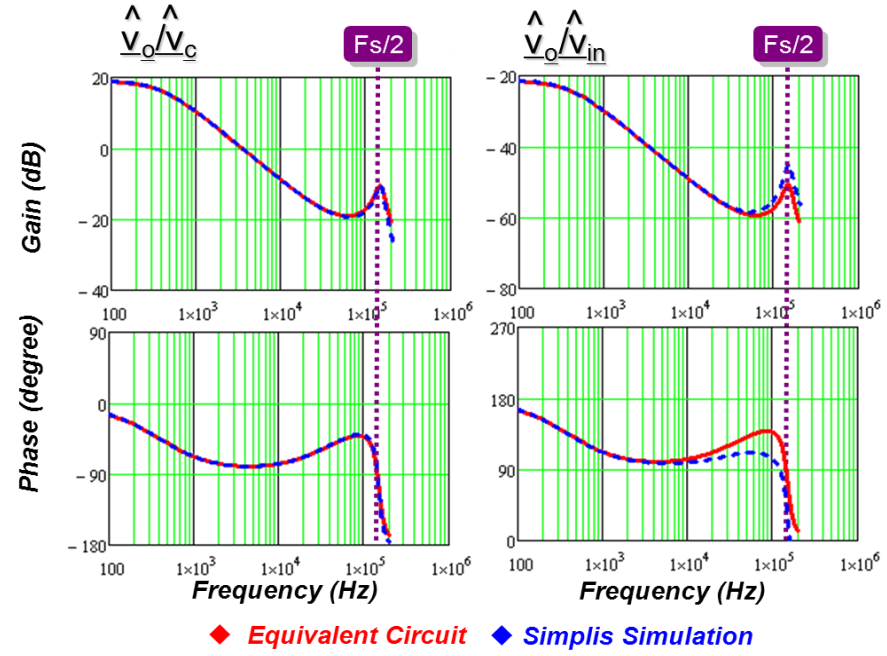


Figure 3.13 Simulation verification of control-to-output and input-to-output transfer function for peak current mode control Buck converter

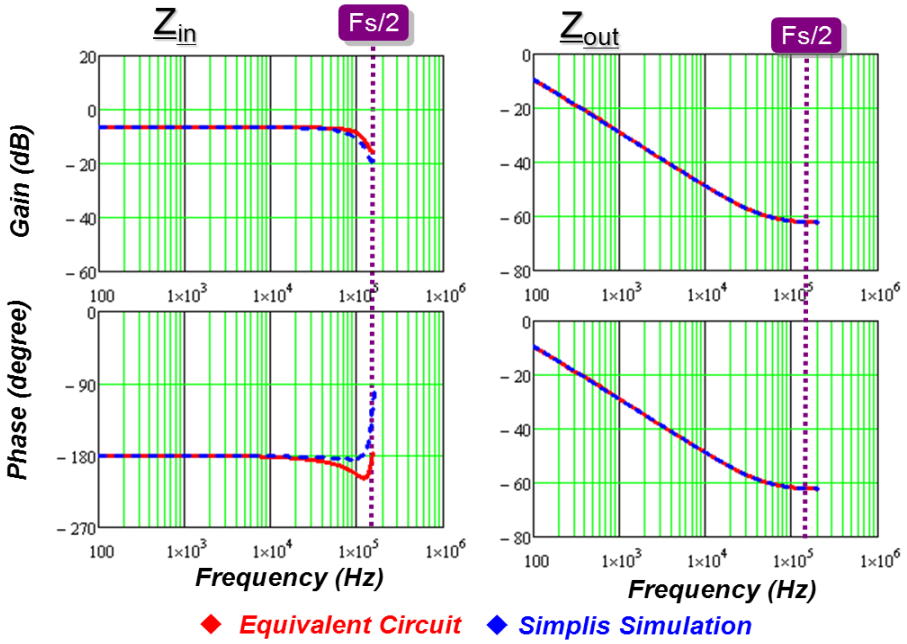


Figure 3.14 Simulation verification of output impedance and input impedance for peak current mode control Buck converter

B. Peak current mode control Boost converter

The circuit diagram and the small signal equivalent circuit of the Boost converter are shown in Figure 3.15. The parameters of the peak current-mode control Boost converter are as follows: V_{in}=220V, V_o=400V, R_L=150Ω, f_{sw}=100kHz, L_s=300μH, ESR=3mΩ. The control-to-output transfer function and the audio susceptibility are shown in Figure 3.16 while the input and output impedance comparisons are shown in Figure 3.17. The proposed model can accurately predict the system response up to half of the switching frequency.

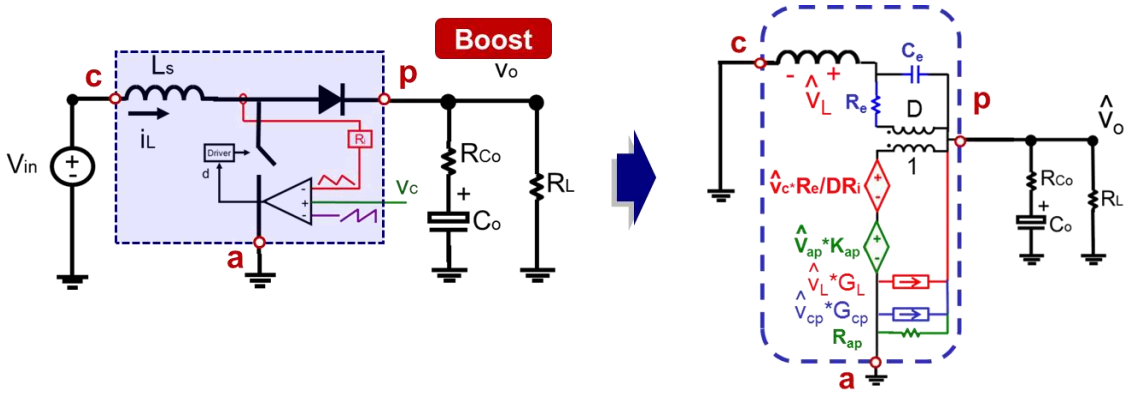


Figure 3.15 Peak current mode control Boost converter and its small signal equivalent circuit

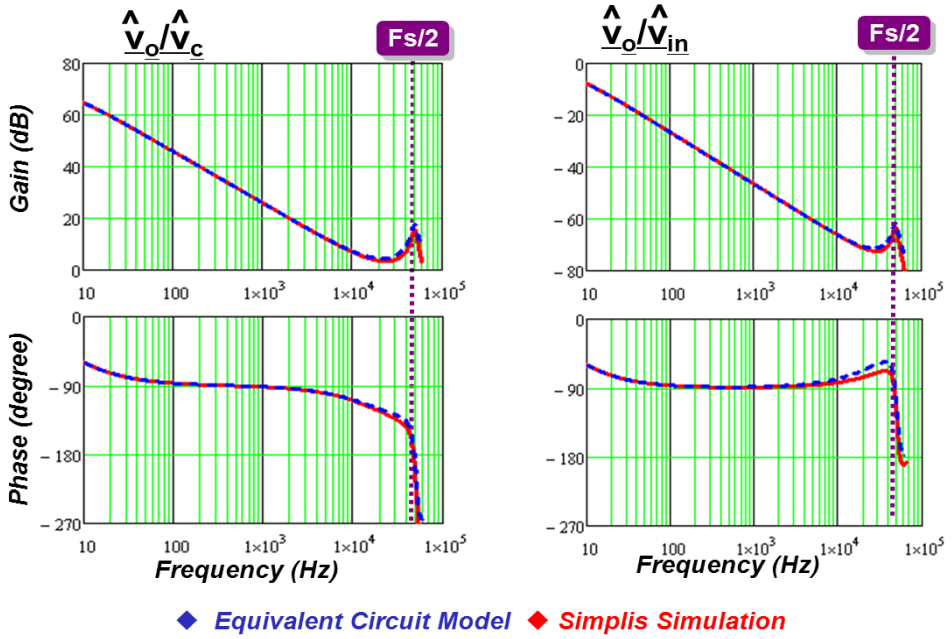


Figure 3.16 Simulation verification of control-to-output and input-to-output transfer function for peak current mode control Boost converter

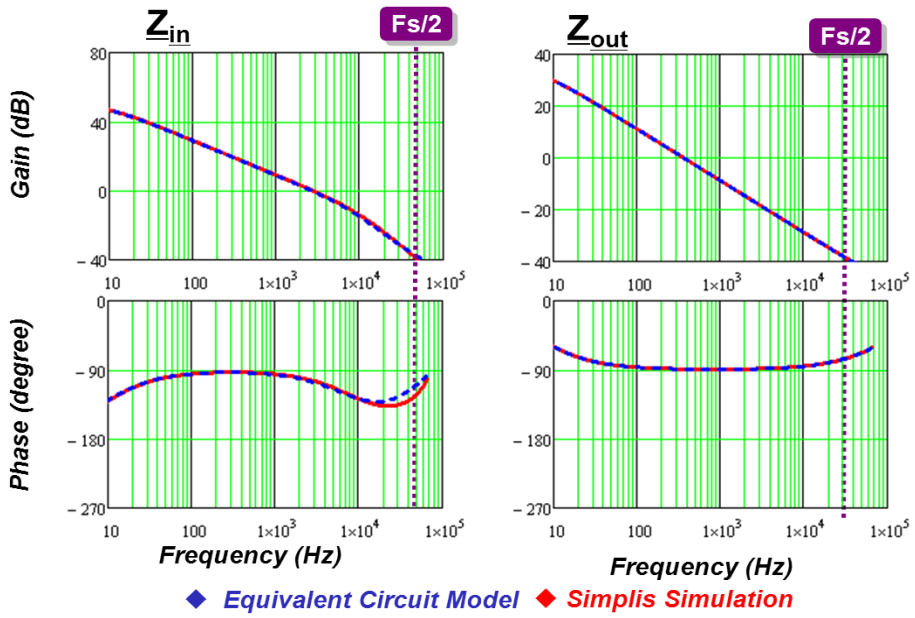


Figure 3.17 Simulation verification of output impedance and input impedance for peak current mode control Boost converter

C. Charge control Flyback converter

The circuit diagram and small signal equivalent circuit of the Flyback converter are shown in Figure 3.18. The parameters of the charge control Flyback converter are as follows: V_{in}=500V, V_o=400V, R_L=150Ω, f_{sw}=100kHz, L_s=300μH, ESR=3mΩ. The control to input current transfer function and the control to output are shown in Figure 3.19. The proposed model can accurately predict the system response up to half of the switching frequency. As the purpose of charge control, the control to input current transfer function is a flat gain up to half of the switching frequency.

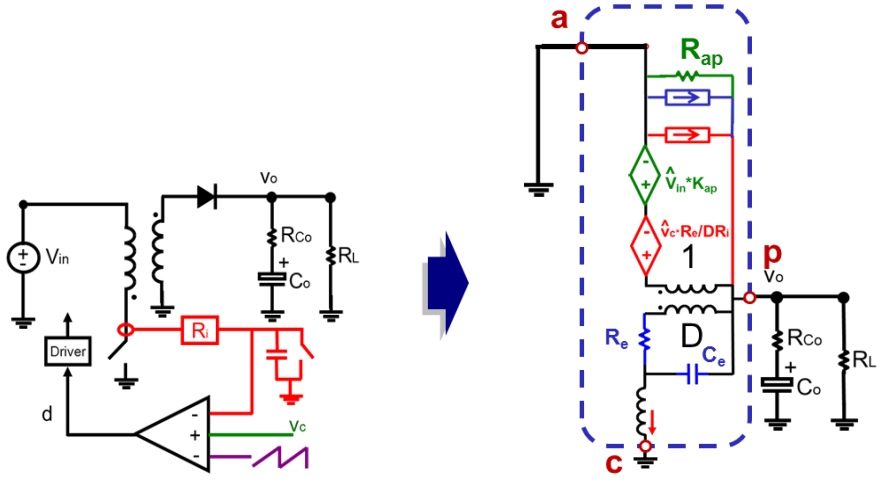


Figure 3.18 Charge control Flyback converter and its small signal equivalent circuit control

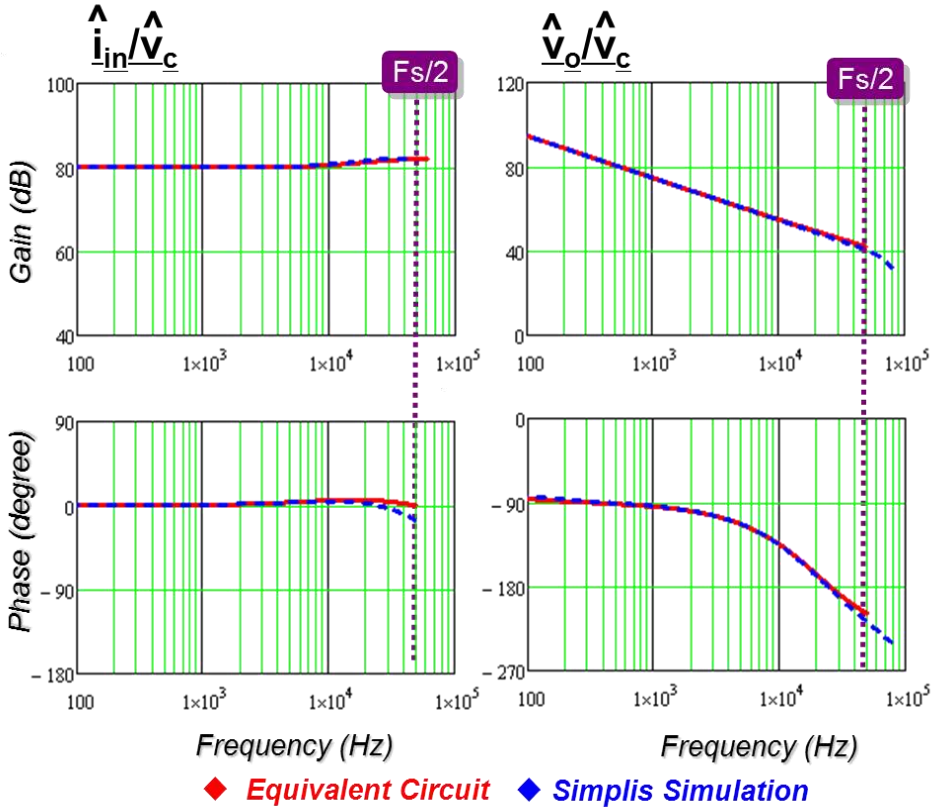


Figure 3.19 Simulation verification of control-to-input current and control-to-output transfer function for charge control Flyback converter

3.6.2 Variable Frequency Modulation Current Mode Control

The SIMPLIS simulation tool is used to verify the proposed model for constant on-time current-mode control. The parameters of the buck converter are as follows: V_{in}=12V, V_o=1.2V, R_L=100mΩ, T_{on}=333nS,L_s=300μH, C_o = 8×560μ F, R_{Co} = 6/8m Ω , and L_s=300nH. The control-to-output transfer function and the audio susceptibility are shown in Figure 3.20 while input and output impedance comparisons are shown in Figure 3.21. The proposed model can accurately predict the system response.

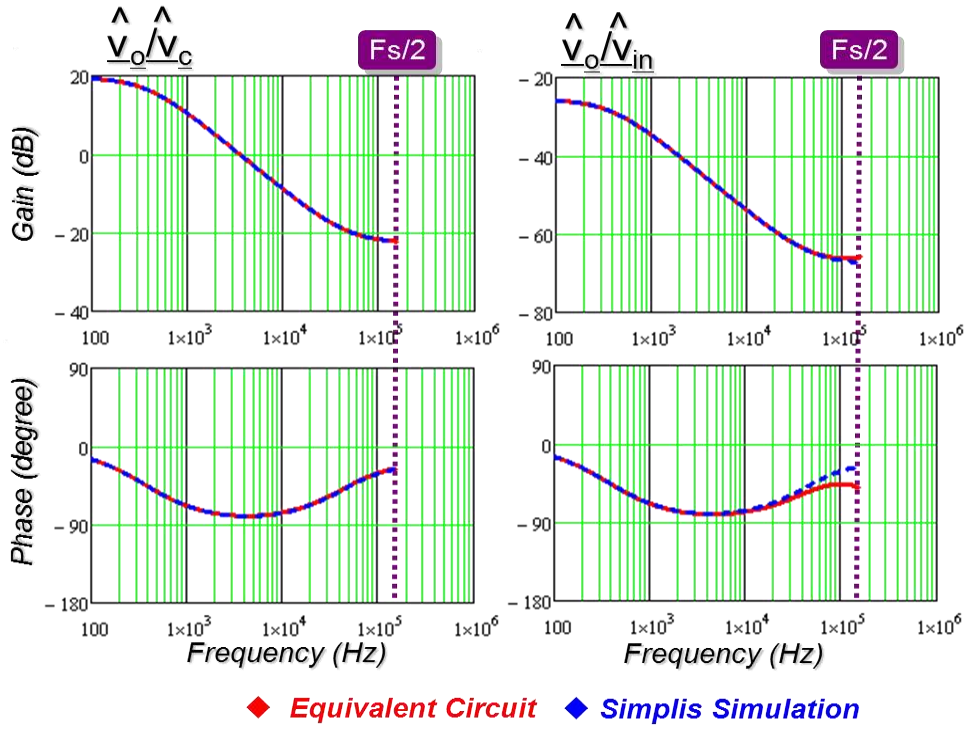


Figure 3.20 Simulation verification of control-to-output and input-to-output transfer function for constant on-time current mode control Buck converter

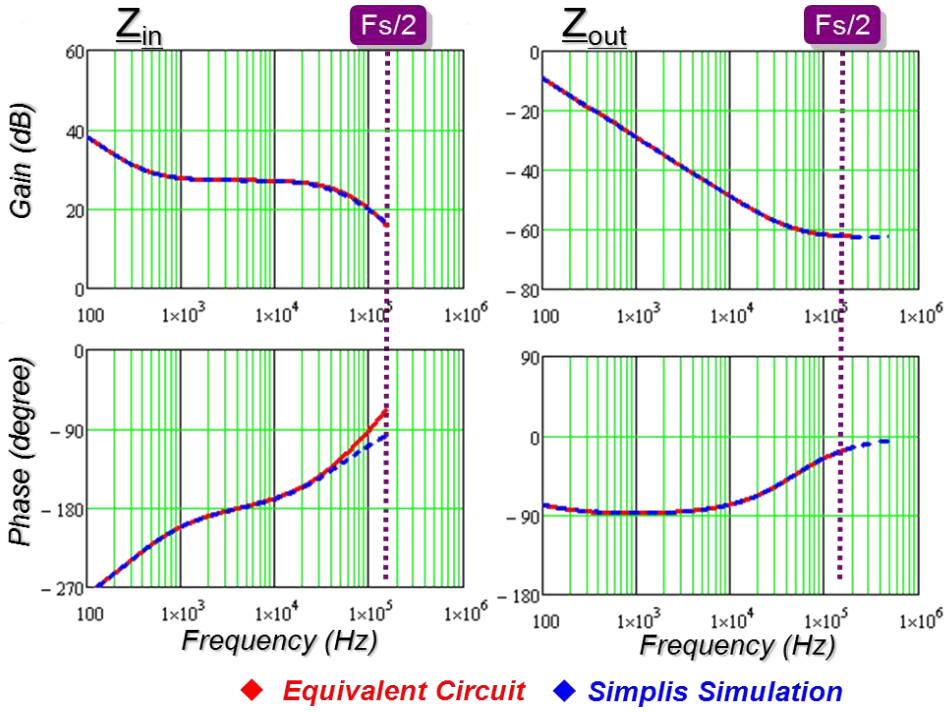


Figure 3.21 Simulation verification of input impedance and output impedance for constant on-time current mode control Buck converter

3.7 Summary

This chapter presents a unified three-terminal switch model for current mode controls. Based on the observation, the PWM switch and the closed current loop is taken as an invariant sub-circuit which is common to different DC/DC converter topologies. The basic small signal relationship is studied and the result shows that the PWM switch with current feedback preserve the property of PWM switch. A three-terminal equivalent circuit is developed to represent the small signal behavior of this common sub-circuit. The proposed model is a unified model that is applicable in both constant frequency modulation and variable frequency modulation. The physical meaning of the three-terminal equivalent circuit model is discussed. The model are verified by SIMPLIS simulation in commonly used converters for both constant frequency modulation and variable frequency modulation.

Chapter 4. Comparison of Current Mode Controls with Different Implementation Based on Proposed Model

In this section, based on the small signal model obtained in chapter 3, a comparison of current mode controls with different implementation is discussed. According to application requirement and operating condition, different implementations exhibit their own unique advantage. The application of charge control is mainly on the application needed to control input current. The discussion compares peak current mode control, valley current mode control, constant on-time control and constant off-time control implementation, which are most commonly used in DC/DC converter design[29][72][73][74][75].

The discussion is based on a current mode control Buck converter with different implementation.

4.1 Control-to-output Transfer Function and Voltage Loop Design

Based on the equivalent circuit model, control-to-output transfer function of all the current mode control can be expressed by a unified form:

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = K_c \frac{(1 + R_{Co}C_o s)}{1 + s/\omega_a} \frac{1}{1 + \frac{s}{Q_x \omega_x} + \frac{s^2}{\omega_x^2}} \tag{4.1}$$

With different implementation, low frequency pole are similar: the position is determined by the load resistor and output capacitor.

High frequency double poles are fundamentally different:

For constant frequency modulation current mode control, the double poles are half of the switching frequency:

$$\omega_x = \frac{\mathbf{1}}{\mathbf{2}} \cdot \mathbf{2}\pi \cdot f_{sw} = \pi \cdot f_{sw} \tag{4.2}$$

Proper design of the external ramp can guarantee the quality factor around 1. For peak current mode control, for D>0.5 case, an external ramp is necessary to stabilize the current loop. In contrast, for valley current mode control, external ramp is necessary for D<0.5 application.

For constant on-time control, the double poles locations are determined by on-time:

$$\omega_x = \frac{\pi}{T_{on}} \tag{4.3}$$

The double poles quality factor is a constant value:

$$Q_x = \frac{\mathbf{2}}{\pi} \tag{4.4}$$

For constant off-time control, the double poles locations are determined by Off-time:

$$\omega_x = \frac{\pi}{T_{off}} \tag{4.5}$$

The double poles quality factor is also a constant value:

$$Q_x = \frac{\mathbf{2}}{\pi} \tag{4.6}$$

This characteristic is the basis of selecting the implementation of current mode control.

For a small duty cycle application, such as voltage regulator for microprocessor [20], the duty ration is only around 0.1 so peak current mode control does not need an external ramp to achieve a proper double pole damping while it is necessary for valley current mode control. It is obvious that peak current mode control is simpler to implement. Based on Eq.(4.3)(4.5), the double poles of constant on-time control are around 5 times of the switching frequency, while those of constant off-time control are around half the switching frequency. The pole-zero-map Figure 4.1 clearly shows the difference between them.

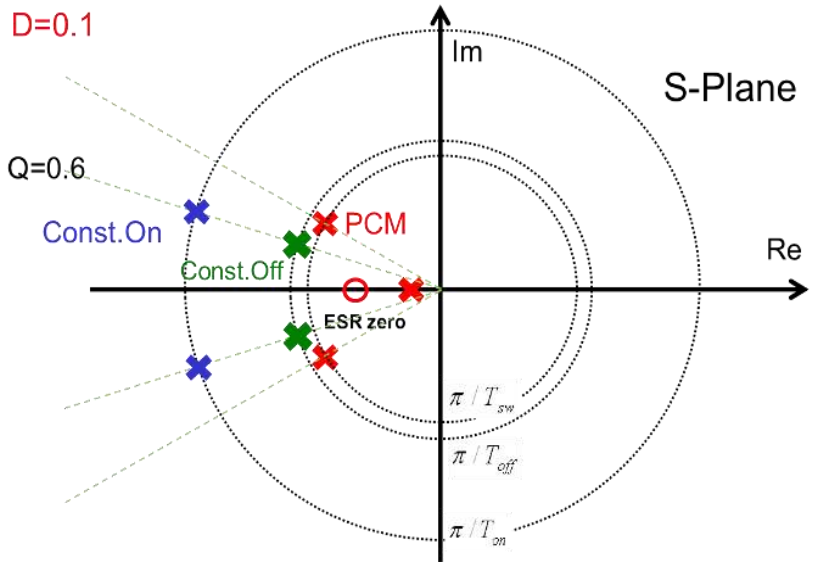


Figure 4.1 Pole-zero map comparison in low duty cycle case

Figure 4.2 shows the bode plots of control-to-output transfer functions for these implementations. Due to the small duty cycle, the curve of constant-off time almost overlaps the curve of peak current mode control. Around half switching frequency, the double poles cause 180° phase delay. In contrast, the phase curve of constant on-time control exhibits no phase drop, and is even boosted up by ESR zero.

This characteristic provides a significant benefit in high bandwidth design. High control bandwidth is a desirable property in most Point-of-load converters and voltage regulators. It can help to improve dynamic response, save output capacitors and footprint.

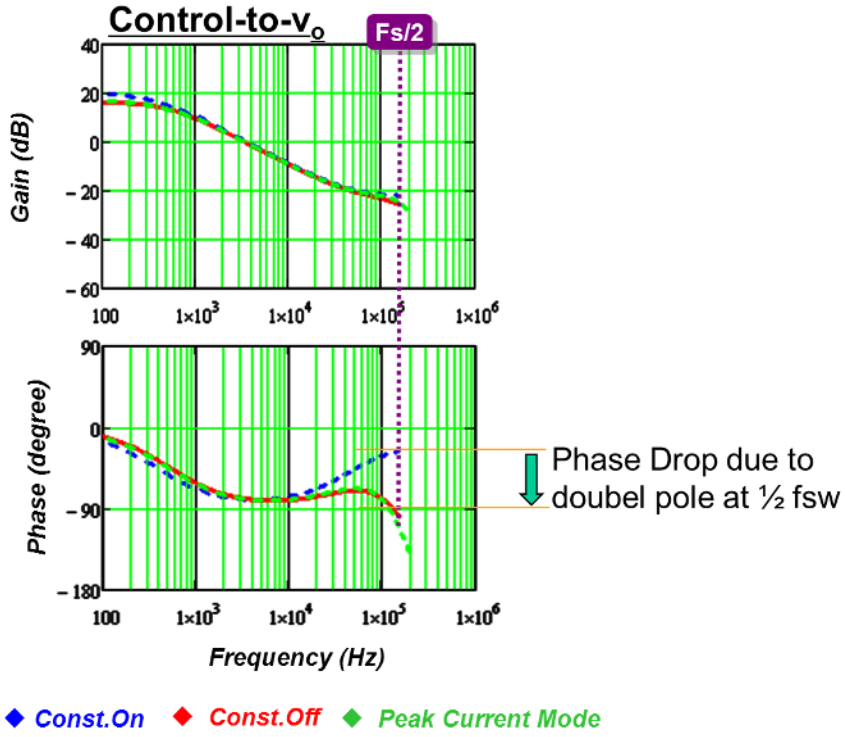


Figure 4.2 Control-to-output transfer function comparison

T_2 is the outer loop gain with the inner loop closed. With the proposed equivalent circuit, T_2 is defined as the loop shown in Figure 4.3. Figure 4.4 is the comparison of T_2 bandwidth for the same Buck converter except with different current mode control implementation. The parameters of the power stage are: V_{in}=12V, V_o = 1.2V, f_{sw} = 300kHz, L_s = 300nH, C_o =4.48mF, and R_{Co} = 0.75mΩ. From Figure 4.4, we can see that with the same required phase margin, constant on-time control can achieve 100kHz bandwidth, which is 1/3 of the switching frequency, while peak current mode and constant off-time control can only achieve 1/5 of the switching frequency bandwidth. So, constant on-time is better than constant off-time in high bandwidth design. However, for a multi-phase interleaving application, although peak current mode control is not as good as constant on-time control in high bandwidth design, the implementation of interleaving is easier and no extra circuitry is needed.

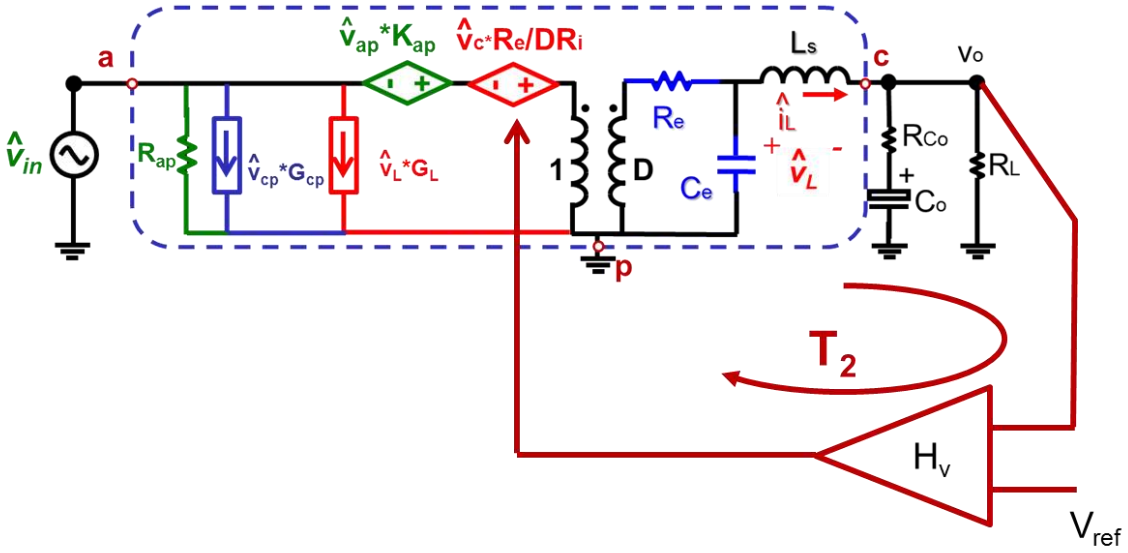


Figure 4.3. Equivalent circuit of Buck converter with outer feedback loop

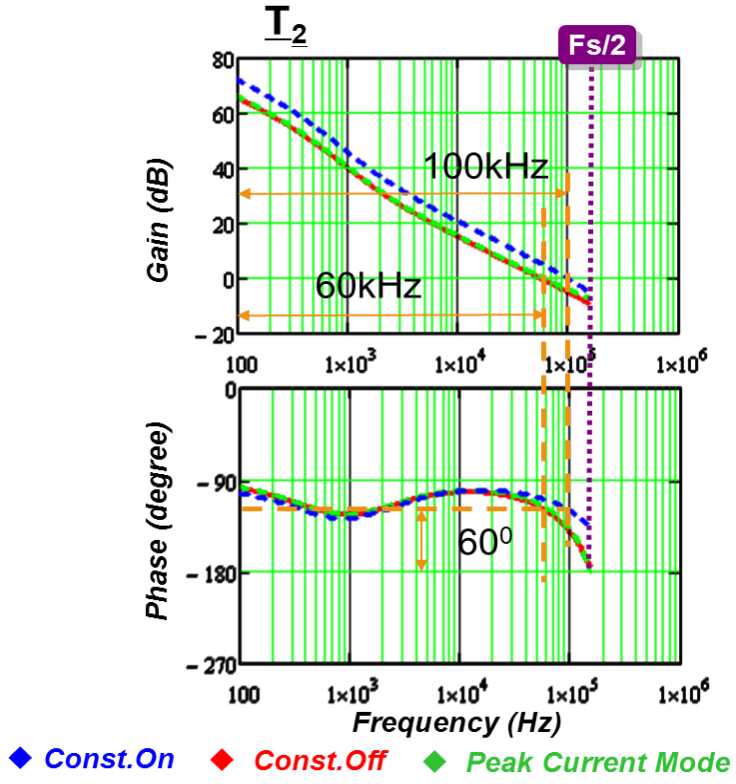


Figure 4.4 T_2 loop gain comparison: constant on-time, constant off-time and peak current mode control

The large duty cycle application has the opposite case, as shown in the

pole-zero-map Figure 4.5. Valley current mode control does not need an external ramp to achieve the proper double pole damping. Double poles of valley current mode control are at half switching frequency, while those of constant off-time control are at a much higher frequency. The pole-zero-map Figure 4.5 clearly shows the difference between them. The parameters of the power stage are: V_{in}=5.2V, V_o=5V, R_L=2.5Ω, C_o=440μF, ESR=50mΩ,f_{sw}=100kHz.

Figure 4.6 is the comparison of the T_2 bandwidth for the same Buck converter with different current mode control implementation. With the same required phase margin, constant off-time control has widest bandwidth.

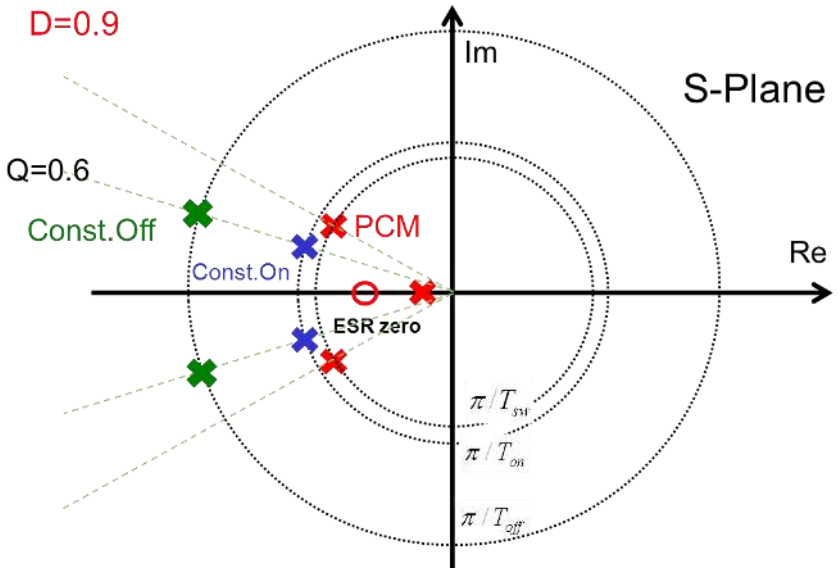


Figure 4.5 Pole-zero map comparison in large duty cycle case

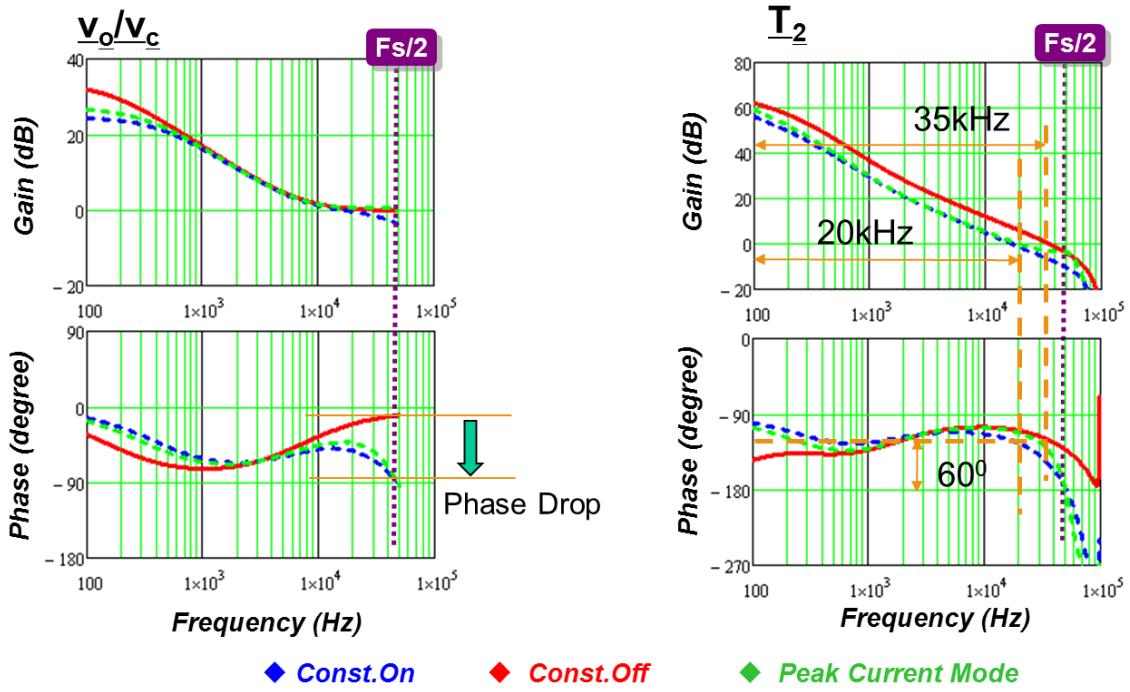


Figure 4.6 T_2 loop gain comparison: constant on-time, constant off-time and valley current mode control

4.2 Audio susceptibility

Based on the equivalent circuit model, input-to-output transfer function of all the current mode controls can be expressed by a unified form:

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} \approx K_{audio} \frac{(1+R_{Co}C_o s)}{1+s/\omega_a} \frac{1}{1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}}$$

$$K_{audio} = \frac{D(1+K_{ap})R_L}{R_e+R_L} \tag{4. 7}$$

where

With different implementation, the most meaningful difference is the gain coefficient K_{audio} of this transfer function.

For different implementations of the current mode control, as mentioned in Table 3. 2, K_{ap} is defined as:

Peak Current Mode Control:

$$K_{ap} = -\frac{T_{off}}{2L_s} \cdot R_e \tag{4. 8}$$

Valley Current Mode Control:

$$K_{ap} = \frac{T_{on}}{2L_s} \cdot R_e \tag{4. 9}$$

Constant on-time Current Mode Control:

$$K_{ap} = \frac{T_{off}}{T_{on}} \tag{4. 10}$$

Constant off-time Current Mode Control:

$$K_{ap} = -1 \tag{4. 11}$$

It is easy to simplify the expression of K_{audio} for different current mode control:

Peak Current Mode Control:

$$K_{audio} = \frac{D(1 - D'Q_2\pi/2)R_L}{R_e + R_L} \tag{4. 12}$$

Valley Current Mode Control:

$$K_{audio} = \frac{D(DQ_2'\pi/2 + 1)R_L}{R_e + R_L} \tag{4. 13}$$

Constant on-time Current Mode Control:

$$K_{audio} = \frac{R_L}{R_e + R_L} \tag{4. 14}$$

Constant off-time Current Mode Control:

$$K_{audio} = 0 \tag{4. 15}$$

Among these implementations, the gain K_{audio} of valley current mode control and

constant on-time control is always positive, so it is impossible to achieve zero audio susceptibility.

For peak current mode control, to make K_{audio}=0, the external ramp should be:

$$s_e = \mathbf{0.5} s_f \tag{4. 16}$$

However, this design criteria contradicts with the criteria of damping the control to output transfer function's high frequency double poles. To achieve proper damping, namely, quality factor of the double poles equals to 1, the external ramp should be:

$$s_e \approx \mathbf{0.82} \cdot s_f - \mathbf{0.18} \cdot s_n \tag{4. 17}$$

These two criteria are compatible with each other only in the case where duty cycle D is around 0.2 to 0.4. As a result, with peak current mode control implementation, null audio susceptibility is not achievable for all operating duty cycle.

For constant off-time current mode control, since K_{audio}=0 as an inherent property, without external ramp design concern, it is the best current mode control implementation if low audio susceptibility is a tight requirement in some designs. This property is provided by the unique "feed-forward effect" of constant off-time current mode control. As an inherent effect of the current loop, K_{ap}=-1 is a pure gain, so it can immediately respond to the input variation and cancel the impact of it.

Figure 4.7 shows a time domain simulation waveform. Under a line frequency perturbation, the feed-forward effect modulates the duty cycle proportionally without any delay. As a result, the output voltage is not influenced by the input voltage even without voltage feedback. This is a significant benefit of constant off-time current mode control for the application requiring fast input transient response.

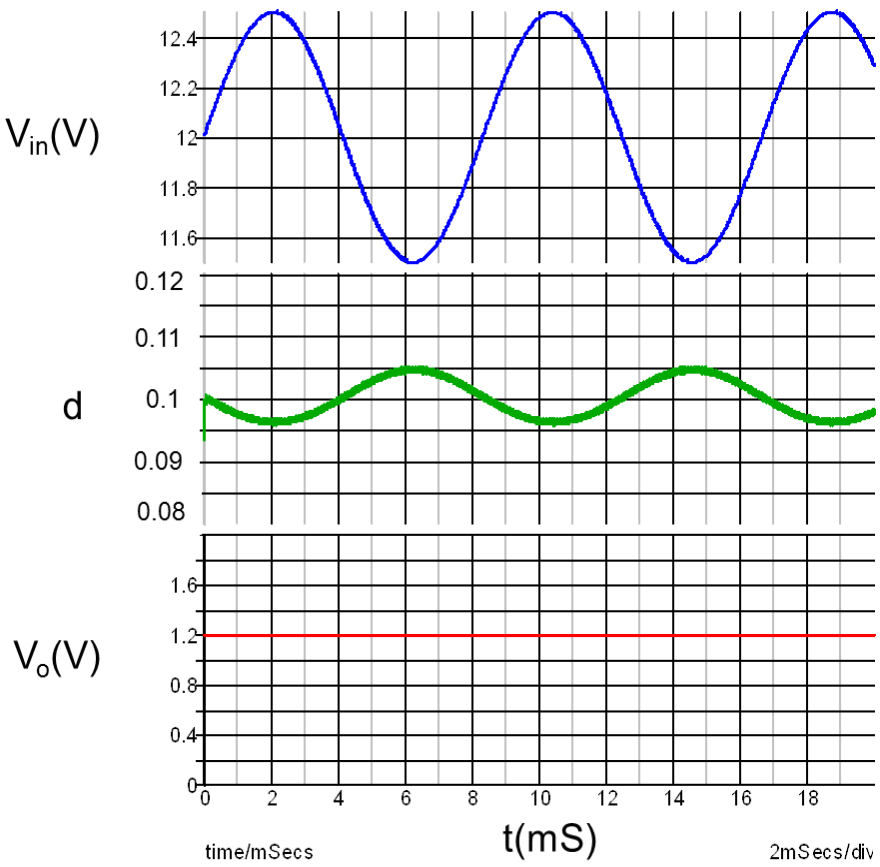


Figure 4.7 Simulation result of constant off-time control under input perturbation

4.3 Output Impedance and Adaptive-voltage-positioning Design

In this section, the property of output impedance for different current mode control Buck converter will be discussed. Based on their characteristic in small signal model, adaptive-voltage-positioning (AVP) designs for different implementations are compared.

As the name implies, the purpose of current mode control is to control the inductor current of the power converter, in another word, converter the inductor to be a current source. Consider a Buck converter, as the inductor is like a high impedance current source, the output impedance with closed current loop is dominated by the

output capacitor. However, current mode controls can not make the inductor as an ideal current source since only the peak or valley value of the inductor current, rather than the average current, as a result, the output impedance of the current source is not infinite value at low frequency range.

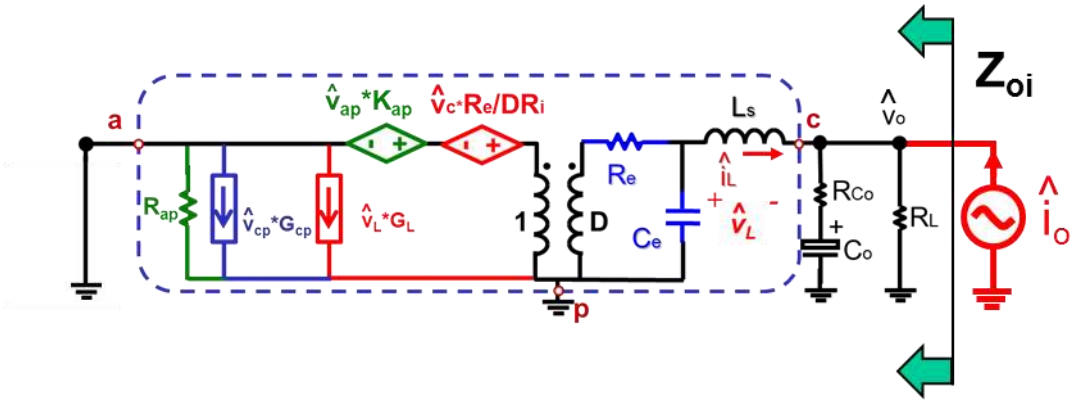


Figure 4.8 Definition of output impedance with closed current loop

The analytical expression of the output impedance with closed current loop can be obtained from equivalent circuit model Figure 4.8 :

$$Z_{oi}(s) \approx \frac{R_e R_L}{R_e + R_L} \frac{\mathbf{1} + R_{Co} C_o s}{\mathbf{1} + (R_e \parallel R_L) C_o s} \qquad (4.\ 18)$$

As showed in Figure 4.9, the impedance curves of peak current mode control, constant on-time control and constant off-time control do not have significant difference.

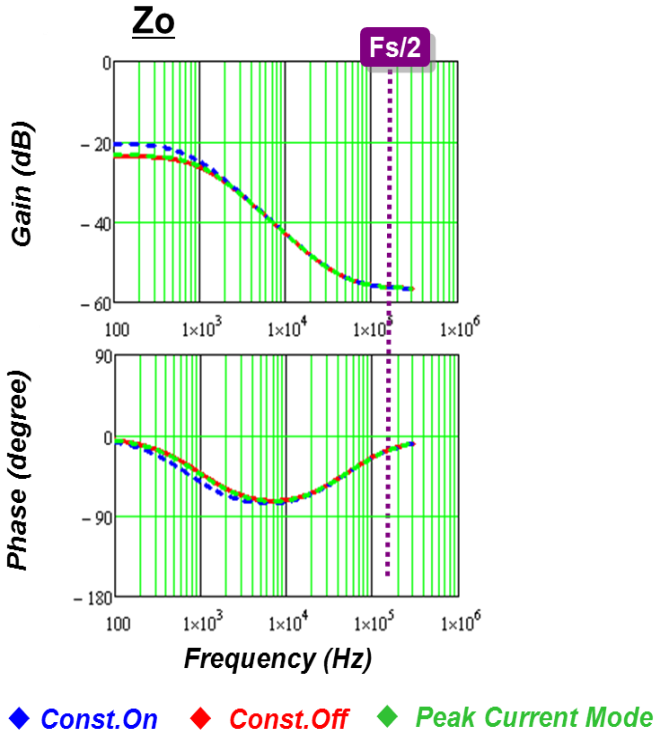


Figure 4.9 Open loop output impedance of current mode control

Current VR faces the stringent challenge of not only high current but also a strict transient response requirement. Figure 4.10 shows the VR output load line from the Intel VRD 11.0 specification. Adaptive voltage positioning (AVP) control is widely used to achieve constant-output impedance design to meet the load-line requirement [20][21][22][23][24][25].

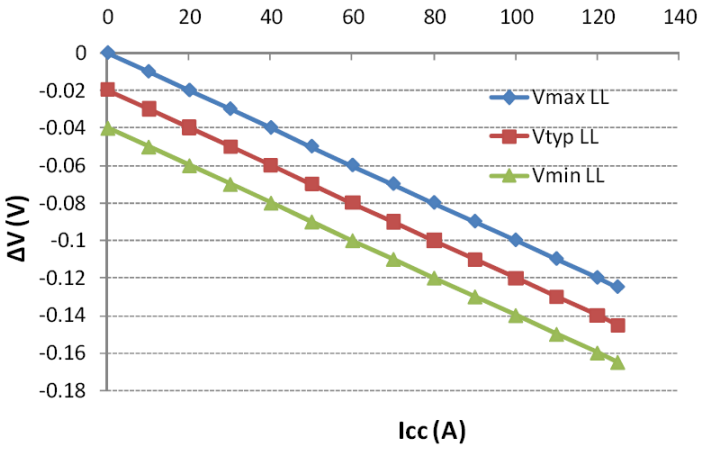


Figure 4.10. Load-line specification of Intel VRD 11.0

Current mode control is one of the most important methods used to achieve constant output impedance. To analyze the outer loop compensator design, asymptote bode plot is used in the following analysis.

Since the high frequency output impedance is determined by the ESR of the output capacitor as mentioned before, designers usually choose proper number of output capacitor to make the equivalent ESR value equals to the required impedance value. The impedance within ESR zero will be reshaped as a flat curve by control loop.

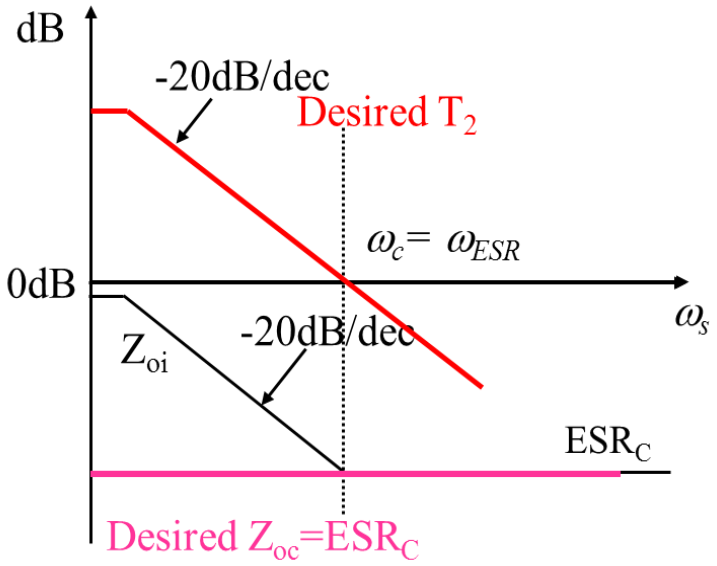


Figure 4.11 Constant output impedance design target and desired T2

For peak current mode control case, as shown in Figure 4.11, within ESR zero frequency, the desired T_2 has the same shape as the control-to-output transfer function. So, only a pure gain is needed in this range. Tune the gain to make T_2 cross over at ESR zero frequency. As a result, the closed loop output impedance within ESR zero is reshaped as a flat curve. After ESR zero, place a pole to compensate the ESR zero to keep the loop gain T_2 keep -20dB/dec roll off. Since the cross over frequency is close to half the switching frequency, especially in a laptop VR case where switching frequency is only 200kHz~300kHz, a pole is needed at half switching frequency to guarantee enough phase margin. Otherwise, the phase drop introduced by double

poles can diminish the phase margin and cause output voltage overshoot in load current step response. The compensator can be expressed by Eq.(4.19) and an asymptote bode plot is shown in Figure 4.12.

$$H_v(s) \approx \frac{R_i}{R_{Co}} \frac{1 + s/\pi f_{sw}}{1 + R_{Co}C_o s} \tag{4.19}$$

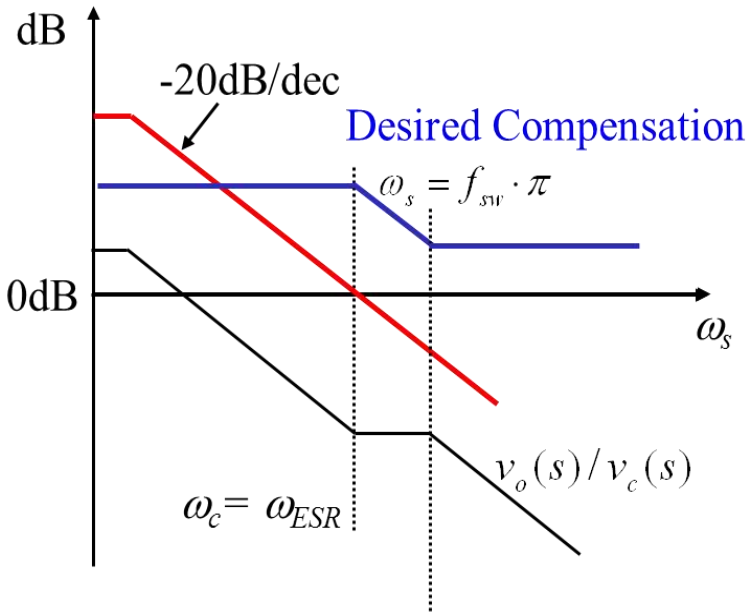


Figure 4.12 Compensator design for peak current mode control

For constant on-time current mode control case, the bandwidth should still be set at ESR zero frequency so that within the bandwidth only a pure gain is needed. The same as peak current mode control, place a pole to compensate the ESR zero. The fundamental difference between constant on-time current mode control is constant on-time control does not have double poles at half switching frequency, so the pole at high frequency is unnecessary. The compensator can be expressed by Eq.(4.20) and the asymptote bode plot is shown in Figure 4.13.

$$H_v(s) \approx \frac{R_i}{R_{Co}} \frac{1}{1 + R_{Co}C_o s} \tag{4.20}$$

Figure 4.14 is the simulation result of the closed loop output impedance, using the

proposed compensator as Eq.(4.20). From the result, we can see constant output impedance is well achieved.

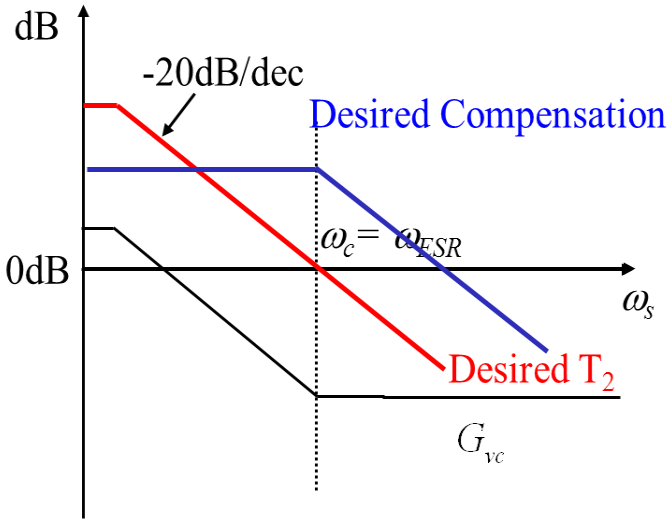


Figure 4.13 Compensator design for constant on-time current mode control

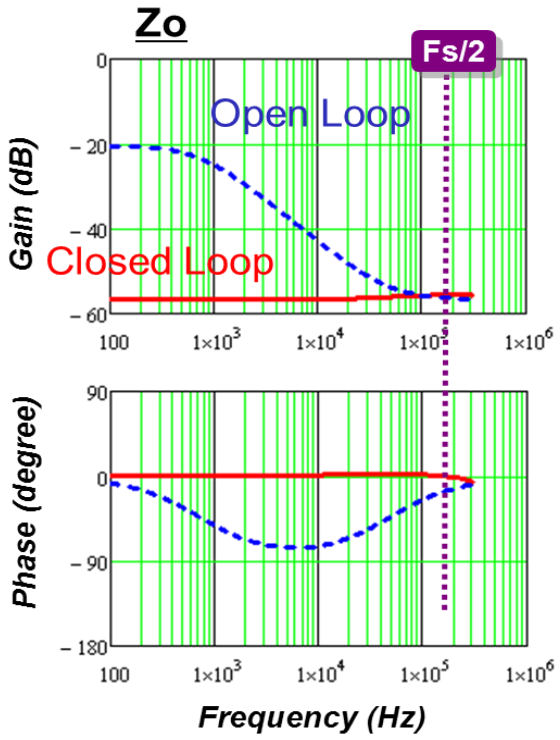


Figure 4.14 Simulation result of output impedance of constant on-time current mode control

Comparing the compensator for peak current mode control (Eq.(4.19)) and the

compensator for constant on-time current mode control (Eq.(4.20)), we can see that the constant on-time implementation simplifies the compensator structure. The simplified structure can help to reduce the cost and the footprint of the converter design.

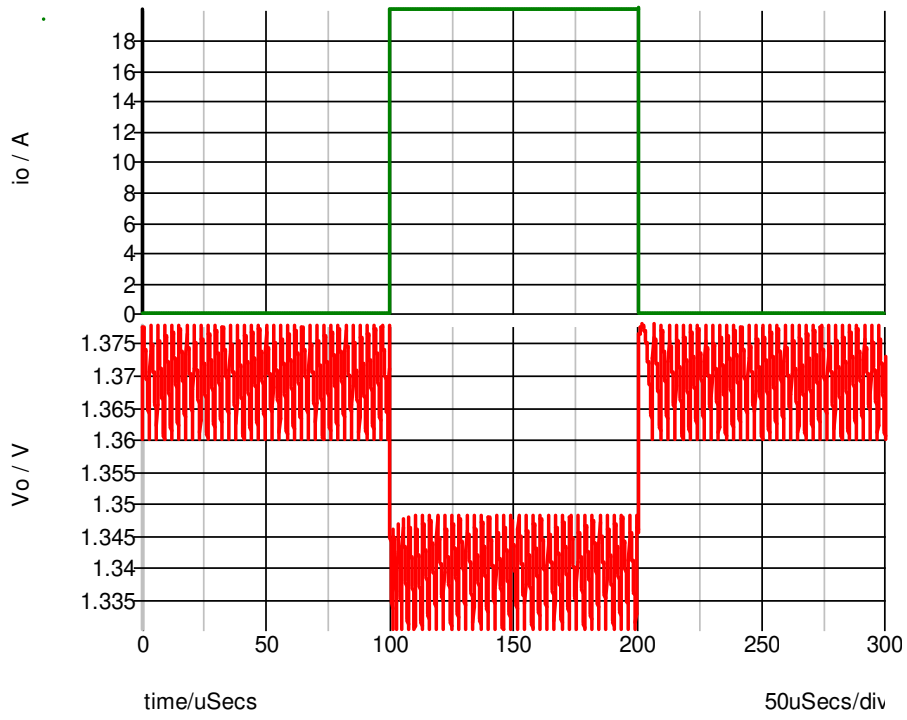


Figure 4.15 Simulation result for the transient response with constant on-time current mode control

4.4 Summary

Comparison between different current mode control implementation is presented. In different applications, different implementations have their unique benefit on extending control bandwidth. The properties of audio susceptibility and output impedance are discussed. It is found that, for adaptive voltage positioning design, constant on-time current mode control can simplify the outer loop design.

Chapter 5. Three-terminal Switch Mode for Multiphase Current Mode Controls

This chapter presents the three-terminal switch mode for multiphase current mode control. It is an extension of the single phase three-terminal switch model. The single phase small signal model and multiphase mode are compared. Simulation and experimental results are used to verify the proposed model.

5.1 Application of Multiphase Current Mode Control Power Converter

Today, with the development of information technology, the power supply industry has a large market in telecom and computer systems [11]. Power supplies for these applications require the power supply to be small, efficient and stackable. To meet these requirements, the distributed power system (DPS) is widely adopted. Instead of using a single bulky power supply to provide the final voltages required by the load, the distributed power system is characterized by the distribution of the power processing functions among many power processing units [14].

By using multi-modular approach, the DPS system has many advantages when compared with conventional centralized power systems, such as less distribution loss, faster current slew rate to the loads, better standardization and ease of maintenance [17].

One of the typical applications for this multi-phase interleaving structure is the voltage regulator of micro-processor. The interleaving multi-phase Buck VR is the current solution for CPU voltage regulator [10] which is shown in Figure 5.1. By paralleling several synchronous buck converters and phase shifting their drive signals,

the interleaving approach can reduce both the input and output current ripples, improve the transient response, and distribute power and heat [11][12].

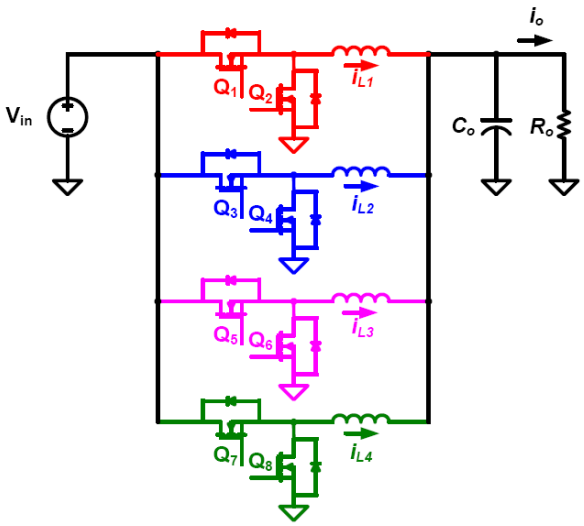


Figure 5.1 Multiphase interleave Buck converter

Recently, in order to improve light load efficiency and EMI filter design, [76] proposed a multi-phase interleaved Boost PFC architecture, as shown in Figure 5.2. According to the load condition, some of the phases are shut off to improve light load efficiency. Meanwhile, interleaving the phases with certain phase shift angle can reduces EMI noise.

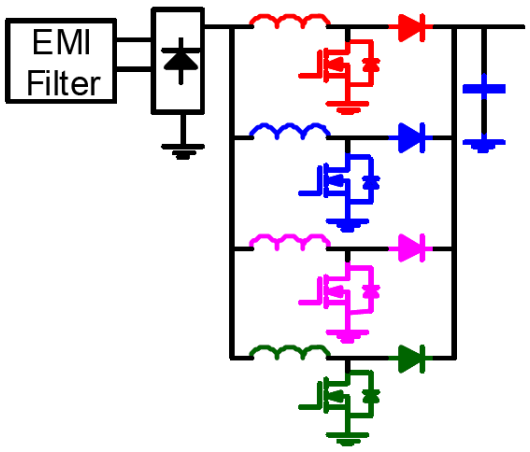


Figure 5.2 Multiphase interleave Boost PFC

5.2 Three-terminal Switch Mode for Multiphase Current Mode Controls

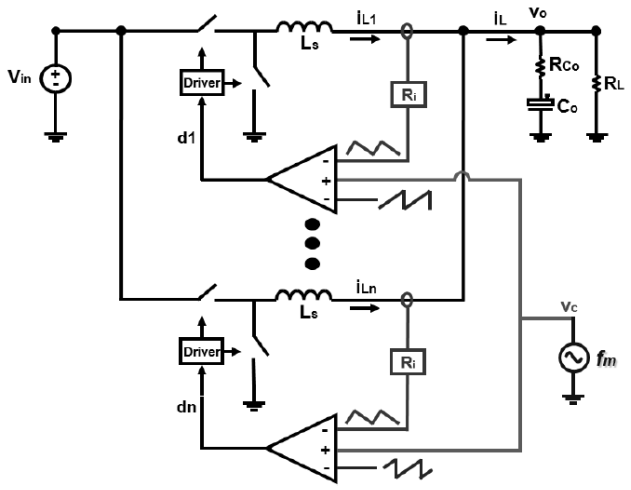


Figure 5.3 Multiphase interleave current mode control Buck converter

A multiphase buck converter with current mode control is shown in Figure 5.3. Each phase has its own current sensor and PWM modulator, and all the phases share the same control voltage v_c. Assume in an ideal case that all the phases are identical, to obtain the small signal equivalent circuit, the PWM switch with closed current loop can be replaced by the identical three-terminal switch model presented in the previous chapter. The small signal equivalent circuit is shown in Figure 5.4.

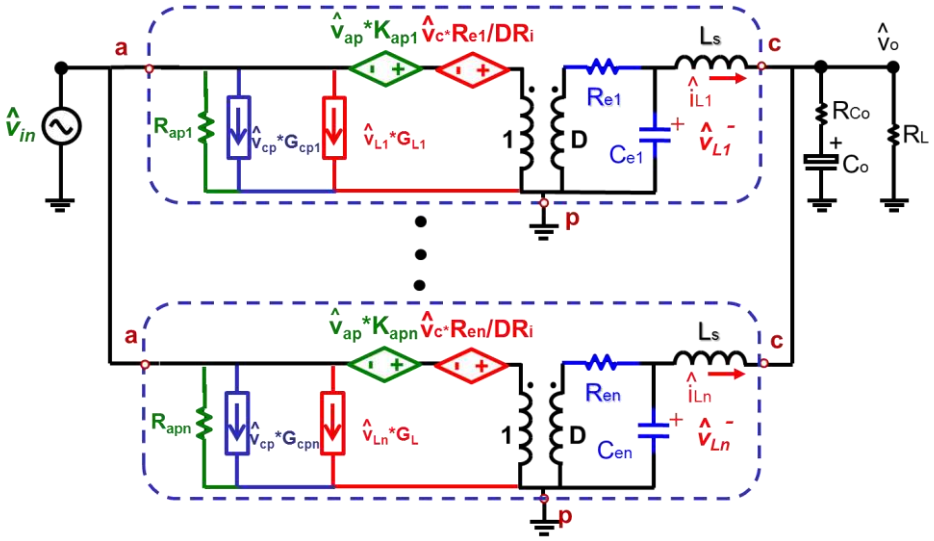


Figure 5.4 Equivalent circuit for multiphase Buck converter

(N single phase equivalent circuit in parallel)

In Table 5.1, the parameters of the small signal model are defined as:

Table 5.1. Parameters Definition of Figure 5.4

Peak current mode control		
$R_{ek} = L_s / [T_{sw}(\frac{s_n + s_e}{s_n + s_f} - \mathbf{0.5})]$	$C_{ek} = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = -\frac{T_{off}}{\mathbf{2}L_s} R_e$
$R_{apk} = -V_{ap} / DI_{ck}$	$G_{cpk} = I_{ck} / V_{ap}$	$G_{Lk} = I_{ck} / V_{ap}$
Valley current mode control		
$R_{ek} = L_s / [T_{sw}(\frac{s_f + s_e}{s_n + s_f} - \mathbf{0.5})]$	$C_{ek} = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = \frac{T_{off}}{\mathbf{2}L_s} R_e$
$R_{apk} = -V_{ap} / DI_{ck}$	$G_{cpk} = I_{ck} / V_{ap}$	$G_{Lk} = I_{ck} / V_{ap}$
Charge control		
$R_e = L_s / [T_{sw}(\frac{L_s I_L}{V_{cp} T_{sw}} - \frac{D}{\mathbf{2}} + \frac{s_e}{s_f}\frac{C_T}{T_{sw}})]$	$C_{ek} = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = \frac{T_{on}}{\mathbf{2}L_s} R_e$
$R_{apk} = -V_{ap} / DI_{ck}$	$G_{cpk} = I_{ck} / V_{ap}$	$G_{Lk} = I_{ck} / V_{ap}$
Constant on-time control		

$R_e = \mathbf{2}L_s / T_{on}$	$C_{ek} = T_{on}^2 / (L_s \pi^2)$	$K_{ap} = T_{off} / T_{on}$
$R_{apk} = -V_{ap} / DI_{ck}$	$G_{cpk} = I_{ck} / V_{ap}$	$G_{Lk} = I_{ck} / V_{ap}$
Constant off-time control		
$R_e = \mathbf{2}L_s / T_{off}$	$C_{ek} = T_{off}^2 / (L_s \pi^2)$	$K_{ap} \approx -\mathbf{1}$
$R_{apk} = -V_{ap} / DI_{ck}$	$G_{cpk} = I_{ck} / V_{ap}$	$G_{Lk} = I_{ck} / V_{ap}$

To further simplify the analysis, the multi-phase structure can be simplified to an equivalent single phase structure, and the three-terminal switches are simplified to a single three-terminal equivalent circuit, as shown in Figure 5.5.

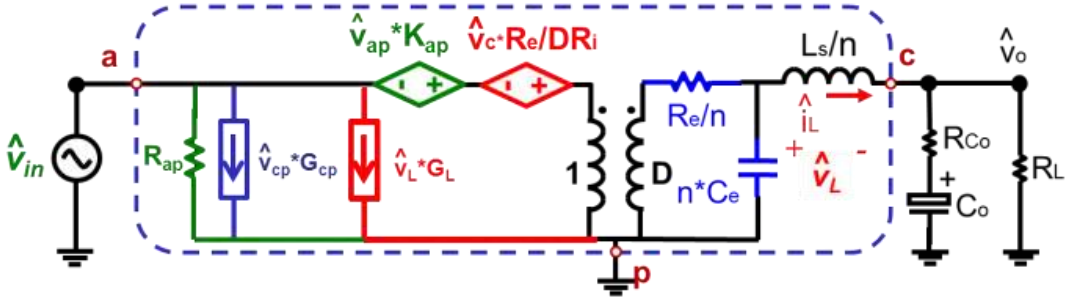


Figure 5.5 Equivalent circuit for multiphase Buck converter

(Equivalent single phase representation)

In Table 5.2, the parameters of the small signal model are defined as:

Table 5.2. Parameters Definition of Figure 5.5

Peak current mode control		
$R_e = L_s / [T_{sw}(\frac{s_n + s_e}{s_n + s_f} - \mathbf{0.5})]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = -\frac{T_{off}}{\mathbf{2}L_s} R_e$
$R_{ap} = -V_{ap} / DI_c$	$G_{cp} = I_c / V_{ap}$	$G_L = I_c / V_{ap}$
Valley current mode control		

$R_e = L_s / [T_{sw}(\frac{s_f + s_e}{s_n + s_f} - \mathbf{0.5})]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = \frac{T_{off}}{\mathbf{2}L_s} R_e$
$R_{ap} = -V_{ap} / DI_c$	$G_{cp} = I_c / V_{ap}$	$G_L = I_c / V_{ap}$
Charge control		
$R_e = L_s / [T_{sw}(\frac{L_s I_L}{V_{cp} T_{sw}} - \frac{D}{\mathbf{2}} + \frac{s_e}{s_f}\frac{C_T}{T_{sw}})]$	$C_e = \frac{T_{sw}^2}{L_s \pi^2}$	$K_{ap} = \frac{T_{on}}{\mathbf{2}L_s} R_e$
$R_{ap} = -V_{ap} / DI_c$	$G_{cp} = I_c / V_{ap}$	$G_L = I_c / V_{ap}$
Constant on-time control		
$R_e = \mathbf{2}L_s / T_{on}$	$C_e = T_{on}^2 / (L_s \pi^2)$	$K_{ap} = T_{off} / T_{on}$
$R_{ap} = -V_{ap} / DI_c$	$G_{cp} = I_c / V_{ap}$	$G_L = I_c / V_{ap}$
Constant off-time control		
$R_e = \mathbf{2}L_s / T_{off}$	$C_e = T_{off}^2 / (L_s \pi^2)$	$K_{ap} \approx -\mathbf{1}$
$R_{ap} = -V_{ap} / DI_c$	$G_{cp} = I_c / V_{ap}$	$G_L = I_c / V_{ap}$

The model is verified by SIMPLIS simulation. The parameters of the of the 2-phase peak current-mode control buck converter are as follows: V_{in} = 12V, V_o = 5V, f_s = 300kHz, C_o = 8×560μF, R_{Co} = 6/8mΩ, and L_s =300nH. The control-to-output transfer function is shown in Figure 5.6. The proposed model can accurately predict the system response up to half switching frequency.

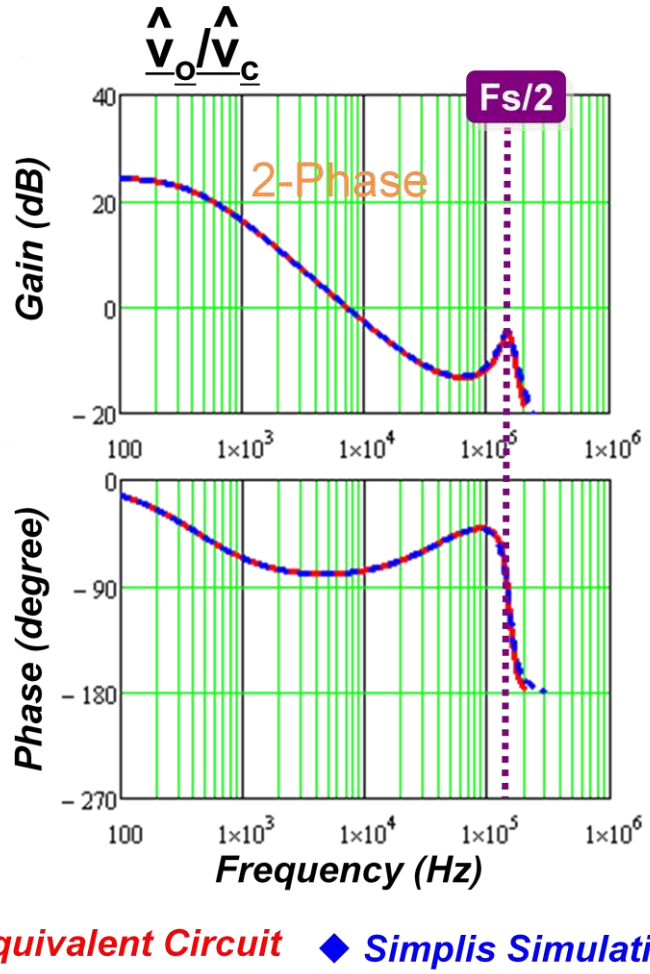


Figure 5.6 Control-to-output transfer function of 2-phase Buck converter

5.3 Analysis of Small Signal Model for Multiphase Converter

Based on the small signal equivalent circuit, control to output transfer function can be written as:

$$\left.\frac{\hat{v}_o(s)}{\hat{v}_c(s)}\right|_{N\_Phase} = N \cdot K_c \frac{(1+R_{Co}C_o s)}{1+s/\omega_a} \frac{1}{1+\dfrac{s}{Q_2\omega_2}+\dfrac{s^2}{\omega_2^2}} \approx N \cdot \left.\frac{\hat{v}_o(s)}{\hat{v}_c(s)}\right|_{1\_Phase} \tag{5.1}$$

where

$$\omega_a = \frac{1+R_L/(R_e/N)}{(R_L+R_{Co})C_o + R_L R_{Co} C_o/(R_e/N)} \qquad K_c = \frac{1}{R_i}\frac{R_L}{1+R_L/(R_e/N)}$$

Compare Eq.(5.1) with Eq.(4.1), the multiphase equivalent circuit reveals some important properties of multiphase current mode control converter.

First, the gain coefficient of control-to-output transfer function is changed with the phase number. The control-to-output gain of the N phase converter is N times of that of the single one, as shown in Figure 5.7. The reason is simple: in a single phase case, the control signal controls only one current source. The control gain is $1/R_i$. In a multiphase case, the control signal controls N inductor current sources, the sum of which feed into the load. As a result, the control to output gain is N times higher than the single phase converter. This property is quite different from the multiphase converter with voltage mode control.

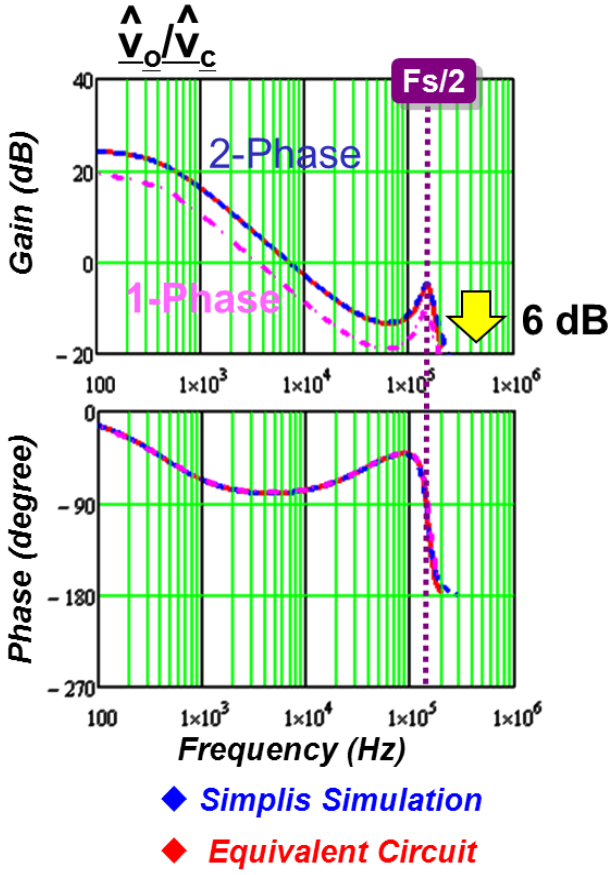


Figure 5.7 Comparison of control-to-output transfer function: single phase vs. 2-phase

Second, compared with a single phase small signal model, the equivalent inductor

is N times smaller. Meanwhile, the damping resistor R_e is N times smaller and C_e is N times larger. The high frequency double poles resonant frequency, which is determined by inductor L_s and equivalent C_e is:

$$\omega_N = \frac{\mathbf{1}}{\sqrt{\frac{L_s}{N}\cdot N\cdot C_e}} = \frac{\mathbf{1}}{\sqrt{L_s C_e}} = \omega \tag{5.2}$$

From Eq.(5.2), we can see that the high frequency double pole position is independent of the paralleling phase number. In another words, a designer can not extend the outer loop bandwidth by paralleling multiphase converter to push the double pole to a higher frequency.

The quality factor of the high frequency double pole is the design target of the external ramp in constant frequency modulation current mode control. From the equivalent circuit in Figure 5.5, the double pole quality factor is expressed as:

$$Q_N = \frac{\sqrt{(\frac{L_s}{N})/(N\cdot C_e)}}{R_e/N} = \frac{\sqrt{L_s/C_e}}{R_e} = Q \tag{5.3}$$

Eq.(5.3) shows that quality factor of the high frequency double pole is also independent of paralleling phase number.

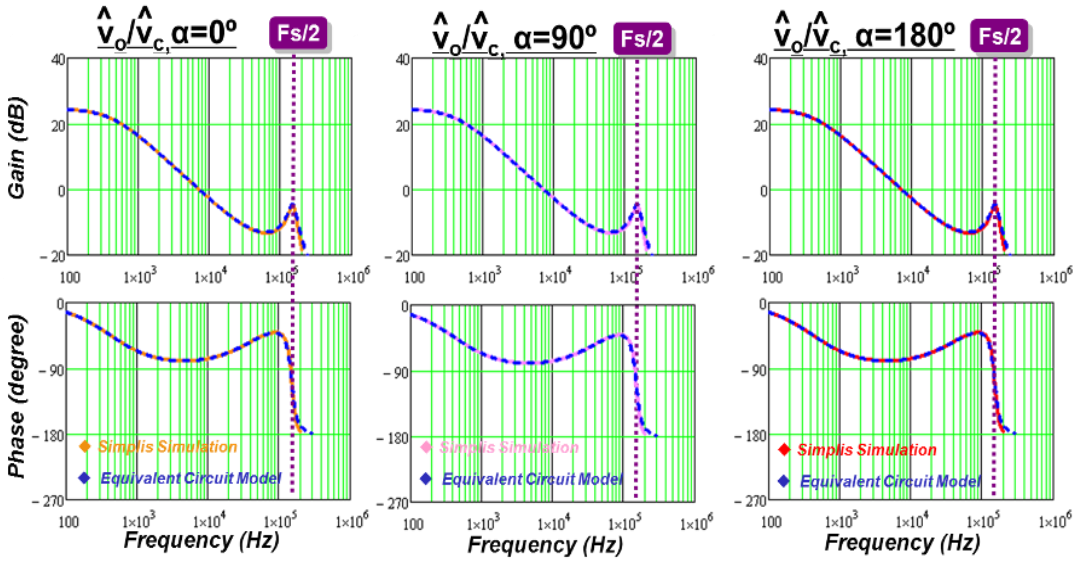


Figure 5.8 Control-to-output transfer function of different phase shift angles

Third, small signal model of multiphase converter is independent of the phase shift angle, as shown in Figure 5.8. In the small signal equivalent circuit, no parameter is related with phase shift angle. Essentially, the current sensing, feedback and modulation of each phase is running without interaction. So, the interleave phase angle does not affect the small signal model.

Similarly, input to output transfer function can be written as:

$$\left.\frac{\hat{v}_o(s)}{\hat{v}_c(s)}\right|_{N\_Phase} \approx N \cdot \left.\frac{\hat{v}_o(s)}{\hat{v}_c(s)}\right|_{1\_Phase} \tag{5. 4}$$

Eq.(5. 4), the gain coefficient of input-to-output transfer function is changed with the phase number. The control-to-output gain of N phase converter is N times of that of the single one, as shown in Figure 5.9. This is considered as a drawback of the multi-phase parallel solution, compared with single module architecture.

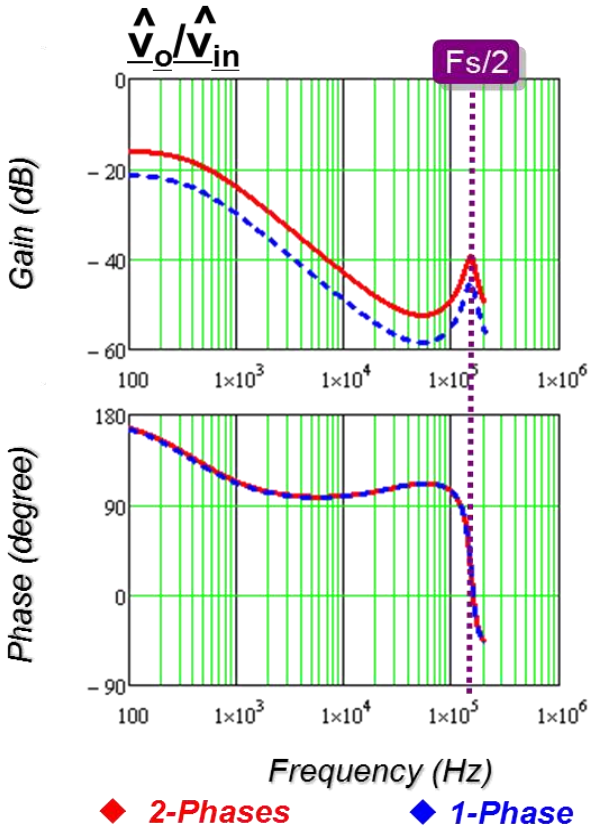


Figure 5.9 Comparison of input-to-output transfer function: single phase vs. 2-phase

5.4 Feedback Design Consideration for Multi-phase Converter with Current Mode Control

Based on the analysis in section 4.3, control-to-output transfer function is repeated in Eq.(5.5)

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = N \cdot K_c \frac{(1 + R_{Co} C_o s)}{1 + s/\omega_a} \frac{1}{1 + \frac{s}{Q_2 \omega_2} + \frac{s^2}{\omega_2^2}} \tag{5.5}$$

Since the quality factor of high frequency double pole is also independent of paralleling phase number, the design guideline of the external ramp has nothing to do with the phase number. The proper design should change the quality factor to approximately equal to 1.

In practical design, many multi-phase converters adopt phase shedding function to improve the light load efficiency. Phase shedding changes the phase number and plant characteristics. To design the voltage loop compensator, the design should start with the maximum phase number, since in this case the control to output gain is maximum. Check the phase margin for single phase configuration. Basically, the dynamic response of less phase configuration is worse than that of more phases because of lower bandwidth.

Figure 5.10 shows a design example. The controller is designed for a 2-phase current mode control Buck converter. T_2 bandwidth is 60kHz in 2-phase operation. With phase shedding, in 1-phase operation, the bandwidth is narrowed to 30kHz.

In voltage regulator for microprocessor, the adaptive voltage positioning function is required. To achieve the load line requirement, the VR should have a constant output impedance. [22] proposed a method using current mode control with a finite gain compensator to achieve constant output impedance. T_2 bandwidth is designed at ESR zero of the output capacitor. In this way, the output impedance within the bandwidth is controlled by feedback loop, and the output impedance beyond the bandwidth is dominated by the output capacitor ESR.

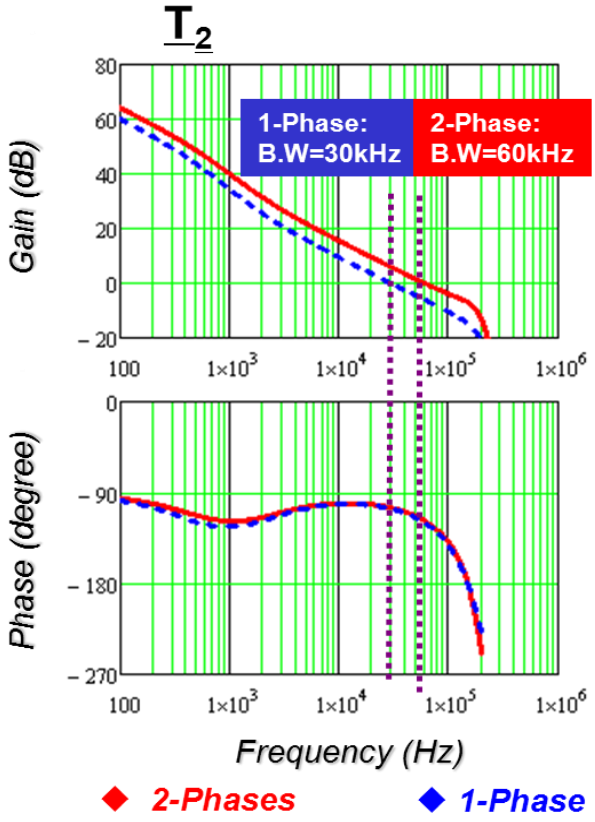


Figure 5.10 Comparison of T_2 loop gain: single phase vs. 2-phase

The small signal model reveals that the gain of the control-to-output transfer function changes with the phase number. With the same compensator, the T_2 bandwidth is variable. As a result, when some of the phase is shut down, the output impedance is no longer constant resistive impedance, as shown in Figure 5.11.

The simulation circuit is a two-phase Buck converter with peak current mode control. Parameters of each phase are as follows: V_{in} = 12V, V_o = 5V, f_{sw} = 300kHz, C_o = 8×560μF, R_{Co} = 6/8mΩ, and L_s =300nH. Figure 5.12 is the comparison of the closed loop output impedance. Since the compensator is design for 2-phase case, in 2-phase operation, the output impedance is a constant. When the circuit operates in a 1-phase configuration, the low frequency output impedance is higher than the specification.

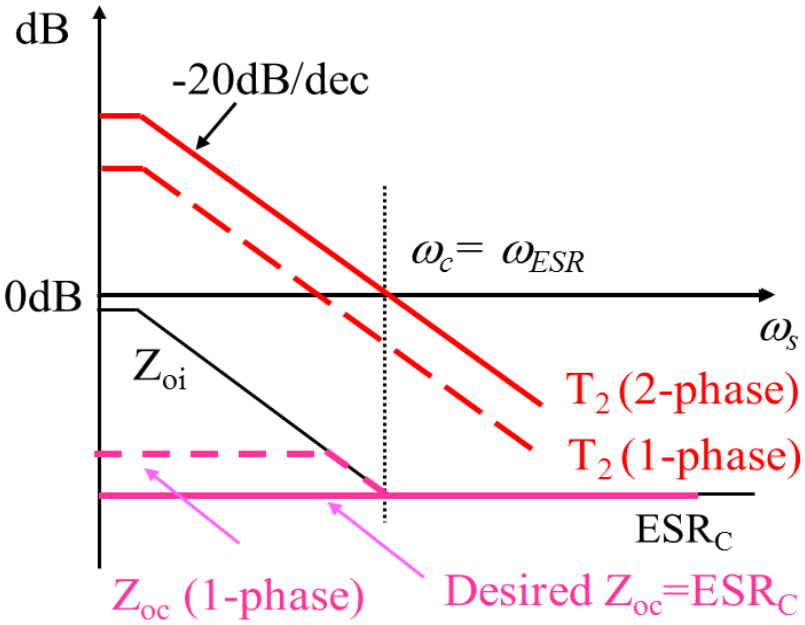


Figure 5.11 Output impedance of single phase Buck

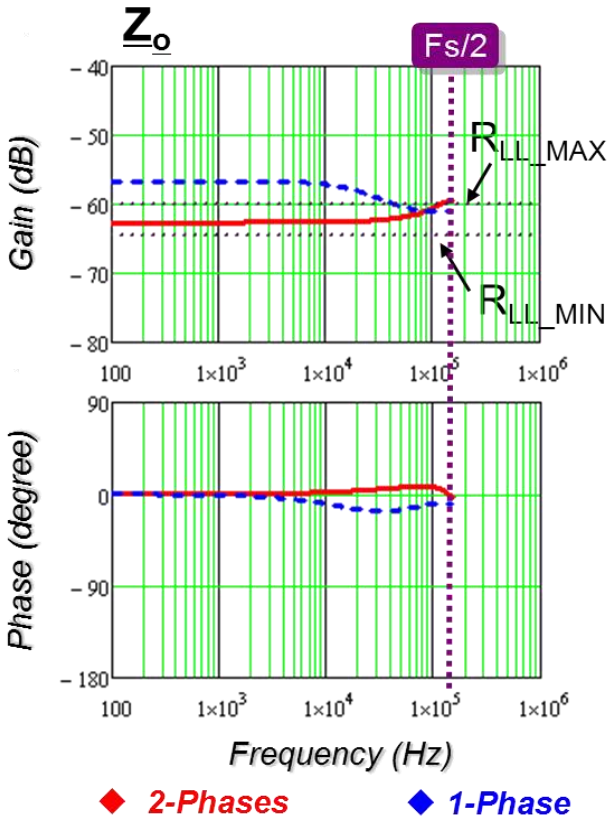


Figure 5.12 Output impedance of single phase Buck and 2-phase Buck

To solve this problem, compensator can use adaptive gain according to the phase number. The other way is to change the current sensing gain to be inversely proportional to the phase number. The implementation of adaptive control is out of the discussion area of this thesis.

5.5 Summary

The three-terminal switch model is extended to a multiphase current mode control. Some design concerns are discussed based on the model.

Chapter 6. Conclusion

6.1 Summary

Current-mode control architectures with different implementation approaches have been an indispensable technique in many applications, such as voltage regulator, power factor correction, battery charger and LED driver. Since the inductor current ramp, one of the state variables influenced by the input voltage and the output voltage, is used in the modulator in current-mode control without any low pass filter, high order harmonics play important role in the feedback control. This is why it is difficult to obtain the small-signal model for current-mode control in the frequency domain. Continuous time domain model proposed recently successfully model the current-mode control architectures with different implementation. However, the model was derived from describing function method, which is very mathematically complicated and also time consuming. Although an equivalent circuit for current mode control Buck converter was proposed to help designers to use the model without involving complicated math, the equivalent circuit is not a complete model. Moreover, no equivalent circuit for other topologies is available for designers. In this thesis, the primary objective is to develop a unified three-terminal switch model for current-mode control with different implementation methods, which are applicable in all the current mode control power converters.

First, the existing model for the current mode control is reviewed. The limitation of average models and discrete time model for the current-mode control is identified. The continuous time model and its equivalent circuit of Buck converter is introduced. The deficiency of the equivalent circuit is discussed.

After that, a unified three-terminal switch model for current mode control is presented. Based on the observation, the PWM switch and the closed current loop is taken as an invariant sub-circuit, which is common to different DC/DC converter topologies. A basic small signal relationship is studied and the result shows that the

PWM switch with current feedback preserves the property of the PWM switch. A three-terminal equivalent circuit is developed to represent the small signal behavior of this common sub-circuit. The proposed model is a unified model which is applicable in both constant frequency modulation and variable frequency modulation. The physical meaning of the three-terminal equivalent circuit model is discussed. The model is verified by SIMPLIS simulation in commonly used converters for both constant frequency modulation and variable frequency modulation.

Then, based on the proposed unified model, a comparison between different current mode control implementations is presented. In different applications, different implementations have their unique benefit on extending control bandwidth. The properties of audio susceptibility and output impedance are discussed. It is found that, for adaptive voltage positioning design, constant on-time current mode control can simplifiy the outer loop design.

Next, since multiphase interleaving structure is widely used in PFC, voltage regulator and other high current applications, the model is extended to multiphase current mode control. Some design concerns are discussed based on the model.

As a conclusion, a unified three-terminal switch model for current mode controls is investigated. The proposed model is quite general and not limited by implementation methods and topologies. All the modeling results are verified through simulation and experiments.

6.2 Future Works

In the thesis, a three-terminal switch model is proposed to characterize the small signal model of current mode control converters, including peak current mode control, valley current mode control, charge control and constant on-time control and constant off-time control. The equivalent circuit model might be extended to average current mode control and hysteresis current mode control. Furthermore, it could be interesting

to develop an equivalent circuit model for V^2 control, which suffers from high frequency sub-harmonic oscillation problem.

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