Unipolar Complementary Circuits using Double Electron Layer Tunneling Transistors.

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ABSTRACT

We demonstrate unipolar complementary circuits consisting of a pair of resonant tunneling transistors based on the gate control of 2D-2D interlayer tunneling, where a single transistor -- in addition to exhibiting a well-defined negative-differential-resistance -- can be operated with either positive or negative transconductance. Details of the device operation are analyzed in terms of the quantum capacitance effect and band-bending in a double quantum well structure, and show good agreement with experiment. Application of resonant tunneling complementary logic is discussed by demonstrating complementary static random access memory using two devices connected in series.

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For over a decade, various quantum tunneling transistors have been continuously proposed and demonstrated. [1] These devices offer the potential for application in high speed and multi-functional circuits. To implement functional circuits with low power dissipation, complementary operation of resonant tunneling transistors (RTTs), analogous to Si complementary metal-oxide-semiconductor (CMOS) architecture, is highly desirable.[2, 3] However, the transconductance of almost all RTTs including those based on double barrier resonant tunneling devices (DBRTDs) [4] is limited to a single polarity determined by the sign of carriers, electrons or holes. Interestingly, a few unipolar (electron) RTTs have been reported with both sign of transconductance, determined by relative alignment of the Fermi levels in the emitter and collector. One such device is fabricated with a two-dimensional (2D) quantum well (QW) collector, instead of the 3D collector in DBRTDs. [5] The second device is based on resonant tunneling from a two-dimensional electron gas (2DEG) into one-dimensional (1D) wire subbands. [3, 6]. However, it is questionable whether these devices have sufficient transconductance to form a complementary circuit when used together in pairs. Thus, to date, the complementary operation of a pair of RTTs has not been reported.

Recently, several techniques for making independent contacts to two closely spaced (typically 200Å) 2DEGs were developed to study 2D-2D interlayer tunneling. [7] Several interesting phenomena, including negative compressibility [8], tunneling resonance [9], and negative-differential-resistance (NDR) [10], have been observed in the electron transport. Recently, a novel RTT, the double electron layer tunneling transistor (DELTT) based on the gate control of 2D-2D interlayer tunneling current, was also successfully demonstrated. [11] In this letter, we demonstrate the complementary operation of a pair of resonant tunneling transistors. The RTTs used are DELTTs, whereby a single DELTT device can be operated in either the positive or negative transconductance region depending on the sign of the Fermi level differences in the source and drain 2D QWs. To further confirm the utility of this approach, a complementary static random access memory

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(SRAM) is demonstrated at 77K using two DELTT devices connected in series.

In conventional Si CMOS, the basic idea is that by using two series-connected transistors of opposite sign of carriers, the middle node voltage can switch high or low with respect to the gate voltage swing, but no significant standby current flows since one of the transistors is always off. To achieve similar behavior in an unipolar circuit consisting of a pair of series-connected DELTTs, the two DELTTs should have transconductance of opposite sign.

Since the 2D-2D interlayer tunneling in DELTTs conserves in-plane momentum and energy, the current depends on the difference between the top and bottom QW lowest subband energies $\Delta E_0 = E_{0,T} - E_{0,B}$, with the tunneling current strongest when $\Delta E_0 = 0$. [9-11] The complementary operation of DELTTs can be implemented in the following way. First assume that the top QW has a higher density as sketched in Fig. 1(a). Application of a positive topgate voltage increases the electron density mainly in the top QW and consequently the subband separation ΔE_0, resulting in further suppression of the interlayer tunneling -- i.e. the device switches off. Similarly, a negative topgate voltage turns the device on. In contrast, application of a positive (negative) gate bias to the backgate switches the device on (off), an opposite effect to that of the topgate. Thus, *the polarity of transconductance can be selected depending on which gate -- top or back -- is biased.* Complementary switching operation can then be obtained by applying input to gates on opposite sides for the two DELTTs connected in series. To get an equally effective gating or gate leverage factor from both sides, crucial for a complementary SRAM application, both gates must be defined in roughly equally close proximity to the QWs.

However, due to the finite compressibility of 2DEGs, the gate electric field penetrates both QWs and changes both electron densities in quantum wells. We estimated this quantum capacitance effect [12] in a double quantum well (DQW) structure first, considering the electrons as non-interacting particles in two infinitely narrow QWs. [13]

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The 'topgate leverage factor', defined as the variation in E_F in each QW due to the top control gate voltage V_{TC}, is given by

$$\lambda_T^{-1} = \left(\frac{\partial E_{F,T}}{e \partial V_{TC}}\right) = \frac{C_1 + C_1 C_2 / C_{Q,B}}{C_1 + C_2 + C_{Q,T} + (C_1 C_2 + C_2 C_{Q,T})/C_{Q,B}}$$

$$\lambda_B^{-1} = \left(\frac{\partial E_{F,B}}{e \partial V_{TC}}\right) = \frac{C_1 C_2 / C_{Q,B}}{C_1 + C_2 + C_{Q,T} + (C_1 C_2 + C_2 C_{Q,T})/C_{Q,B}}$$

Here, $C_1 = \varepsilon/L_1$ and $C_2 = \varepsilon/L_2$ are the geometric capacitances per unit area between the topgate and the top QW, and between the two QWs, respectively. $C_Q = m^* e^2 /(\pi \hbar^2)$ is the quantum capacitance with the effective mass m^*. Using the experimental parameters of our current DELTTs, we find that the relative change in electron densities, $\frac{\delta N_B}{\delta N_T} = \frac{1}{C_{Q,T}}(\frac{C_2 \cdot C_{Q,B}}{C_2 + C_{Q,B}})$, is about 10%. The shift in ΔE_0 can also be estimated from

$\lambda_{QC}^{-1} = \lambda_T^{-1} - \lambda_B^{-1}$. In reality, corrections due to the finite thickness of the QWs need to also be taken into account. The dominant correction is the band-bending effect which occurs due to the added electrons and results in making the QW potentials more asymmetric. We solved the Schrödinger and Poisson equations self-consistently as a function of gate voltage, and found $\delta N_B / \delta N_T \approx 6\%$, implying that the band bending reduces the field penetration to the bottom QW. [14] Thus, the gate electric field primarily influences the quantum well closest to it, allowing the complementary operation scheme described above.

Devices were processed from an MBE-grown heterostructure (wafer G1881) with two 120Å thick GaAs QWs separated by a single 125Å thick $Al_{0.3}Ga_{0.7}As$ tunnel barrier. Both QWs are Si modulation doped and the 2DEGs are confined in the top and bottom QWs with densities of 8.0 and 2.0 x 10^{11} cm^{-2}, respectively. The resulting Fermi energy

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difference ΔE_0 is ~21 meV. A basic description of the DELTT structure in Fig. 1(b) can be found elsewhere. [11] The topgates are defined with 1000Å Si_3N_4/SiO_2 gate dielectrics underneath, not only to minimize the gate leakage but also to better equalize the gate leverage factor. The control gate length of devices studied were 40, 70, and 200 μm for DELTTs 1, 2, and 3 respectively. All DELTTs had both top and back control gates vertically aligned to one another, and channel widths of 500 μm. All measurements were done at 77 K, with excellent reproducibility over thermal cycles.

First, the I-V characteristics of a single device, DELTT 2, are shown in Fig. 2(a) for several topgate voltages V_{TC} and in Fig. 2(b) for several backgate voltages V_{BC}. The I-V characteristics are asymmetric with a single resonance peak occuring at single source-drain bias polarity only. [15] With no control gates biased, the peak-to-valley ratio is ~ 2:1 with a peak current I_p of 57 μA and peak and valley voltages of V_p ~ 0.053 V and V_v ~ 0.057 V. As can be seen from Fig. 2, the sign of the transconductance actually depends in a rather complex way on both the value of V_{SD} and of the gate bias, for either gate. Most importantly, the topgate and backgate voltages strongly modulate both V_p and I_p in an *opposite* polarity; the plots of peak current vs. gate voltage in the insets show clearly the opposite effect of the gates. The shift in V_p with respect to the topgate bias is obtained as $\Delta V_p / \Delta V_{TC} \approx 17$ mV/V, which is considerably larger than the $\Delta E_0 / \Delta V_{TC}$ of 7 meV/V obtained from simultaneously solving the Schrödinger and Poisson equations and taking the gate dielectric into account. Indeed, the peak positions V_p occur at much higher source-drain bias than expected from the simply estimated ΔE_0; at $V_{TC} = V_{BC} = 0$, the discrepancy is about 32 mV. From a careful examination of both the tunnel conductance and the channel depletion characteristics of each gate, the in-plane resistance of the QWs is

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estimated as 500 ~ 600 Ω. Thus, in addition to the tunneling resistance, there is a significant source-drain voltage drop in the channel ; at $V_{TC} = V_{BC} = 0$, the voltage drop is about 28 ~ 32 mV at $V_{SD} = V_p$, consistent with the observed discrepancy in the peak voltage. We also attributed the discrepancy in $\Delta V_p / \Delta V_{TC}$ to the finite in-plane resistance.

The current-voltage characteristics of two DELTTs connected in series is shown in Fig. 3(a), where the control gates are grounded. The I-V has two peaks at V_{Supply} ~ 0.10 V and ~ 0.14 V with hysteresis present. Since DELTT 2 has a smaller peak current than DELTT 3, DELTT 2 switches from peak to valley first as the supply voltage increases above ~ 0.1 V ($\geq 2V_p$). At ~ 0.14 V, DELTT 3 then switches from peak to valley. The middle node voltage switches correspondingly as shown in Fig. 3(b). The measured two-peak I-V characteristic agrees well with our load-line analysis based on the measured I-Vs of the individual DELTTs, as shown in insets.

Complementary operation of these DELTTs was tested by applying an equal bias to gates on opposite sides for the two DELTTs, i.e. the backgate of DELTT 2 and the topgate of DELTT 3. (See Fig. 4(a).) The supply voltage is set at $\approx$ 0.12 V ($\geq 2V_p$), so that the two stable circuit operating points are near the I-V valley points of each DELTT, as shown in Fig. 4(d). The output (middle node) voltage and the circuit current, both as a function of gate input voltage, are shown in Fig. 4(b). V_{out} latches to ~ 0.045 V ('low') at $V_{in} \approx$ -0.13 V and to ~ 0.075 V ('high') at $V_{in} \approx$ 0.2 V, with hysteresis between the two states. By contrast, the circuit current stays almost constant at ~ 45 μA during the switching, qualitatively similar to Si-CMOS operation. The complementary operation of this circuit can be further analyzed by plotting the measured I-Vs of the individual DELTTs at representative V_{in} values, with the I-V of DELTT 3 serving as the load-line of DELTT 2. This is done in Fig. 4(c)-(e) for V_{in} = 0.3 V, 0 V and -0.2 V, respectively, with $V_{Supply} \approx$

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0.12 V. As expected, a positive V_{in} (0.3 V) raises the I-V curve of DELTT 3 while lowering that of DELTT 2, making the circuit latch to 'high', ~ 0.075 V. Similarly, the opposite behavior is observed with a negative V_{in} (-0.2 V), which latches the circuit to 'low', ~ 0.045 V. Thus, the output (middle node) voltage switches between bistable (high or low) values, but with one of the DELTTs always "off", i.e. operating near the valley point. Thus, the unipolar complementary operation of DELTTs is successfully obtained. In addition, due to the NDR of the DELTTs, the output for -0.13 V < V_{in} < 0.2 V is bistable and depends on its past history, as shown in Fig. 4(b). Hence these two series-connected DELTTs also constitute a complementary static RAM using half as many transistors as required in conventional CMOS. While the valley currents are relatively large in the present device, the use of different material systems with larger conduction band offsets should greatly improve the peak-to-valley ratio, as well as increasing the temperature of operation, making the DELTT more likely to find application in high-speed SRAMs.

In summary, unipolar resonant tunneling complementary circuits are demonstrated using two unipolar DELTTs connected in series. Due to the opposite effect on the NDR of the same topgate and backgate voltage, complementary circuits are achieved by connecting close-proximity gates on opposite sides for two DELTTs in series. The transconductance of an individual DELTT was analyzed in terms of both the quantum capacitance effect and the band-bending in a double quantum well structure, in good agreement with the device operation.

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[13] A contribution from the interlayer exchange interaction, significant at lower (typically $\leq 1 \times 10^{10}/cm^2$) carrier density, is negligible in the current DELTT device.

[14] Using our device values of $L_1 = 1160$Å, and $L_2 = 245$Å, we have $\lambda_{QC}^{-1} \approx 15$ meV/V. By simultaneously solving the Schrödinger and Poisson equations for our structure, we obtained $\Delta E_0 / \Delta V_{TC} \approx 20.5$ meV/V. Thus, assuming the many-body correction is negligible, the band-bending contribution is approximately 5 meV/V in these DQW structures. The gate leverage factor for the case of a single QW [12] can be obtained as $C_{Q,B} \rightarrow \infty$.

[15] The 2D-2D interlayer tunneling devices have asymmetric I-Vs with a resonance peak near $V_{SD} = \Delta E_0$. By contrast, double barrier resonant tunneling devices have roughly symmetric I-Vs due to their 3D-2D-3D tunneling structure.
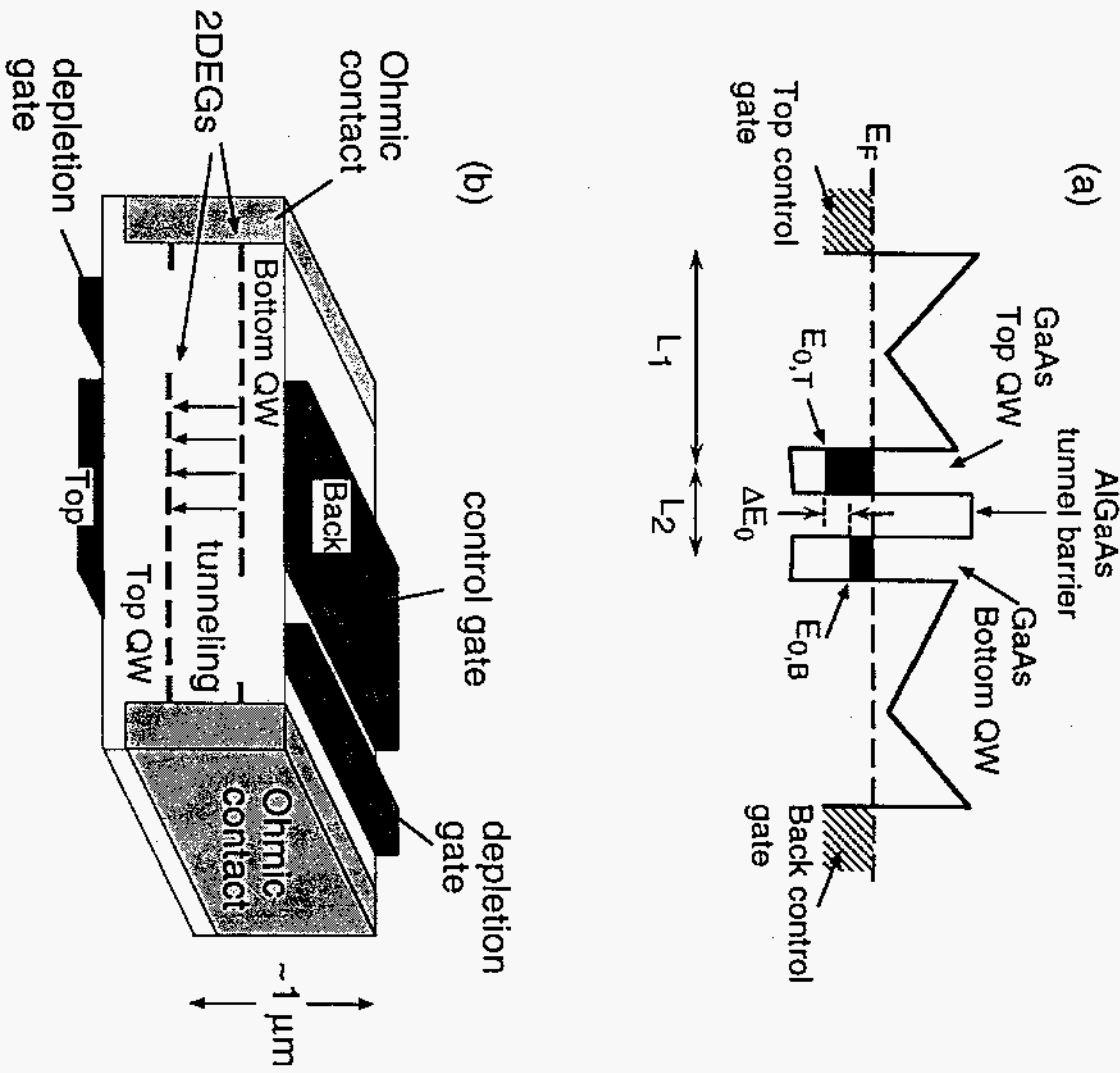
Figure Captions

Fig. 1. (a) Typical conduction band profile with no gate or source-drain bias. (b) Schematic diagram of the DELTT device structure, showing the two selectively contacted 2DEGs via a selective gate depletion technique, and top and back 'control' gates.
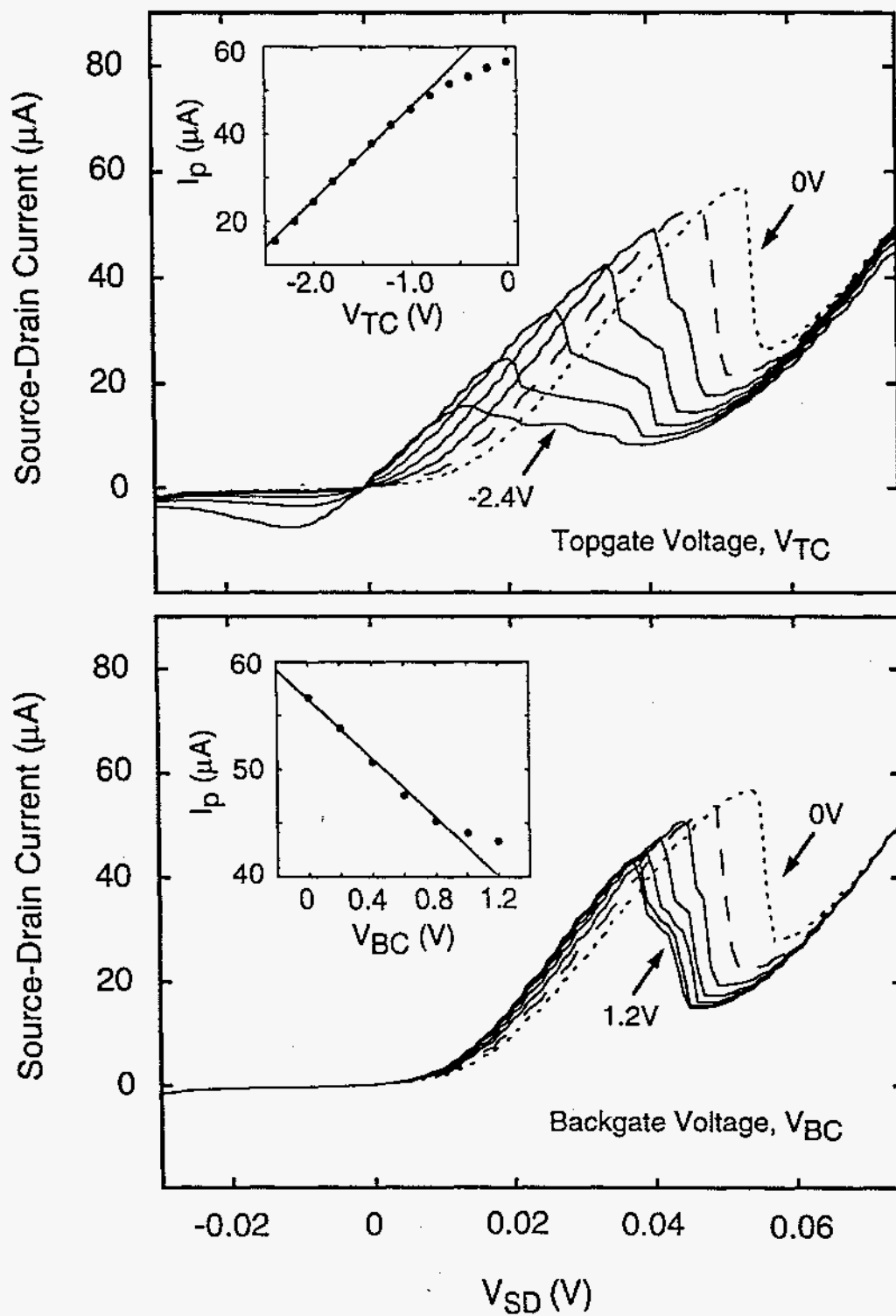
Fig. 2. Source-drain current I_{SD} vs. voltage V_{SD} characteristics of a single device, DELTT 2, measured at 77 K (a) for several values of V_{TC} changing from 0 V to -2.4 V with steps of -0.4 V, and (b) for several values of V_{BC} changing from 0 V to 1.2 V with steps of 0.2 V. The insets show how the peak current changes as a function of (a) V_{TC} and (b) V_{BC}.

Fig.3. (a) Circuit current vs. circuit supply voltage for two DELTTs connected in series, at 77 K. (b) The corresponding output (middle node) voltage vs. the supply voltage. The insets show the I-Vs of individual DELTTs overlaid at V_{supply} = 0.065 V, 0.115 V, and 0.150 V, respectively.

Fig. 4. (a) Connection of two DELTTs to form a unipolar complementary circuit, with the control gates of the two DELTTs located on opposite sides. (b) Output voltage V_{out} and circuit current as a function of input voltage V_{in} measured in the complementary circuit with a fixed supply voltage of 0.12 V. Hysteretic bistable switching in the voltage output is observed, while the circuit current stays almost constant. The individual I-Vs of both DELTTs in the complementary circuit are overlayed for (c) V_{in} = 0.3 V (d) V_{in} = 0 V, and (d) V_{in} = -0.2 V. See text for further discussion.

(a)

Top control gate

E_F

GaAs Top QW

AlGaAs tunnel barrier

$E_{0,T}$

L_1

L_2

ΔE_0

GaAs Bottom QW

$E_{0,B}$

Back control gate

(b)

depletion gate

2DEGs

Ohmic contact

Bottom QW

Back

Top

tunneling

Top QW

control gate

depletion gate

Ohmic contact

~1 μm

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APL, Fig. 1

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APL, Fig. 2

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APL, Fig. 4