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Unipolar Organic Transistor Circuits Made Robust by Dual-Gate Technology

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Unipolar Organic Transistor Circuits Made Robust by Dual-Gate Technology

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***Abstract*—Dual-gate organic transistor technology is used to increase the robustness of digital circuits as illustrated by higher inverter gains and noise margins. The additional gate in the technology functions as a $V_{\rm T}$-control gate. Both zero-$V_{\rm GS}$-load and diode-load logic are investigated. The noise margin of zero-$V_{\rm GS}$-load inverter increases from 1.15 V (single gate) to 2.8 V (dual gate) at 20 V supply voltage. Diode-load logic inverters show an improvement in noise margin from $\sim$0 V to 0.7 V for single gate and dual gate inverters, respectively. These values can be increased significantly by optimizing the inverter topologies. As a result of this optimization, noise margins larger than 6 V for zero-$V_{\rm GS}$-load logic and 1.4 V for diode-load logic are obtained. Functional 99-stage ring oscillators with 2.27 μs stage delays and 64 bit organic RFID transponder chips, operating at a data rate of 4.3 kb/s, have been manufactured.**

***Index Terms*—Dual-gate, organic circuits, organic RFID, organic transistor.**

I. Introduction

RESEARCH towards organic RFID tags is one of the drivers of organic electronics. In recent years, 64 bit organic RFID tags have been published with capacitive coupling [1] and inductive coupling at 13.56 MHz [2]–[4]. Recently, we reported a 128 bit organic transponder chip with basic anticollision protocol and Manchester encoding [2], [5]. In all these realizations, the most widespread technology is single-$V_{\rm T}$ p-type only. This technology has intrinsic limitations concerning integration of larger circuits, as a result of parameter variability [6]. The move towards an organic complementary technology [7], [8] is the most favorable route to obtain robust organic circuitry [9] and first 4 bit tags in complementary organic technology [7] have been made. This requires, however, matching of the n-type material in device performance. This matching has turned out to be difficult for close integration in complex circuits. Here, we present an alternative to improve the robustness of organic circuits [10]. It is based on p-type organic transistors equipped with a double gate [11]–[13]. The extra gate is used to vary the $V_{\rm T}$, which effectively leads to a dual-$V_{\rm T}$ p-type technology. The dual-gate transistor configuration allows to innovate the topology of logic gates. In this paper, we first discuss the logic families possible in unipolar organic electronics. Subsequently, dual-gate topologies are introduced and optimized topologies are selected. We show inverter topologies with substantially increased gain and noise margin [6]. Finally, we demonstrate a 64 bit organic RFID transponder chip based on these dual-gate organic thin-film transistors (OTFTs) for two different inverter topologies.

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II. Logic Families With Unipolar Logic

In p-type only organic electronics, inverters and NANDs are designed in zero-$V_{\rm GS}$-load logic or diode-load logic. Both schemes are depicted in Figs. 1 and 2. Both inverters comprise a drive transistor, which is the pull-up transistor in p-type logic and a load transistor, i.e., the pull-down transistor.

A. Zero-V_{GS}-Load Logic

In zero-$V_{\rm GS}$-load configuration, the gate and source nodes are shorted and effectively the load transistor is a current-source with a constant $V_{\rm GS}$-voltage of 0 V. As a consequence, this transistor needs to have a positive threshold voltage (depletion transistor), as shown in Fig. 1. The operation of the inverter can readily be understood as follows. For low $V_{\rm IN}$, the drive transistor is strongly on, in other words the channel resistance of this transistor in low, much lower than the channel resistance of the load transistor ($V_{\rm GS} = 0$ V). Therefore, the resistive divider between the load and drive transistors sets $V_{\rm OUT}$ close to $V_{\rm DD}$. In the other case, when $V_{\rm IN}$ is high, the drive transistor has a gate-source voltage close to 0 V. Therefore, the dimensions (W/L) of the load transistor are chosen significantly (e.g., 5 to 10 times) larger than those of the drive transistor. Now, the resistive divider between the load and drive transistor pulls $V_{\rm OUT}$ close to 0 V. For these inverters, non-idealities are present, being the swing of $V_{\rm OUT}$ that is smaller than 0 to $V_{\rm DD}$, caused by the leakage current of the drive and load transistors which are always "on". Another non-ideality is the asymmetrical trip point that is not at $V_{\rm DD}/2$ caused by the equal threshold voltages of both drive and load transistors. A typical measured inverter is shown in Fig. 1. The single gate inverter in this work yields a

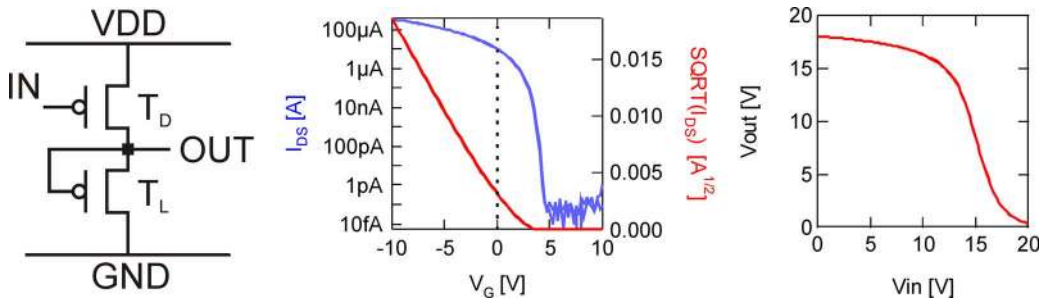

Fig. 1. (left) Schematics of zero-$V_{\rm GS}$-load inverter with unipolar p-type logic. (middle) $I_{\rm DS}$–$V_{\rm GS}$ transfer characteristic of a depletion-mode, p-channel OTFT with positive threshold voltage. (right) Typical measured transfer characteristics of a zero-$V_{\rm GS}$-load inverter.

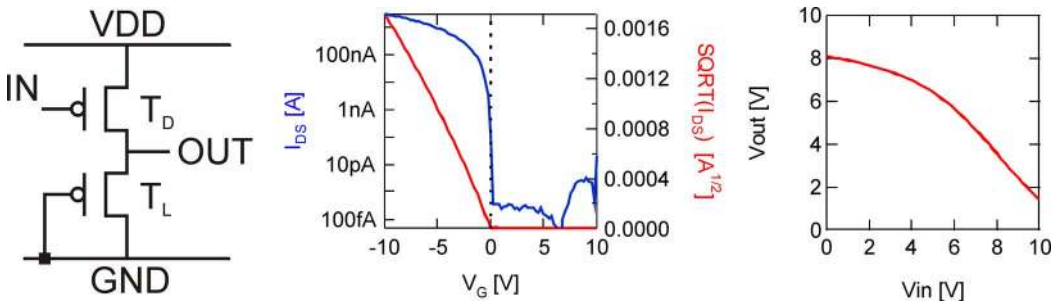

Fig. 2. (left) Schematics of diode-load inverter with unipolar p-type logic. (middle) $I_{\rm DS}$-$V_{\rm GS}$ transfer characteristic of an enhancement-mode, p-channel OTFT with negative threshold voltage. (right) Typical measured transfer characteristics of a diode-load inverter.

noise margin of 1.15 V at a supply voltage of 20 V. Its gain is 3.90.

B. Diode-Load Logic

Fig. 2 shows the configuration of a diode-load inverter. The gate and drain nodes of the pull-down transistor are connected, resulting in a diode-connected transistor. This configuration is, in contrast to the zero-$V_{\rm GS}$-load configuration, compatible with enhancement-mode transistors [14] (Fig. 2) and mildly depletion-mode transistors [15]. This type of logic therefore has some more robustness against large threshold-voltage variations of the load transistor and it provides faster circuits [1]. The inverters yield lower gains than the zero-$V_{\rm GS}$-load inverters, resulting in severely reduced noise margins, as indicated by the characteristics of a diode-load organic inverter of Fig. 2. The swing of $V_{\rm OUT}$ in this logic is also smaller than 0 to $V_{\rm DD}$. In order to be able to integrate more logic gates in a circuit, the use of level-shifters has shown to be successful to improve the noise margin of diode-load inverters [1]. A level-shifter is an additional stage which requires a third voltage rail. This circuit results in a shift of the transfer characteristics of the inverter. This is testified by the demonstration of relatively large circuits with this configuration [16]. A major advantage of diode-load logic is an increased speed compared to zero-$V_{\rm GS}$-load logic. As a consequence of using a diode-connected transistor as load, this OTFT yields large pull-down currents leading to a decreased stage delay for diode-load gates versus zero-$V_{\rm GS}$-load gates, in which the pull-down action is speed limiting.

III. Circuitry With Dual-Gate OTFTs

So far, we have discussed organic unipolar circuitry with one threshold voltage. The availability of a second threshold voltage would be beneficial for the characteristics of building blocks for digital circuits, similar to the silicon n-MOS logic used in the 1980s. One option to obtain multiple threshold voltages is the addition of a second gate in the technology. The organic dual-gate TFT technology that is used in this work is described elsewhere [17], [18]. The organic insulator layers and the p-type pentacene semiconductor are processed from solution. The transistors have a typical channel length of 5 μm and an average saturation mobility of 0.15 $\rm cm^2/Vs$. A cross section image of the layers and a typical measured dual-gate OTFT are shown in Fig. 3. The coupling to the channel of the second or back-gate is weaker than for the front-gate, therefore it is used as $V_{\rm T}$-control gate. By varying the back-gate bias between $+30$ V and -30 V, the transistor threshold voltage can be controlled, leading from depletion-mode to more enhancement-mode curves, in agreement with earlier publications [18], [19].

In this section, we investigate both architectures of inverters discussed previously for a technology where both the load and drive transistors have a back gate available. The electric schemes are depicted in Figs. 4 and 5. The $V_{\rm T}$-control gate is denoted with the subscript 'BG'. The ratio between the drive and load transistor for the diode-load logic is 10:1, however we have found that the zero-$V_{\rm GS}$-load logic can be designed with a 1:1 ratio resulting in a significantly smaller chip area. Figs. 4 and 5 depict contour plots of noise margin and trip point when varying the $V_{\rm T}$-control gate voltage of the drive and load transistor for both inverter topologies. As can be seen, noise margins can exceed 2.8 V for zero-$V_{\rm GS}$-load inverters and 0.7 V for diode-load inverters at $V_{\rm DD} = 20$ V. The trip point can be shifted towards $V_{\rm DD}/2$ (i.e., 10 V) for both designs by appropriate $V_{\rm T}$ control.

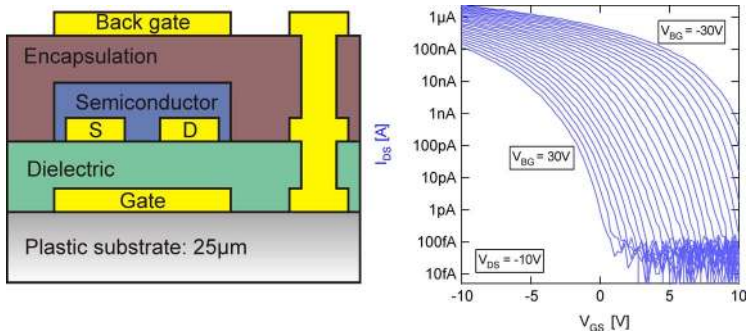

Fig. 3. Cross-section of the dual-gate OTFT technology (left) and a typical measured transfer characteristic of this OTFT when using the back-gate as V_{T}-control gate (right). The channel width equals 140 μm, the channel length 5 μm.

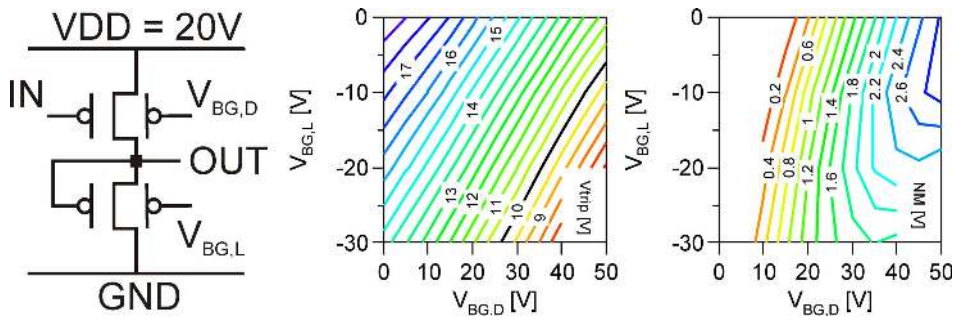

Fig. 4. Architecture of a dual-gate zero-V_{GS}-load inverter (left). Contour plots of the trip point (middle) and the noise margin (right) determined from measured transfer curves of inverters when varying the back-gate voltage of the load and drive transistor and applying a supply voltage of 20 V.

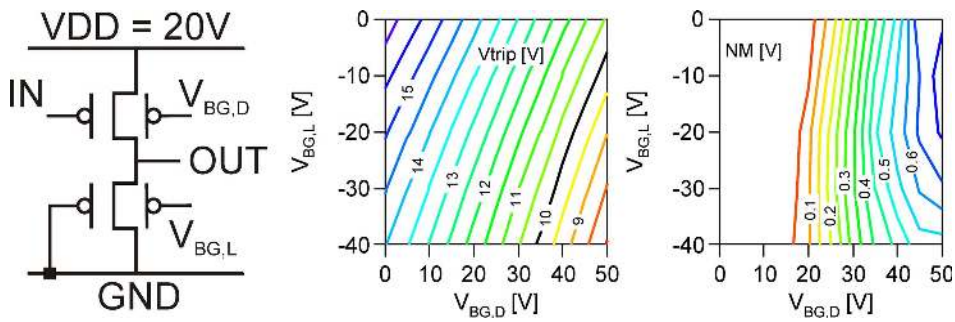

Fig. 5. Architecture of a dual-gate diode-load inverter (left). Contour plots of the trip point (middle) and the noise margin (right) determined from measured transfer curves of inverters when varying the back-gate voltage of the load and drive transistor and applying a supply voltage of 20 V.

Next, besides the inverter topologies of Figs. 4 and 5, we have fabricated and measured 19-stage ring oscillators, designed using the dual-gate zero-V_{GS}-load inverter architecture with a 1:1 ratio. Fig. 6 shows the obtained frequency when varying back gate of the drive and load transistor. A frequency range between 3 kHz and 24 kHz has been obtained. The influence of the threshold voltage of the drive transistor is much weaker than the influence of the threshold voltage of the load transistor, which delivers the small pull-down current to discharge the input capacitance of the next stage. The variation of the back-gate is a viable route to increase the frequency of the dual-gate zero-V_{GS}-load circuits.

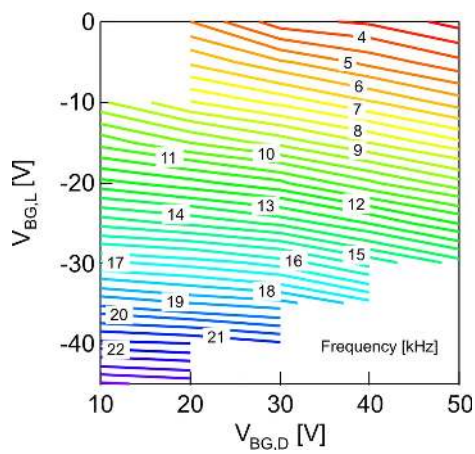

Fig. 6. Contour plot of the frequency determined from measured curves of 19-stage ring oscillators using the dual-gate zero-V_{GS}-load architecture (Fig. 4) when varying the back-gate voltage of the load and drive transistor and applying a supply voltage of 20 V.

IV. Enhanced Dual-Gate Architecture

One disadvantage of previous dual-gate configurations is that the threshold voltage of the load transistor changes dynamically with the output node, since this node is also the source-contact for the back gate transistor. The threshold voltage moves in opposite direction as required for high gains when the output node

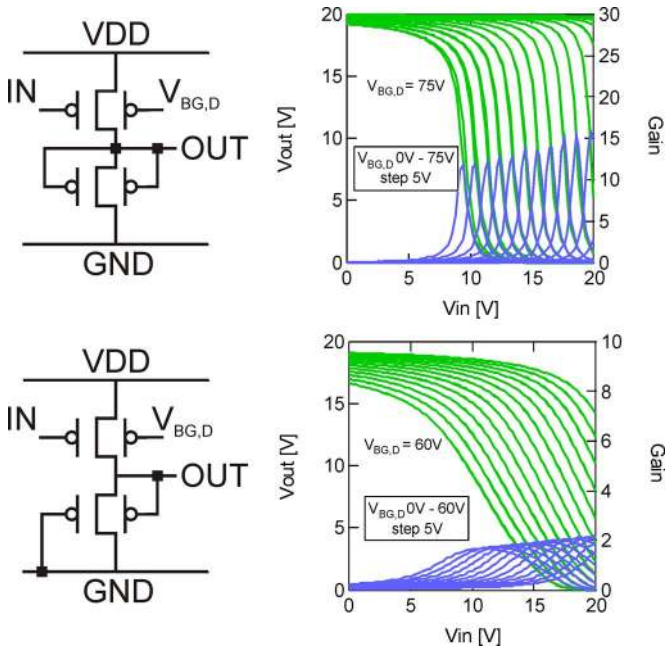

Fig. 7. Architecture of optimized inverter architectures in dual gate technology for (top left) zero-V_{GS}-load inverter and (bottom left) diode-load inverter. Transfer curves of these inverters are plotted for a supply voltage of 20 V, as a function of the voltage on the V_{T}-control gate of the drive transistor (right).

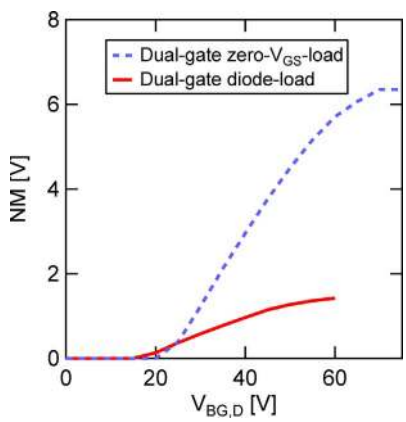

Fig. 8. Extracted noise margin for both zero-V_{GS}-load and diode-load inverter logic as function of the back-gate voltage of the drive transistor.

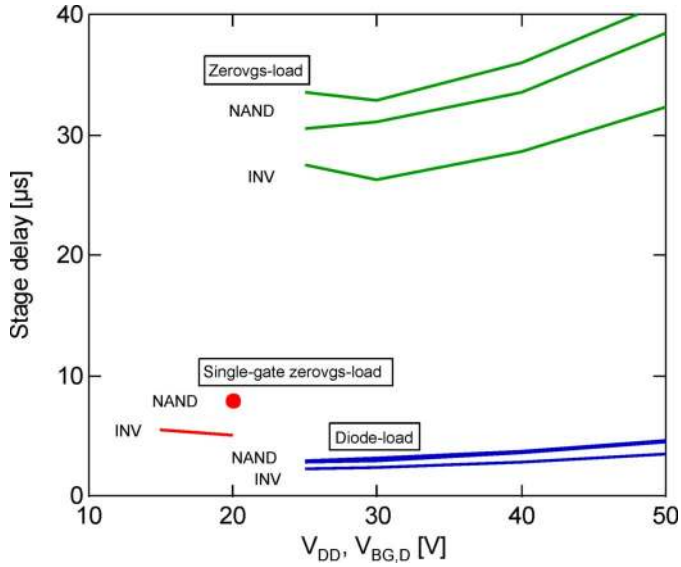

Fig. 9. The stage delay is plotted as a function of the V_{T}-control voltage of the drive transistor ($V_{\mathrm{BG,D}}$) for optimized zero-V_{GS}-load and diode-load inverters for a supply voltage of 20 V. The stage delay of a single-gate zero-V_{GS}-load inverter is shown for reference. This stage delay is plotted as a function of the power supply voltage (V_{DD}).

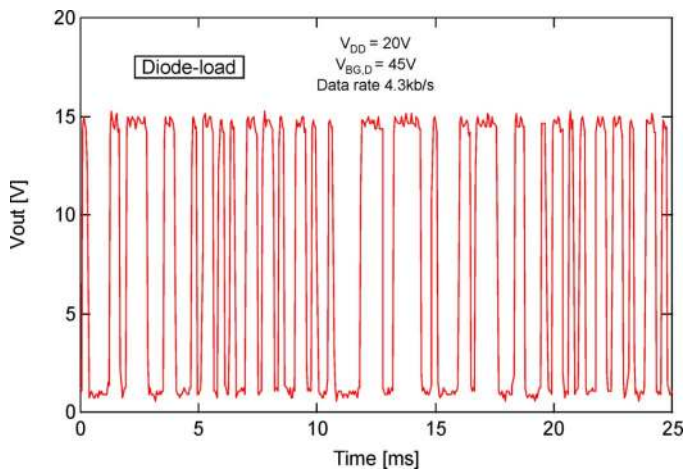

Fig. 10. The output signal of a 64 bit organic RFID transponder chip with optimized diode-load configuration for a supply voltage of 20 V and a back-gate voltage of 45 V. The corresponding data rate is 4.3 kb/s.

varies. In other words, the load transistor is made dynamically weaker when it should pull the output node down. Therefore, we have found an optimized architecture. Connecting the back-gate of the load with the output node delivers a topology that leads to increased noise margin and gain (see Fig. 7). The transfer curves of zero-V_{GS}-load and diode-load inverters using this optimized topology are depicted in Fig. 7.

De Vusser *et al.* [6] showed that, for zero-V_{GS}-load logic, a linear increase in noise margin is directly proportional to a V_{T}-difference between load and drive transistor. In our topology, this V_{T}-difference is obtained by a back-gate voltage difference between load and drive TFT. Fig. 3 depicts that, in our device configuration, the threshold voltage shifts with about 35% of the applied back-gate voltage. This yields an increase in noise margin of 16% of the applied back-gate voltage, as can be seen in Fig. 8. For the diode-load logic, a much smaller increase in noise margin (4%) is obtained with the change in the back-gate voltage. The V_{T}-control gate of the drive transistor can be used to move the trip point towards $V_{\mathrm{DD}}/2$ (see Fig. 7). At this point, in zero-V_{GS}-load inverters, the gain exceeds 11 and the noise margin is larger than 6 V at $V_{\mathrm{DD}} = 20$ V. Importantly, the typically low gain of diode-load inverters increases to 2.

In order to demonstrate that organic p-type only dual-gate technology can obtain a high integration density, we made 99-stage dual-gate ring oscillators with zero-V_{GS}-load and diode-load architectures. In Fig. 9, we show the extracted stage delays of NAND-gates and inverters, using the topologies of Fig. 7, and compare them to reference single-gate zero-V_{GS}-load gates fabricated on the same foil. The fastest family is the optimized diode-load topology, with a stage delay of 2.27 μs. The optimized zero-V_{GS}-load topology is an order

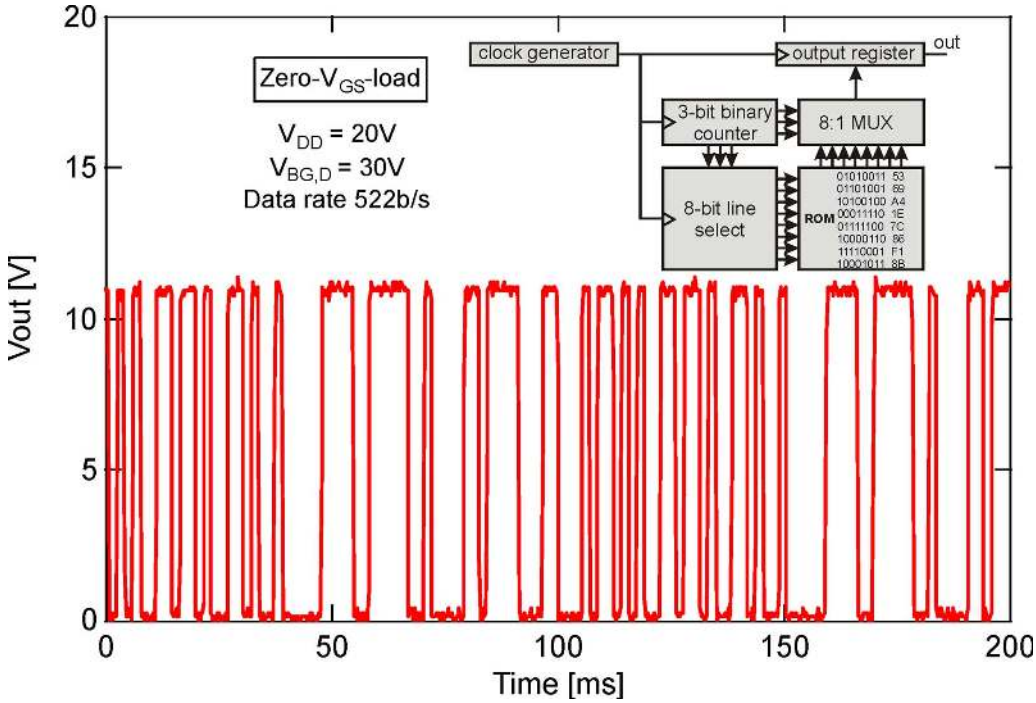

Fig. 11. The output signal of a 64 bit organic RFID transponder chip with optimized zero-$V_{\rm GS}$-load configuration for a supply voltage of 20 V and a back-gate voltage of 30 V. The corresponding data rate is 522 b/s.

of magnitude slower ($\tau_{\rm stage} = 26\ \mu$s), due to limited pull-down current and the high parasitic output-capacitance.

V. Organic RFID Transponder Chip With Enhanced Dual-Gate Architecture

Next, we fabricated 64 bit RFID transponder chips similar to earlier designs [2]. To secure accurate clocking, we increased the size of the ring oscillator that generates the clock from 19 to 33 stages. The inset of Fig. 11 shows the digital schematic of the RFID transponder chip. The ring oscillator generates the clock signal when powered. This clock signal is used to clock the output register, the 3-bit binary counter and the 8-bit line select. The 8-bit line select has an internal 3-bit binary counter and a 3-to-8 decoder. This block selects a row of 8 bits in the code. The 3-bit binary counter drives the 8:1 multiplexer, selecting a column of 8 bits in the code matrix. The data bit at the crossing of the active row and column, is transported via an 8:1 multiplexer to the output register, which sends out this bit on the rising edge of the clock. The 3 bits of the 3-bit binary counter are also used in the 8-bit line select block for selecting a new row after all 8 bits in a row are transmitted. The design is made using only inverters and NAND-gates. For the optimized diode-load logic, the ratio between drive and load transistor is 10:1 leading to a transponder chip area of 74.48 mm^2. Fig. 10 shows the output signal of the chip designed in optimized diode-load topology for $V_{\rm DD} = 20$ V and $V_{\rm BG,D} = 45$ V. The data rate is 4.3 kb/s, more than twice the fastest single gate transponder chips shown in [2] and [5]. We verified on three different wafers that some chips start operating at $V_{\rm DD}$ as low as 10 V and all chips work at 15 V.

The 64 bit transponder chip in optimized zero-$V_{\rm GS}$-load topology is only 45.38 mm^2 in size, thanks to the 1:1 ratio used in this logic. In Fig. 11, the output is shown for $V_{\rm DD} = 20$ V and $V_{\rm BG,D} = 30$ V. Also this transponder chip has been measured on three different wafers. All measured transponder chips are operational at $V_{\rm DD} = 10$ V. The data rate at $V_{\rm DD} = 20$ V is 522 b/s. These findings are fully in line with the fact that the zero-$V_{\rm GS}$ topology has higher noise margin but larger stage delay than the diode-load topology. Fig. 12 shows a photograph of both 64 bit transponder chips.

For comparison, a 64 bit transponder chip having single-gate zero-$V_{\rm GS}$-load logic has also been fabricated. The onset voltage, more precisely the minimal supply voltage at which the transponder is functional, on the three wafers differs between 20 V and 26 V. These onset voltages for power supply are comparable to the second generation transponder chips published by Myny *et al.* [2], [5]. As mentioned earlier, the dual-gate technology allows to lower the supply voltage, even to 10 V, which is the lowest value reported to-date for 64 bit transponder chips.

The back-gate voltages of the drive transistors are relatively high, 30 to 45 V. In an organic RFID transponder, such high voltage cannot be generated by a rectifier. However, it can be generated by charge pumps, provided that the required current is limited. To verify whether that last assumption is realistic, we have operated the chips with a 1-nA current compliance for the voltage supply of the back gate of the driver transistor. All chips were fully operational after a delay to charge all back gates. This delay was about 2.09 s for the diode-load configuration and only 246 ms for the zero-$V_{\rm GS}$-load configuration. The output signal measured in latter circuit is plotted in Fig. 13. The difference in delay time is due to the fact that the drive transistor is 10 $\times$ larger for the diode-load (ratioed) than the zero-$V_{\rm GS}$-load configuration. We conclude that charge pumps are a viable route

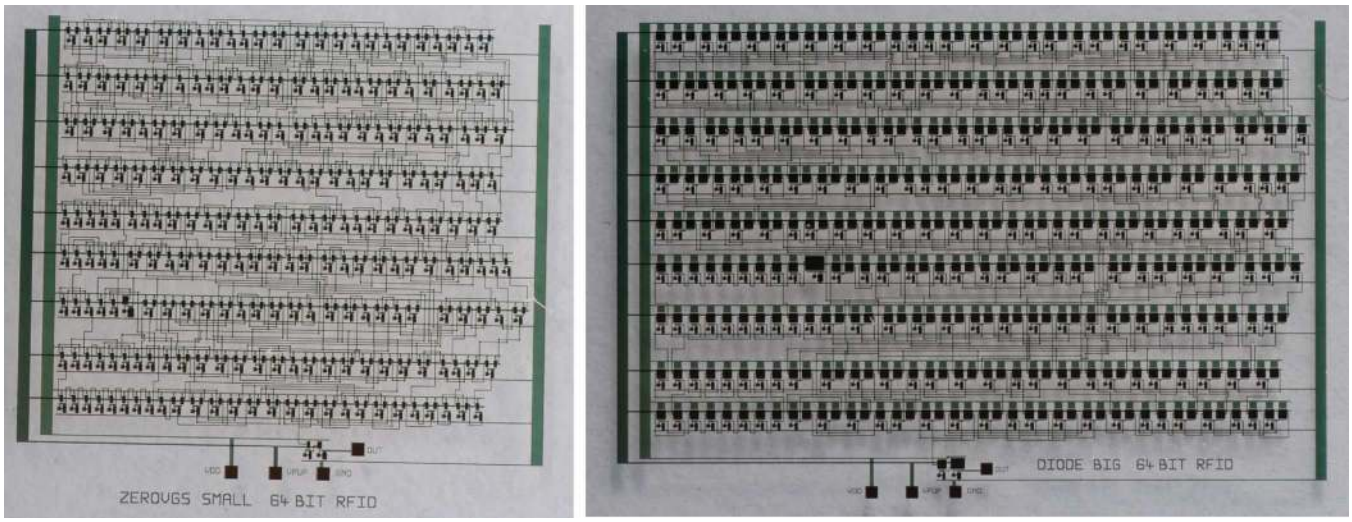

Fig. 12. Photograph of the 64 bit organic RFID transponder chip designed with optimized zero-V_{GS}-load configuration (left) and optimized diode-load configuration (right).

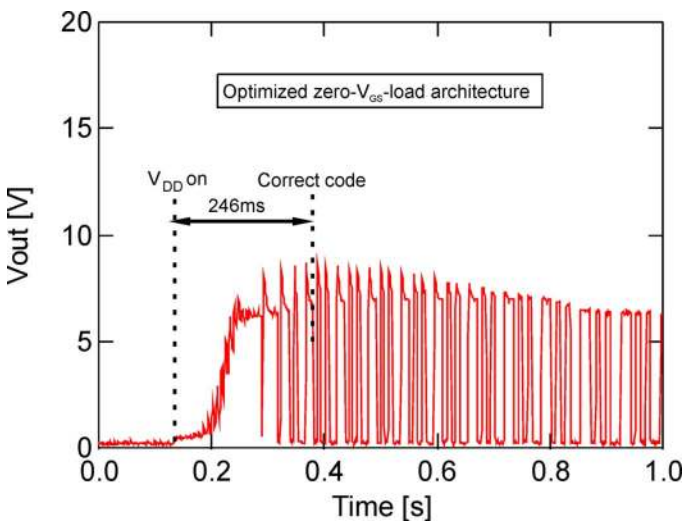

Fig. 13. The output signal of an 8 bit organic RFID transponder chip with optimized zero-V_{GS}-load configuration for a supply voltage of 20 V and a back-gate voltage being charged towards 50 V at a current compliance of 1 nA.

to charge the back gates of the logic blocks of the proposed dual-V_T technology. A better solution to enable lower back-gate voltage levels can be found in technology improvements targeting a higher oxide capacitance of the back-gate dielectric. This can be achieved by means of e.g., a thinner back-gate dielectric. A drawback of this solution is a limited performance in terms of stage delay of logic gates due to an increased output capacitor for the enhanced dual-gate architecture.

VI. Conclusion

In this work we have demonstrated that a dual-gate OTFT technology is a realistic option to increase the robustness of digital building blocks for larger integration into circuitry. Therefore, dual-gate zero-V_{GS}-load and diode-load logic are investigated. For both topologies, noise margins and trip points could be improved when varying the back-gate voltage for the drive and load transistor. Next, an optimized design for both topologies is found. The new design is used to integrate 99-stage ring oscillators, to determine stage delays, and in 64 bit organic RFID transponder chips, yielding data rates of 4.3 kb/s. This is, to our knowledge, the first integration of a dual-gate OTFT technology in complex digital circuits.

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