Use of High-Speed Microprocessors for Digital Synthesis

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This paper describes a processor specialized for the synthesis and treatment of sound signals, realized with bipolar bit-slice microprocessors. This processor has been studied at the Musical Department of I.N.A., within a project aiming at the development of digital systems for sound processing with real-time control (SYTER Project). A prototype has been built with the help of Denis Valette. The main characteristic of this processor is that it is completely programmable, which makes it possible to use many existing methods of synthesis or to adapt it to new methods, without modifying the hardware. Three other points have also been crucial for the conception of the processor:

– the possibility of directly treating sounds sampled by an analog-to-digital converter.

– the possibility of connecting several units in a multiprocessor structure to multiply the capacity of treatment of each processor.

– a simple interface with the control system.

For this purpose, all the data controlling the functioning of the processor is stored in a dual-port memory which can be used as a main memory block by a microprocessor or a minicomputer.

General Structure

Fundamentally, the SYTER digital processor is a microprogrammable 16-bit machine. There are two data paths, A and B. (Figure 1). The arithmetic and logic unit (ALU) is composed of 16 general-purpose registers accessible to the user, while multiplications in the system are carried out by

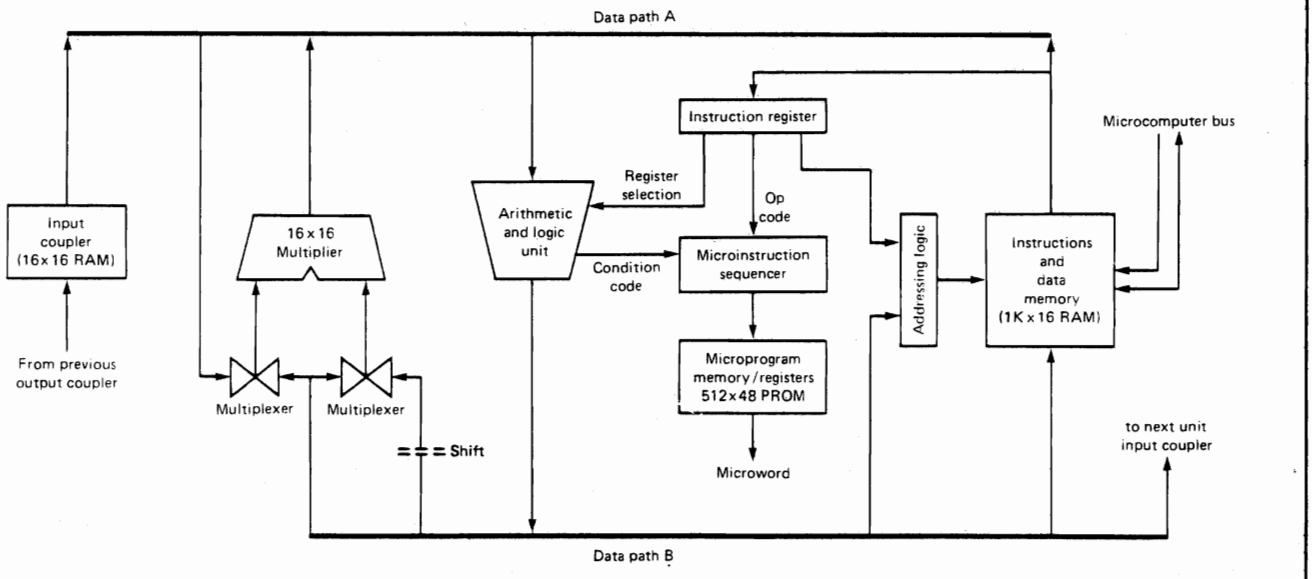

Figure 1. General Structure

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a 16-bit × 16-bit multiplier (TRW MPY 16). Special shift circuits (for the multiplier and the RAM) have been constructed for the manipulation of the fixed-size function tables (of 64 words at present). Intermediate registers (not on the figure) allow the simultaneous execution of several elementary operations.

Instruction Set

There are three *general* modes of memory addressing: immediate, direct, and indexed by a general-purpose register, plus a *special* mode allowing the use of a 64-word array beginning at an address multiple of 64. Every instruction is coded on a 16-bit word divided into four fields of four bits each with four possible formats. (Figure 2).

The instruction set, (Figure 3) which was realized by microprogramming includes:

– a minimal set of "classical" instructions similar to those of a microcomputer: arithmetical and logical instructions, transfers, connections, *etc*.

– special instructions designed for the treatment of the signal.

This instruction set also allows for experimentation with various synthesis methods before later translating the corresponding instructions into microcode for faster execution.

Control of the Treatment

Access to the main memory is realized by an external bus. This access is transparent and does not affect the functioning of the processor. The basic sampling rate is programmable and corresponds to an execution range going from 32 to 256 microcycles, that is to say, at present: 20 Khz $\leqslant S \leqslant$ 160 Khz.

At the beginning of each cycle, control is transferred to an address among 16 stored at the beginning of the memory (Figure 4). Thus, certain control sub-sequences can be executed at frequencies which are a multiple of $S/16$ (envelope generation, for example). Moreover, the connecting instructions can – if required – transfer control to certain instruction sequences co-resident in the memory, which makes high-

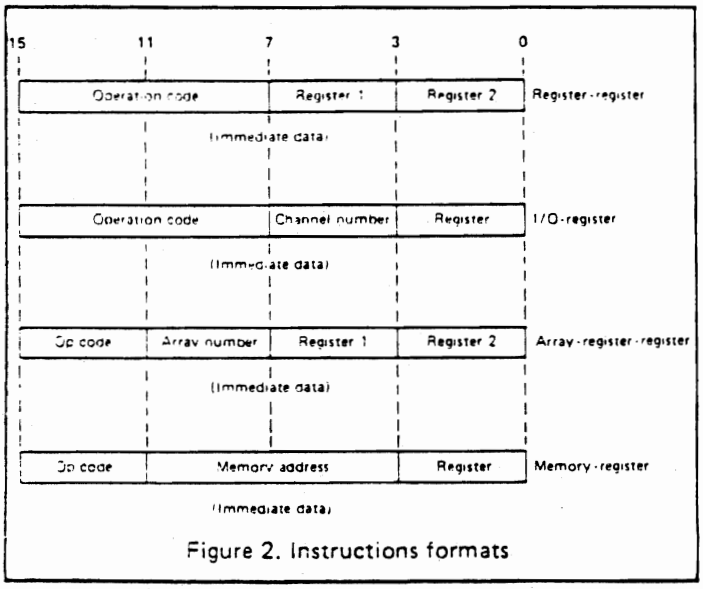

Figure 2. Instructions formats

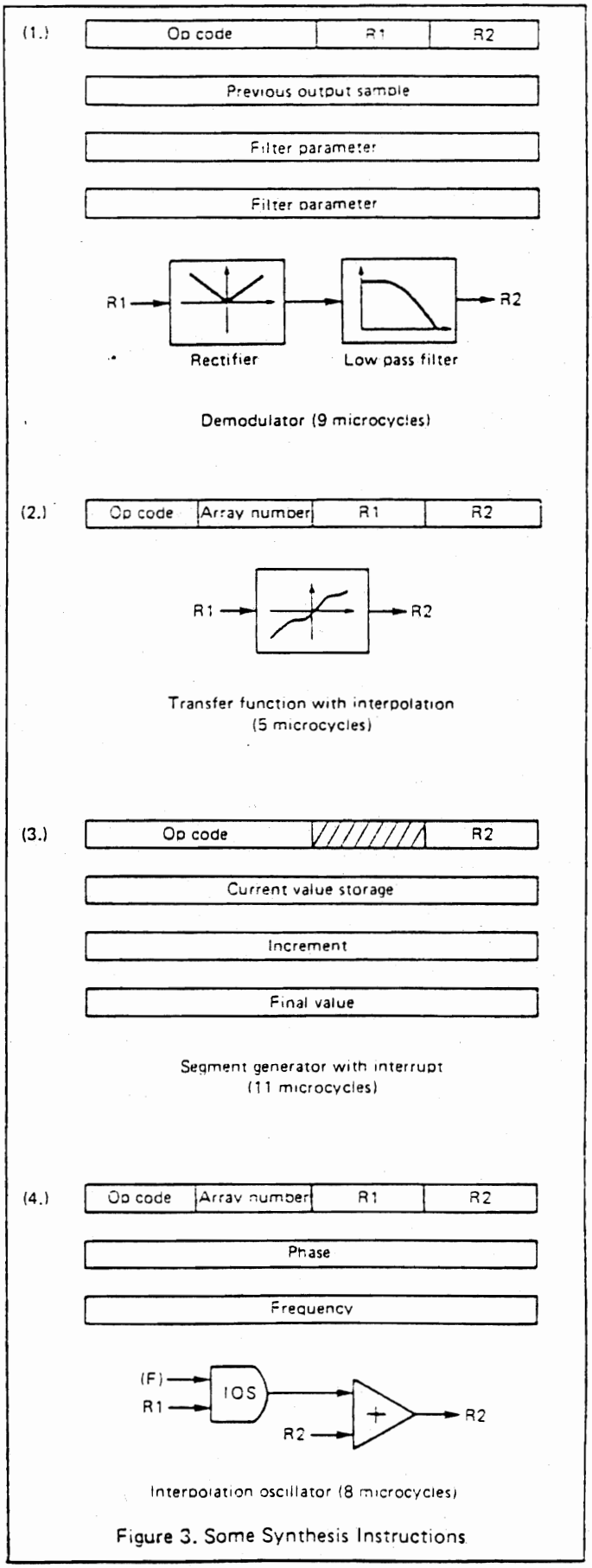

Figure 3. Some Synthesis Instructions

speed commutation of several synthesis programs possible. The execution of an instruction may set a flag, thus sending an interrupt request to the external bus. The address of the instruction is then stored in the first word of the memory and further requests are masked until this word is demanded by the external control system.

Present Realization

The prototype which was built includes 120 IC's distributed on three cards. The basic cycle is 200 nS, which permits for example the realization of 16 randomly connected linear interpolation oscillators and the corresponding envelope controls (sampling rate: 30 Khz). The experimentation system (Figure 5) includes a Motorola 6800 microprocessor which controls a chain composed of an analog-to-digital converter multiplexed on four channels, one or several synthesis processors and four 16-bit digital-to-analog convertors.

Possible Extensions

The accuracy of 16 bits in fixed-point arithmetic seems sufficient for most cases, except for complex filter realizations. Although it is possible to make calculations in double precision, the resulting drop of performance seems generally prohibitive. The calculation power of the processor is mainly limited by the speed of the bipolar microprocessors (AMD 2901). If we work with more recent versions of the 2901, it seems possible to multiply this power by a factor of almost two. For this purpose, we are studying at the moment the realization of a new version using the same architecture. This processor would have a larger memory, a 24-bit word size, and use about 140 LSI and MSI circuits on a unique card of greater dimensions. This processor could be the basic element of a system composed of up to 16 daisy-chained units, following the afore-described principle.

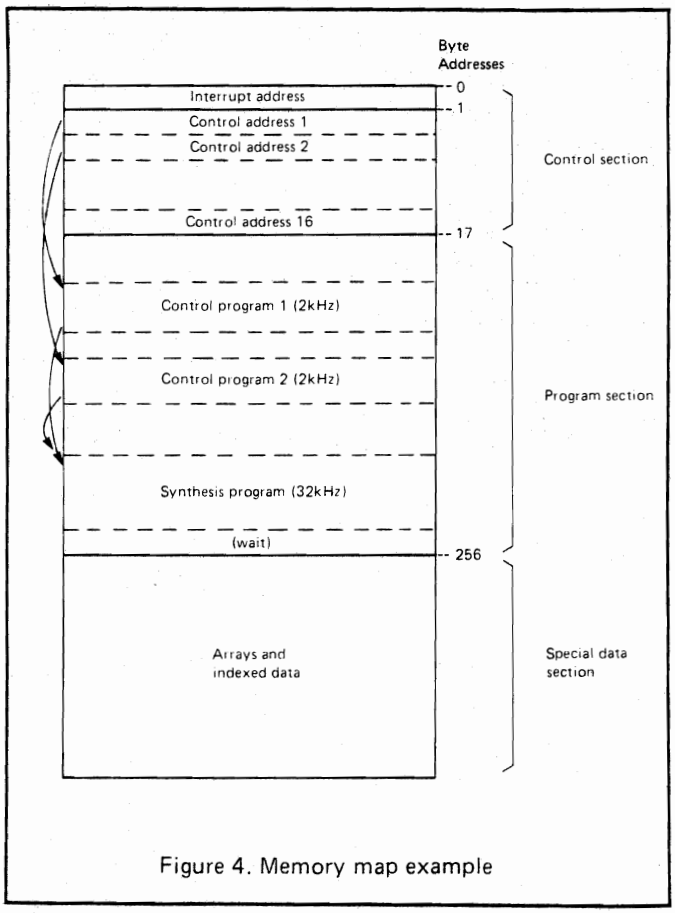

Figure 4. Memory map example

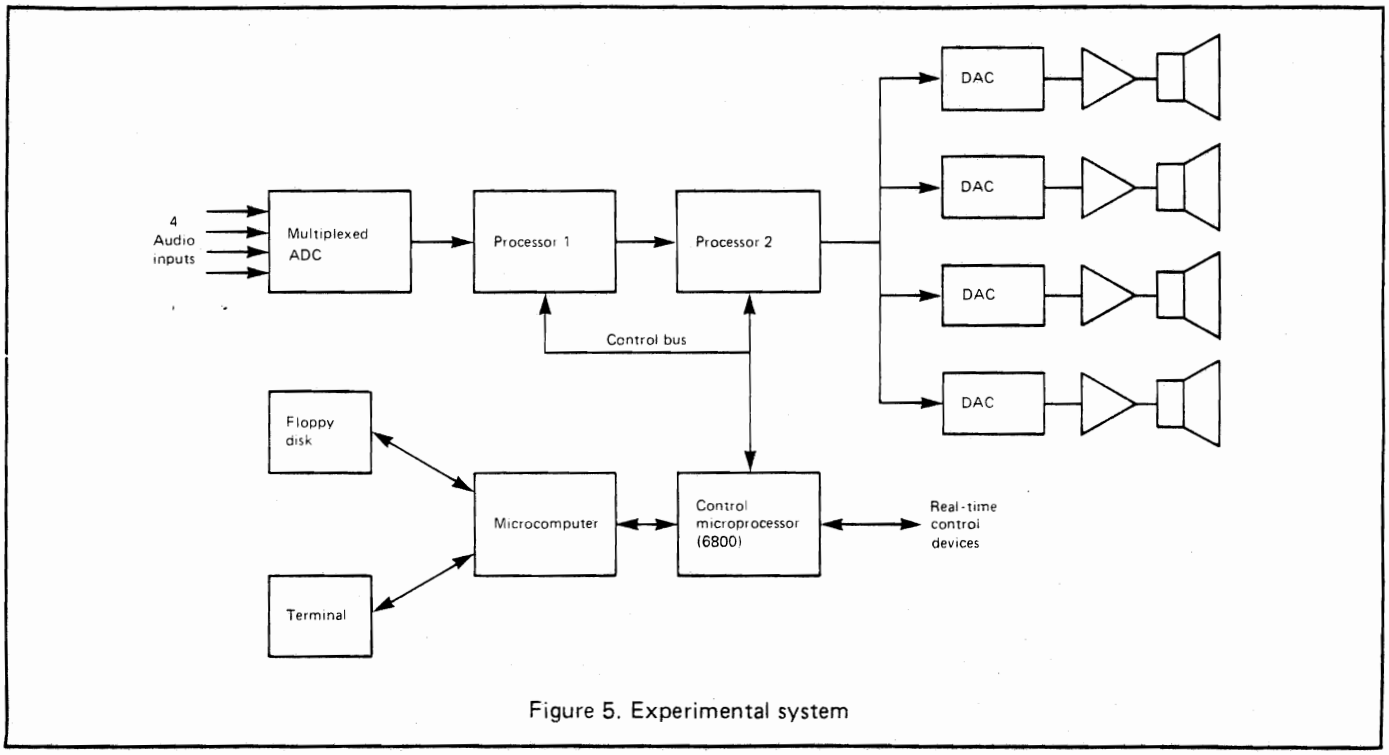

Figure 5. Experimental system