USING BULK BUILT-IN CURRENT SENSORS TO DETECT SOFT ERRORS

CONNECTING A BUILT-IN CURRENT SENSOR IN THE DESIGN BULK OF A DIGITAL SYSTEM INCREASES SENSITIVITY FOR DETECTING TRANSIENT UPSETS IN COMBINATIONAL AND SEQUENTIAL LOGIC. SPICE SIMULATIONS VALIDATE THIS APPROACH AND SHOW ONLY MINOR PENALTIES IN TERMS OF AREA, PERFORMANCE, AND POWER CONSUMPTION.

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Integrated circuits operating in space applications are susceptible to radiation effects that can be permanent or transient.[1] Various energetic particles in the space radiation environment can interact with silicon to cause undesirable effects. When a single heavy ion strikes silicon, it loses its energy by creating free electron-hole pairs, resulting in a dense ionized track in the local region. Protons and neutrons can cause nuclear interactions when passing through the material. The recoil also produces ionization, which generates a transient current pulse that can cause an upset when interpreted as a signal in the circuit. With technology scaling into deep-submicron dimensions, the effects of energetic particle hits become a concern even at sea level, where the major high-energy radiation source is atmospheric neutrons and protons.

A single particle can hit either the sequential logic or the combinational logic in the silicon. When an energetic particle strikes one of a memory cell's sensitive sites, the effect can produce an inversion in the stored value—in other words, a bit flip in the memory cell. This is called a single-event upset (SEU).[2] When an energetic particle hits a sensitive site in the combinational logic block, it also generates a transient current pulse. This phenomenon is called a single-event transient (SET).[3] For combinational logic blocks with registered outputs, the SET can eventually appear at the input of the flip-flops placed at the combinational logic outputs, unless the induced transient pulse is either logically or electrically masked by the logic inputs. If interpreted as a valid signal in the register input, this SET can cause an incorrect value to be stored in the register, provoking a soft error.

Continuous technology evolution and smaller transistor features have made soft errors on devices more frequent. Detecting soft errors in combinational and sequential logic is critical for avoiding errors in the circuit application. However, this task is complex because the internal circuit signals are decreasing to the same order of magnitude as the transient currents generated by charged-particle strikes.

Researchers have proposed a built-in current sensor (BICS) connected to the power lines for monitoring on-chip current variations provoked by permanent faults, such as stuck-at faults, and by soft errors in memory elements.[4,5] However, to the best of our knowledge, no one has yet proposed a BICS-based method for detecting SETs in combinational logic, and this issue is gaining importance in new technologies. We propose an approach for using BICS to detect transient

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upsets in sequential *and* combinational logic. The BICS connects to the transistors' design bulk—an arrangement we call *bulk-BICS*—which increases the sensor's sensitivity to detect any discrepancy in a circuit's internal current that might occur during a particle strike. This approach helps in two ways: First, the BICS can distinguish SETs from internal logic signals and consequently detect them, while the BICS connected to the power lines cannot. Second, bulk-BICS has a minor effect on performance and power dissipation, compared with a BICS connected to the power lines.

We used 100-nm CMOS technology to design the bulk-BICS and the circuits in our case studies, and SPICE simulation validated the detection capability. Our results show that bulk-BICS has high detection sensitivity to SEUs and SETs and a negligible effect on performance.

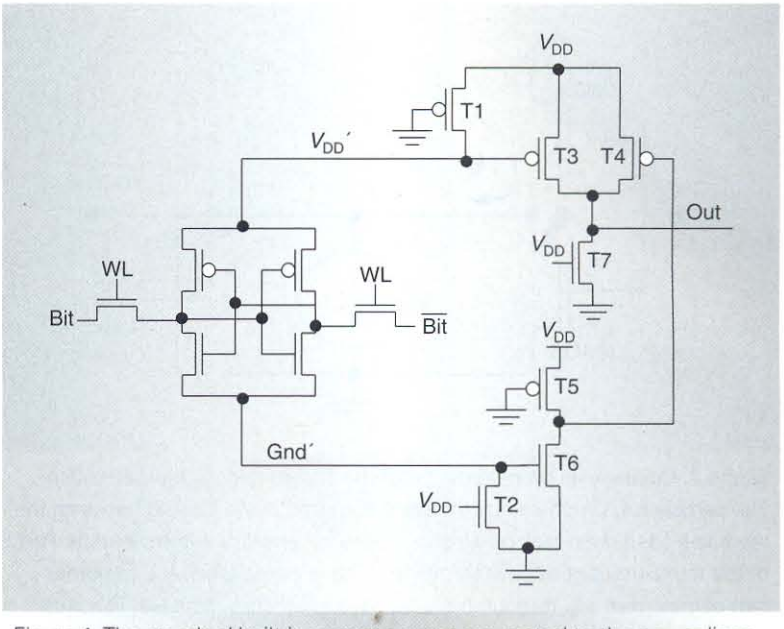

Figure 1. The standard built-in current sensor connected to the power lines of a SRAM cell.

The bulk-BICS approach

An efficient SEU and SET detection method is mandatory for evaluating an IC's sensitivity and to guarantee its reliability. Researchers proposed BICS for monitoring on-chip SEUs because a BICS presents fewer penalties than error correcting code, and experiments have shown that asynchronous BICS can detect SEUs in memories.[4,5] This approach places the BICS on a memory's power lines.

The BICS cited by Vargas and Nicolaidis[4] appears in Figure 1, where a memory cell is the circuit under test. Without current in the virtual power bus (V_{DD}' and Gnd'), the voltage level on the gate of transistor T3 is V_{DD} and that on the gate of T6 is Gnd. A charged particle striking the silicon can cause two situations, and in both cases the voltage level on the BICS output increases, producing a positive output. The first case is when the upset results from a particle that charges the drain of a PMOS device that is off, thereby charging the T6 gate to a voltage greater than Gnd. The second case is when the upset results from a particle that discharges the drain of an NMOS device that is off, thereby discharging the T3 gate to a voltage smaller than V_{DD}.

This is an efficient solution for sequential circuits, but it doesn't work for combinational logic because BICS connected to the power line cannot efficiently differentiate internal signals propagating through the logic from SETs (upsets). Detecting transient upsets in the combinational logic is much more complex because it requires evaluation of the intensity of the pulse generated by the charged-particle strike. Previous work proposed logic duplication, time redundancy, and extra transistors for SET detection.[6] These methods require costly design modification. Our method uses BICS connected to the bulk of the transistors; this reduces area, performance, and power dissipation penalties while increasing the efficiency of detecting SEUs and SETs in integrated circuits.

Why connect the BICS to the bulk instead of to the power lines? When a charged particle strikes a sensitive site in a CMOS circuit, it generates a current that flows between the transistor's drain and the bulk. The sensitive sites surround the reverse-biased drain junctions of a transistor biased in the off state—for example, the drain junction of the n-channel transistor in Figure 2. The transient current pulse I_p flowing through the pn-junction of the struck transistor arises from the discharge of node capacitance I_C and from the current conducted by the transistor in the on state (I_D of the p-channel transistor in Figure 2). The current's direction depends on whether the particle is discharging or charging the logic node.[2] The

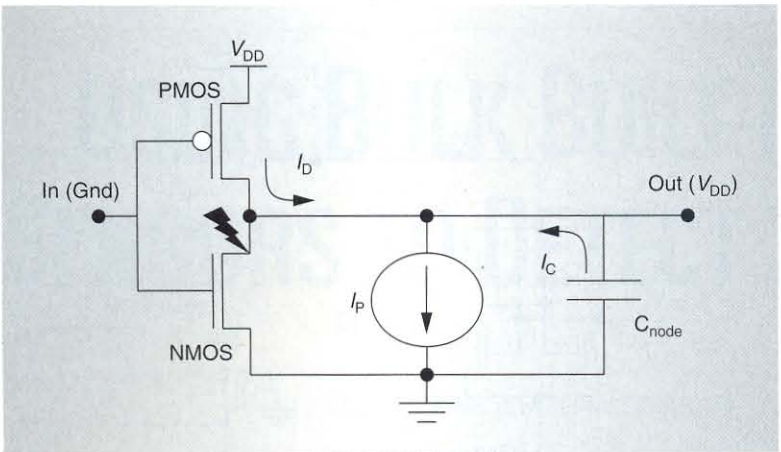

Figure 2. Circuit-level representation of the charge deposition mechanism. The particle hit is modeled by transient current pulse I_P flowing between the reverse-biased drain-bulk pn-junction of the n-transistor in the off state. Part of the transient current flow comes from node capacitance (I_C); the other part comes from V_{DD} through the p-transistor in the on state (I_D). This illustration depicts the case of a particle hit at the drain junction of the n-transistor in the off state.

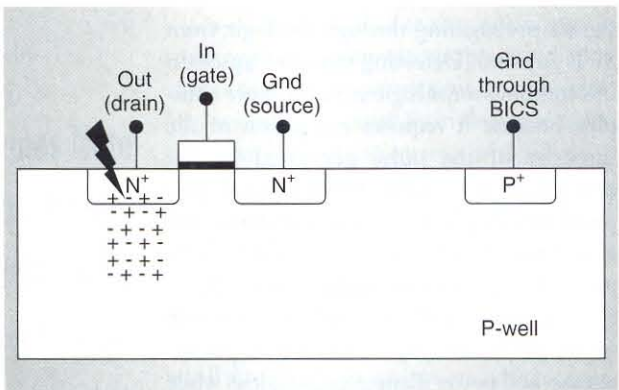

Figure 3. The body ties connect to the V_{DD} or to the ground through the bulk-BICS.

peak current induced by an energetic particle strike is more intense at the drain-bulk junction than at the connection to the power lines.

During normal circuit operation, the current flowing between a reverse-biased drain junction and the bulk is negligible compared with the current peak induced by an energetic particle hit. Consequently, a BICS connected to a circuit's bulk instead of to its power lines is more efficient. The bulk-BICS works just like the one shown in Figure 1, except that now the BICS analyzes the current appearing at the bulk terminal. During normal operation, the current in the bulk is approximately zero. Only the leakage current flows through the biased junction, and it is still very low compared with the current generated by charged particles. So when a charged particle generates a current in the bulk, the bulk-BICS recognizes that a SET has occurred. Figure 3 shows the connection of the bulk-BICS to the body ties. The circuit itself connects to the power lines at the transistor sources, like every standard CMOS circuit, but the body ties connect to the V_{DD} (n-well case) or to the ground (p-well case) through the bulk-BICS.

Figures 4a and 4b show the bulk-BICS connected to a sequential and a combinational circuit, respectively. The bulk-BICS approach requires a dedicated BICS in each type of well (n-well and p-well). Consequently, designers can use one BICS design for PMOS transistors in the n-well and another BICS design for NMOS transistors in the p-well. Each BICS uses less area than the standard BICS that detects SEUs in memory cells (Figure 1). In addition, the possibility of distinguishing upsets that occur in the PMOS region (out-P) from those occurring in the NMOS region (out-N) can help to precisely map the faulty region in the circuit design. In Figures 4a and 4b, the P-BICS detects 0-to-1 transitions and N-BICS detects 1-to-0 transitions.

Designers can calibrate the bulk-BICS to detect only transient current pulses that can cause a logic transition at the struck node. We assume a SET occurs if the voltage of the logic gate output node changes by more than $V_{DD}/2$. This bulk-BICS technique represents a conservative approach to SET detection; it detects all SETs that might cause a soft error. However, a SET can be masked logically, electrically, or by a latching window. For these cases, in which SETs are masked out before they reach a memory element, it is necessary to combine bulk-BICS with other techniques. Alternatively, we can assume that every time a SET occurs, even if it is a false positive, the system must be restarted or an error correction procedure invoked.

The number of BICS needed for SET and SEU detection in a given circuit is related to the amount of area to be protected. Circuit sensitivity (load capacitance and junction capacitance) and body-tie density (bulk resistance) determine the maximum detection capacity. We present area overhead as the ratio of the active area occupied by BICS transistors

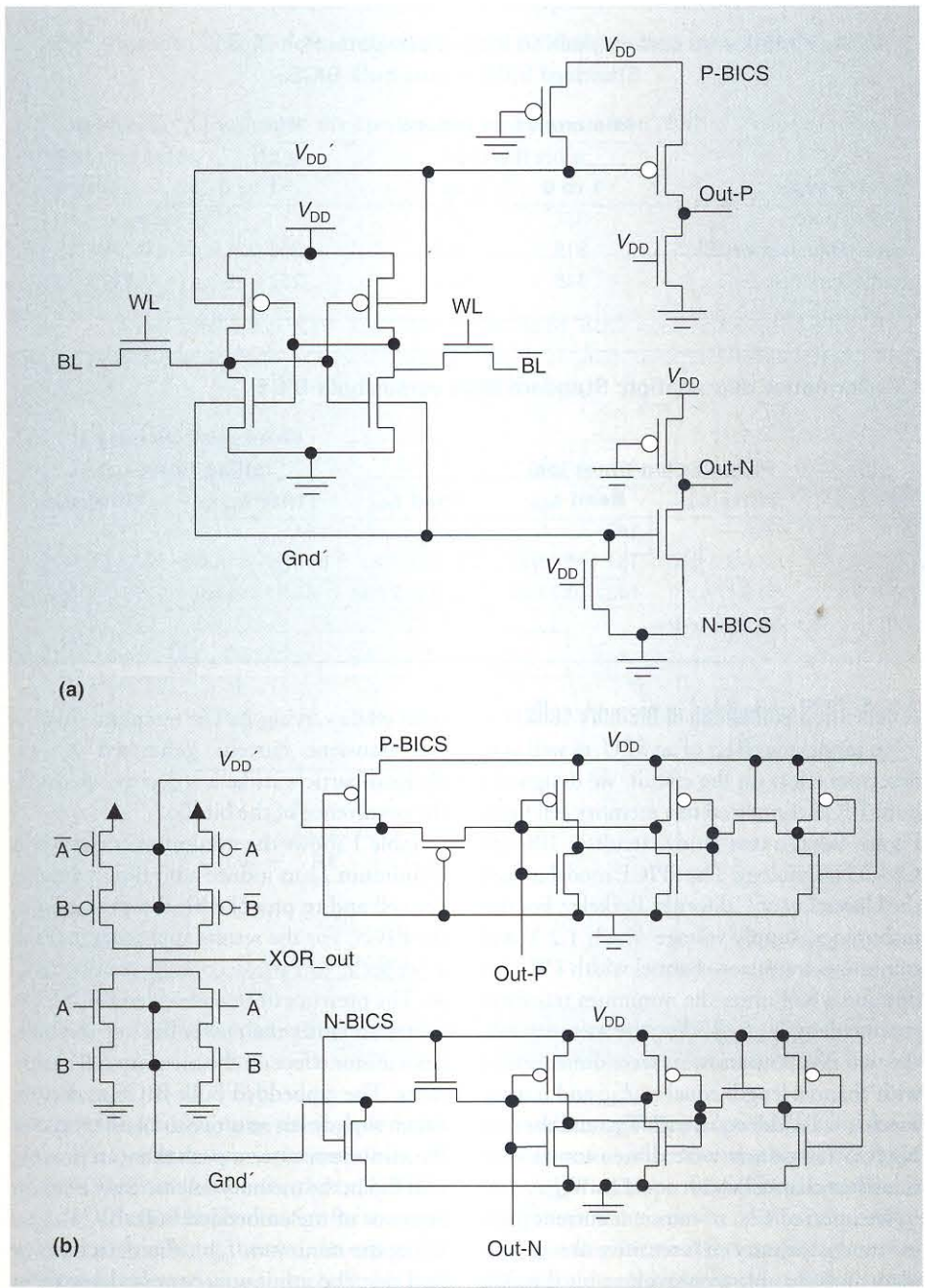

Figure 4. In the bulk-BICS approach, the proposed N-BICS and P-BICS connect to the bulk of sequential and combinational logic circuits: BICS connected to the bulk of a memory cell (a) and BICS connected to the bulk of an exclusive-OR logic gate (b).

to the active area occupied by the transistors of the circuit that the BICS protects. The distance from the body tie to the transistor drain location affects the current's resistance and therefore the magnitude of the current pulse. Hence, the bulk-BICS has a maximum bulk resistance that it can tolerate. Bulk resistance varies widely among different technologies; therefore, the minimum body-tie contact density also varies by technology. For this reason, in the simulations we describe, we consider the impact of the bulk resistance on SET detection, and we evaluate the maximum bulk resistance the bulk-BICS can tolerate.

Table 1. Minimum current peak to induce and detect bit flips in memory cells: Standard BICS versus bulk-BICS.

	Minimum I_0 to induce a bit flip (μA)		Minimum I_0 to provoke a bit-flip detection (μA)	
Device type	**1 to 0**	**0 to 1**	**1 to 0**	**0 to 1**
Memory cell	335	361		
Embedded standard BICS	319	347	252 (–21%)	278 (–28%)
Embedded bulk-BICS	345	365	257 (–25%)	217 (–40%)

Table 2. Performance degradation: Standard BICS versus bulk-BICS.

	Propagation times (ps)				Write cycle rising and falling times (ps)	
Device type	**Write t_{PLH}**	**Write t_{PHL}**	**Read t_{PLH}**	**Read t_{PHL}**	**Write t_{rising}**	**Write $t_{falling}$**
Memory cell	82.2	69.6	143	143	44.5	39.6
Embedded standard BICS	85.6 (4.1%)	63 (–9.5%)	151.1 (5.7%)	151.1 (5.7%)	851.3 (1,813.7%)	32.4 (18.2%)
Embedded bulk BICS	81.9 (–0.3%)	69.6 (0%)	143.4 (0.27%)	143.3 (0.27%)	44.3 (–0.44%)	39.8 (0.5%)

PLH: propagation, low-to-high; PHL: propagation, high-to-low

A bulk-BICS embedded in memory cells

To model the effect of an SEU, as well as to detect its effect on the circuit, we designed a bulk-BICS connected to a memory cell (as in Figure 4a) as a case-study circuit in 100-nm CMOS technology. The SPICE model is from the University of California, Berkeley. For this technology, supply voltage V_{DD} is 1.2 V and minimum transistor channel width (W_{min}) is one and a half times the minimum transistor channel length (L_{min}).[7] For the memory cell, the two PMOS transistors were dimensioned with channel length equal to L_{min} and transistor channel width equal to $2W_{min}$; and the four NMOS transistors were dimensioned with transistor channel width equal to W_{min}.

We injected a set of transient current pulses into the memory cell's sensitive sites to simulate an SEU able to provoke a bit flip. We modeled this transient current pulse by introducing a double exponential current source at the struck node:[8]

$$I_P(t) = I_0 \left[\exp(-t/\tau_F) - \exp(-t/\tau_R)\right] \quad (1)$$

where I_P is the transient current pulse, I_0 is the current peak, τ_F is the decay time of the current pulse, and τ_R is the time constant for initially establishing the ion track. During the simulations, we kept the time parameters of the double exponential current source constant while varying I_0. The temporal shape of the transient current generated by the charged-particle strike is a decisive factor for the occurrence of the bit flip.[8,9]

Table 1 shows the minimum current peak (minimum I_0) to induce a bit flip in a memory cell and to provoke bit-flip detection by the BICS. For the results appearing in Table 1, we set τ_R to 1 picosecond (ps) and τ_F to 15 ps. The presence of an embedded BICS, connected to either the power lines or the bulk, has a minor effect on the memory cell's sensitivity. The embedded bulk-BICS makes the circuit slightly less sensitive to an SEU because the minimum current peak that can provoke a bit flip in the memory cell increases with the presence of the embedded bulk-BICS. Analyzing the minimum I_0 bit-flip detection, we find that the minimum current detected by the BICS is about 20 percent less than the actual minimum current that can provoke an SEU. This is a conservative approach, and the BICS works within a safe margin of detection. Results show that the embedded bulk-BICS has higher detection sensitivity than the standard BICS connected to the power lines.

Table 2 compares standard BICS and bulk-BICS in terms of performance degradation. We analyzed propagation times from high to low and low to high transitions (t_{PHL} and t_{PLH}, respectively) in the write and read cycle, and

Table 3. Power dissipation by BICS: Standard versus bulk connection method.

BICS method	Power dissipation for write operation (fW)	Power dissipation for read operation (fW)
Embedded standard	0.54	0.73
Embedded bulk	0.0046	0.0024

fW: femtowatt

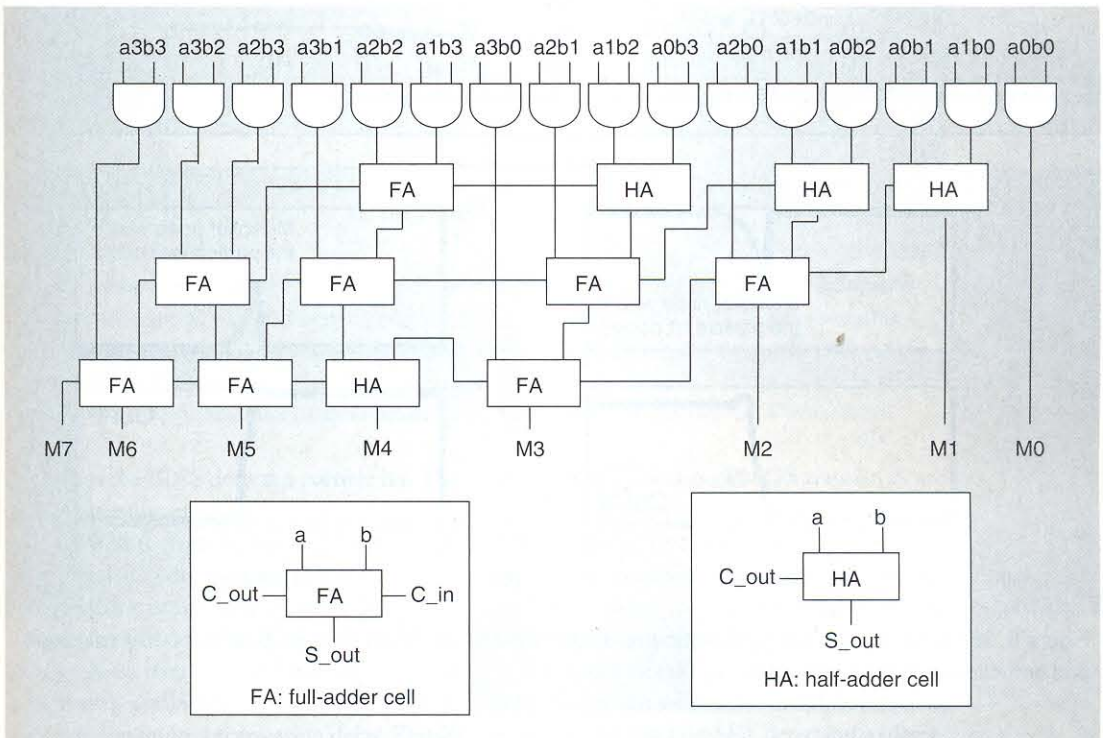

Figure 5. Bulk-BICS for detecting single-event transients in a combinational circuit 4-bit multiplier.

the rising and falling time during the write cycle. The performance variations observed in the SPICE simulation for the bulk-BICS are within the simulation's range for numerical accuracy, meaning that we can expect no performance degradation if the bulk-BICS is embedded in a design. Using a standard BICS, however, results in performance penalties.

Table 3 compares BICS and bulk-BICS in terms of power dissipation. The results show that power dissipation for the standard BICS is two orders of magnitude higher than for the bulk-BICS.

A pair of bulk-BICS (N-BICS and P-BICS) can monitor SEU and multiple-bit upsets (MBUs) in a set of SRAM cells. Simulation showed that one N-BICS and one P-BICS can detect SEUs in 128 memory cells. This means we could connect one pair of bulk-BICS to each memory row to determine whether bit flips have occurred in a 128-bit stored data item. This is an efficient way to detect MBUs in memory cells, avoiding the need for complex error correction code such as Hamming code with double-bit correction capability or higher detection codes, such as Reed-Solomon code.

The ratio of active area occupied by the 6 BICS transistors to active area occupied by the memory cells' 768 transistors is roughly 0.18, meaning that the bulk-BICS occupies 15 percent of the total active area, which is acceptable for fault-tolerant circuits.

Bulk-BICS embedded in combinational logic

The 4-bit multiplier in Figure 5 exemplifies the ability of the bulk-BICS to detect SETs in

Table 4. Evaluation of bulk-BICS SET detection in a 4-bit multiplier.

	0-to-1 transition						1-to-0 transition					
	τ_F (ps)						τ_F (ps)					
I_0 (μA)	10	20	30	40	50	60	10	20	30	40	50	60
150	NN	NN	ND	ND	ND	TD	NN	ND	ND	ND	TD	TD
250	NN	ND	TD	TD	TD	TD	NN	ND	TD	TD	TD	TD
350	NN	TD	TD	TD	TD	TD	NN	TD	TD	TD	TD	TD
450	NN	TD	TD	TD	TD	TD	ND	TD	TD	TD	TD	TD
550	ND	TD	TD	TD	TD	TD	ND	TD	TD	TD	TD	TD
650	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD

NN: no transition and no detection; ND: no transition but detection; TD: transition and detection

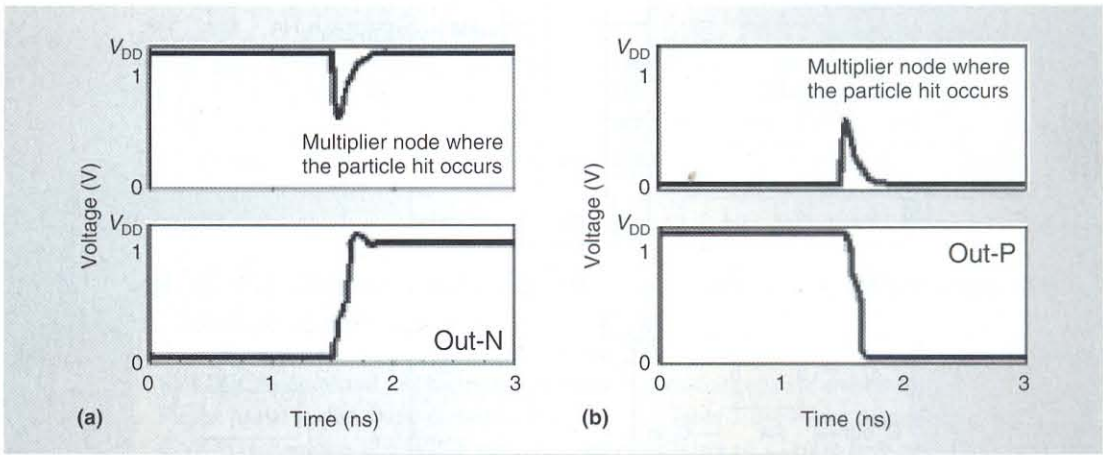

Figure 6. SET detection simulation results: 1-to-0 transition and detection by N-BICS (a) and 0-to-1 transition and detection by P-BICS (b).

combinational circuits. We placed the BICS to ensure detection of all SETs in all the multiplier's sensitive nodes. A set of transient pulses, modeled as double exponential current pulses and injected by simulation into the multiplier's sensitive nodes, simulated SETs that could propagate to the outputs. By SPICE simulation, we generated the set of current pulses using Equation 1, with $\tau_R = 5$ ps in all simulations and parameters I_0 and τ_F varying. Our goal was to model the effect of different transient current pulses in the multiplier's sensitive nodes for all combinations of inputs and thereby analyze the bulk-BICS detection capability.

Table 4 shows the results for a set of injected transient current pulses of various shapes capable of provoking transitions from 0 to 1 and from 1 to 0 in the output node M3 (Figure 5). The other 4-bit multiplier output nodes showed similar results. ND in Table 4 indicates cases in which the bulk-BICS could detect a transient pulse, but the pulse could not provoke an error at the output. This happens only when the combined I_0 and τ_F parameters produce very low current pulse amplitudes (around 150 to 250 μA) combined in some cases with a very fast decline in the exponential curve. This type of transient pulse has a high likelihood of being electrically masked at a subsequent gate.

The SPICE simulations show that the bulk-BICS is very efficient for SET detection, once the bulk-BICS has detected all SETs that could provoke transitions at the multiplier outputs. Bulk-BICS detects a transition to 1 when a node reaches $V_{DD}/2$ or more. Figures 6a and 6b show example SPICE simulation results—for 1-to-0 and 0-to-1 transitions, respectively—that occurred at 1.5 ns into the simulation time. In both cases, the BICS were able to detect the SET. The logic voltage on the P-BICS output (out-P) is high when there is no particle hit and

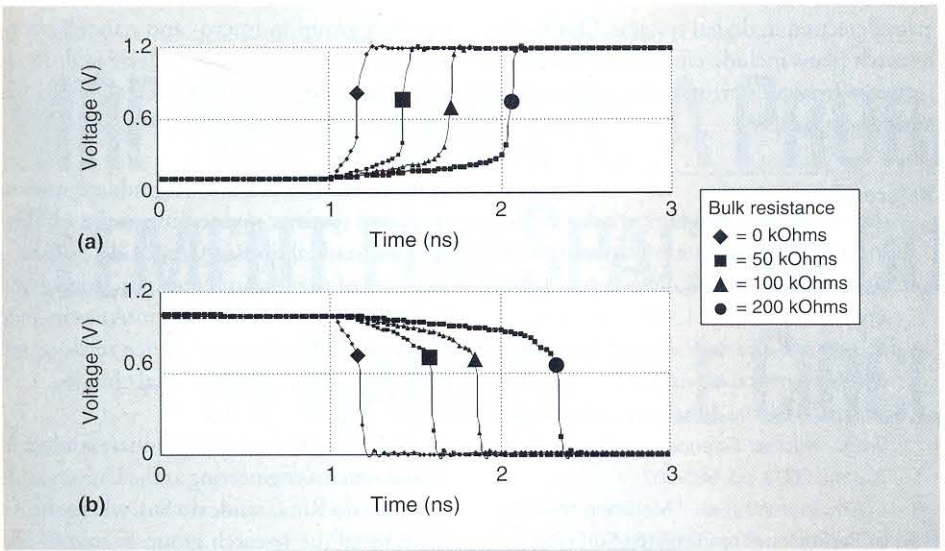

Figure 7. Impact of bulk resistance on SET detection by the bulk-BICS: 1-to-0 transition and detection by N-BICS (a) and 0-to-1 transition and detection by P-BICS (b). In all cases, the particle hit occurs at $t = 1$ ns. Increasing bulk resistance increases the delay between particle hit and SET detection.

low when the BICS detects a particle hit. The logic voltage on the N-BICS output (out-N) is low when there is no particle hit and high when the BICS detects a particle hit.

To measure the effect of the embedded BICS on the multiplier's performance and power consumption, we stimulated the multiplier's inputs exhaustively and evaluated the minimum, average, and maximum propagation delay. Results show that the embedded bulk-BICS does not cause performance degradation. In this case study, the power dissipated by the set of BICS is of the same order as the dynamic power of the multiplier, which increases the overall power dissipation in the protected circuit. Although the dynamic power of the circuit to be protected depends on the switching frequency, the power dissipated by the BICS is mostly static. This drawback of the BICS is not related, however, to its connection either to the power lines or the bulk. We are working to reduce the BICS static power consumption, thereby decreasing the impact on power dissipation in the protected circuit.

As for area overhead, the 504 transistors in the multiplier require five P-BICS and two N-BICS. The active area occupied by 70 BICS transistors represents roughly 29 percent of the total active area of the entire protected circuit. We use two and a half times more P-BICS than N-BICS because PMOS transistors are approximately two and a half times wider than NMOS transistors. Each BICS connects to roughly the same amount of node capacitance, and we avoided connecting more than one BICS to the same basic logic cell.

We used different values for the bulk resistance in various simulations so that we could evaluate its impact on SET detection to determine the maximum bulk resistance that the bulk-BICS can tolerate. Bulk-BICS detection works properly for bulk resistance values up to 200 kOhms. As Figure 7 shows, high values of bulk resistance introduce a delay between particle hit and SET detection by the bulk-BICS.

Bulk-BICS offers an attractive means of enhancing high-level fault-tolerance methods based on fault detection and correction. Its costs are low in terms of both area and performance degradation, and it responds quickly to soft error detection. It can be applied, for instance, in microprocessors with recomputing and pipeline refreshing capabilities. In this case, once a soft error is detected, the processor can reexecute the corrupted instruction. Our bulk-BICS method is easy to integrate into a standard integrated circuit design flow; no major changes to the original circuit topology are required to embed the bulk-BICS for soft

error detection in digital systems. Our further research plans include efficient techniques to recovery from soft errors, both at the circuit and system levels. MICRO

References

1. G.R. Srinivasan, "Modeling the Cosmic-Ray-Induced Soft-Error Rate in Integrated Circuits: An Overview," *IBM J. Research and Development*, vol. 40, no. 1, 1996, pp. 77-90.
2. P.E. Dodd and L.W. Massengill, "Basic Mechanism and Modeling of Single-Event Upset in Digital Microelectronics," *IEEE Trans. Nuclear Science*, vol. 50, no. 3, part 3, June 2003, pp. 583-602.
3. P. Shivakumar et al., "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," *Proc. Int'l Conf. Dependable Systems and Networks* (DSN 02), IEEE CS Press, 2002, pp. 389-398.
4. F. Vargas and M. Nicolaidis, "SEU-Tolerant SRAM Design Based on Current Monitoring," *Proc. 24th Int'l Symp. Fault-Tolerant Computing* (FTCS 94), IEEE CS Press, 1994, pp. 106-115.
5. B. Gill et al., "An Efficient BICS Design for SEUs Detection and Correction in Semiconductor Memories," *Proc. Design, Automation and Test in Europe* (DATE 05), IEEE CS Press, 2005, pp. 592-597.
6. L. Anghel, D. Alexandrescu, and M. Nicolaidis, "Evaluation of a Soft Error Tolerance Technique Based on Time and/or Space Redundancy," *Proc. Symp. Integrated Circuits and System Design* (SBCCI 13), IEEE CS Press, 2000, pp. 237-242.
7. Device Group at UC Berkeley, "Berkeley Predictive Technology Model," 2004; http://www-device.eecs.berkeley.edu/~ptm.
8. G. Wirth, M. Vieira, and F. Lima Kastensmidt, "Computer Efficient Modeling of SRAM Cell Sensitivity to SEU," *Proc. IEEE Latin American Test Workshop*, IEEE CS Press, 2005, pp. 51-56.
9. G. Wirth et al., "Single Event Transients in Combinatorial Circuits," *Proc. 18th Int'l Symp. Integrated Circuits and Systems Design*, ACM Press, 2005, pp. 121-126.

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