Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design

Using Capacitive Cross-Coupling Technique in RF Low Noise Amplifiers and Down-Conversion Mixer Design

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Abstract

We report an approach to improve the noise performance of RF low noise amplifiers (LNAs) and down-conversion mixers. The technique we described here is based on capacitive cross-coupling across the two sides of a differential input stage. A LNA and mixer have been implemented in 0.5m CMOS process to demonstrate the viability of this technique. The measurements show that the LNA achieves 3.0dB noise figure and 12.2 dB voltage gain (optimized for the maximum power transfer), and the mixer has 5.2dB DSB noise figure and 13.2 dB voltage conversion gain. Both LNA and mixer operate at 2.7V voltage supply and consume 27mW and 8.1mW power, respectively.

1. Introduction

Growth of the wireless communication market puts increasing demand on low power, low cost and high performance receivers. RF LNAs and mixers are among the most critical building blocks in the receiver chain. The CMOS technology has shown its feasibility for high frequency applications [1-2].

This paper describes how a capacitive cross-coupling (CCC) technique can be used for RF amplifiers and mixers to improve the performance. Section II discusses a capacitive cross-coupling (CCC) technique. Section III presents the LNA implementation using the CCC technique. Details of mixer implementation using CCC are described in Section IV. Experimental results are shown in Section V, followed by conclusions in Section VI.

2. Capacitive cross-coupling technique for noise reduction

Common gate and common source input stages are structures widely seen in the LNA design. The main drawback of common-gate amplifiers is their relatively high noise figure. Ignoring the noise contribution due to the load, a common-gate LNA has a minimum NF [1]:

$$F = 1 + g \qquad (1)$$

Where, γ represents the channel thermal noise coefficient. It is usually difficult for common-gate LNAs to provide a NF well below 3dB. A Common source input stage offers the possibility to achieve the best noise performance by increasing their input quality factor Q. However, it degrades the linearity and increases the sensitivity of the input matching. Common-gate amplifiers can be more easily matched and usually exhibit better linearity than common-source amplifiers.

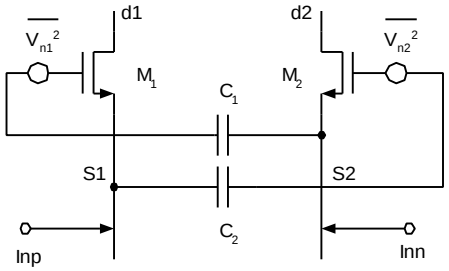

Fig. 1 Capacitive cross-coupling technique

The capacitive cross-coupling (CCC) has been used for gain enhancement and matching [3]. In this section, we will demonstrate how the CCC can be used to improve the NF of a common-gate input stage. Fig.1 shows the schematic of a differential common-gate input stage with CCC. It can be shown that the cross-coupling causes the noise of M_1 and M_2, namely $\overline{v_{n1}^2}$ and $\overline{v_{n2}^2}$, to produce common-mode noise voltages at the output node d1 and d2. Intuitively, This can be explained as follows. Let's assume the following instantaneous polarity for noise source $\overline{v_{n1}^2}$; positive polarity at the gate terminal of input transistor M_1 and negative at the other side (polarity can be exchanged as well). One can easily see that the drain voltage of M_1 will decrease due to the positive disturbance at the gate terminal. On the other hand, because of the negative disturbance at S2, the drain voltage of M_2 will also decrease. Hence, the input noise source $\overline{v_{n1}^2}$ causes a common-mode voltage at d1 and d2. Similar analysis can be applied to the input noise source $\overline{v_{n2}^2}$.

A more rigorous small signal noise analysis was used for a mathematical derivation. Here, only channel

thermal noise source is considered, and other noise mechanisms are neglected for simplicity. The cross-coupling capacitors C_1 and C_2 are assumed to be much greater than gate-source capacitance C_{gs}. The derived noise factor expression of the input pair M_1 and M_2 is given by :

$$F = 1 + \frac{g}{2} \tag{2}$$

It can be seen that due to the capacitive cross-coupling the noise contribution from the input transistors is reduced though not completely eliminated.

Worthy to mention is that the derivation of the noise factor assumes that the input impedance is matched to the source impedance for maximum power transfer. Matching for the optimal noise performance can reduce the NF value. This can be demonstrated by changing the effective input impedance ($1/2\times g_m$). Fig. 2 illustrates the change of the NF vs. the effective transconductance ($2\times g_m$). The noise performance will be improved as the transconductance is increased. Another advantage of the common gate input stage with CCC is that the input effective transconductance is doubled due to the capacitive cross-coupling. Thus, the current consumption can be reduced. Finally, it is also interesting to note that the capacitive cross-coupling does not add much cost and complexity.

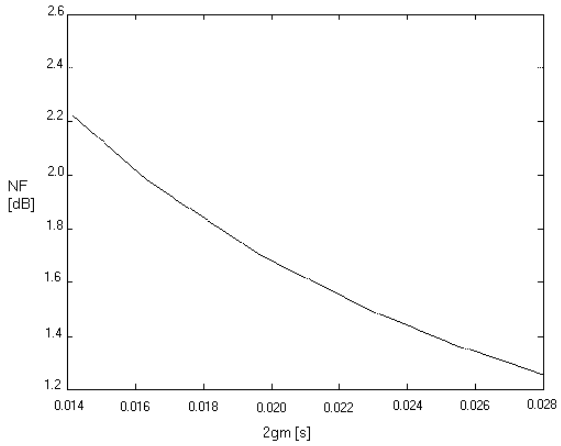

Fig. 2 NF of the input pair with CCC vs. $2g_m$

3. LNA Implementation using the CCC Technique

The full schematic of a LNA employing the CCC technique is depicted in Fig.3. The input impedance matching is achieved by sizing and adjusting the bias current of the input transistors M_1 and M_2 such that $1/(2\times g_m)=50\Omega$. The cross-coupling capacitors C_1 and C_2 are 10pF poly-to-poly capacitors in our implementation. Off-chip inductors L_1 and L_2 are used to resonate with the gate-source capacitor C_{gs} and the input parasitic capacitance at the frequency of interest. Cascode transistors M_3 and M_4 are added to improve the reverse isolation of the LNA. Transistors M_5, M_6, M_7, and M_8 are used to realize large resistors to isolate the signal path from the biasing circuitry. The LNA's load is a 300Ω resistance (assuming an on-chip mixer).

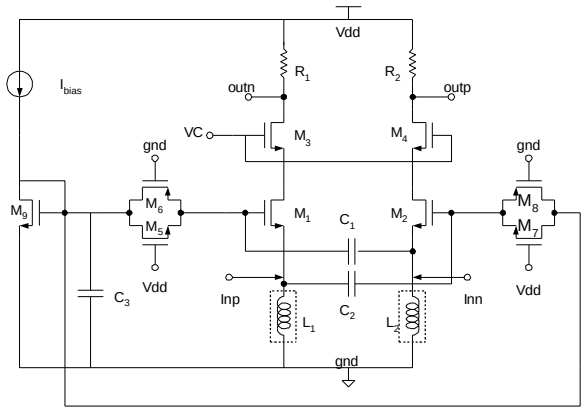

Fig. 3 Schematic of the LNA with CCC

As pointed out in the previous section, the LNA with CCC provides noise advantage over the conventional differential common-gate LNA. However, the dynamic range of a circuit is not only determined by the noise but also by the linearity. Assuming that the transconductance g_m is the only source which causes nonlinearity, the input referred IP3s of the conventional differential common-gate LNA and the LNA with CCC are derived using *volterra* series. The derived expressions are given in (3) and (4), respectively.

$$IP3 = 8\sqrt{\frac{2\cdot G_s}{3\cdot\left|(-K_{3gm} + K_{2gm}{}^2 / G_s)\right|}} \tag{3}$$

$$IP3 = 4\sqrt{\frac{G_s}{3\cdot\left|K_{3gm}\right|}} \tag{4}$$

Equations (3) and (4) are simplified expressions evaluated under input matching conditions. The parameters K_{2gm} and K_{3gm} are the second-order and third-order transconductance nonlinear coefficients. G_s is the source conductance. It is observed that the IP3 of the conventional differential common-gate LNA is not only determined by the third-order nonlinear coefficient but also by the second-order nonlinear coefficient. The IP3 of the LNA with CCC is only influenced by the third-order nonlinear coefficient. For a first-order analysis, we may consider the MOSFET transistor to be a square-law device. This means that the third-order nonlinear coefficient is usually much smaller than the second-order one. Thus, the IP3 of the LNA with CCC is higher than that of the conventional differential common-gate LNA. Although the second-order intercept point (IP2) is not important in a heterodyne receiver, it is a limiting factor in a direct conversion receiver. The IP2 of a differential circuit is usually limited by mismatch between differential path. Assuming that only transconductance

(g_m) has mismatch (Δg_m) and applying the same procedure for the IP3 modeling, the input-referred IP2s of both LNAs are given by (5) and (6), respectively.

$$IP\ 2 \approx \frac{16 \cdot G_s^{\ 2}}{3\left|K_{\ 2\,gm} \cdot \Delta g_{\ m}\right|} \tag{5}$$

$$IP2 \approx \infty \tag{6}$$

Due to mismatch, the conventional differential common-gate LNA shows a finite IP2, while the mismatch effect is minimal on the IP2 of the LNA with CCC.

4. Mixer Implementation using the CCC Technique

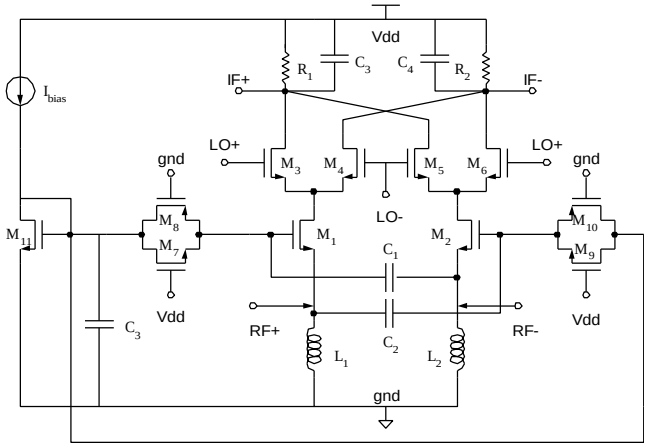

Fig. 4 Schematic of the mixer with CCC

In the Gilbert cell mixer, the linearity is usually determined by RF transconductance. Thus, most of the design effort is spent attempting to find better ways of providing V-I conversion. One simple, but powerful technique consists of using degeneration resistors in the source of V-I converter. But, additional resistors will penalize the mixer noise performance, which may, in turn, increase design difficulties for the circuitry preceding it.

The capacitive cross-coupling technique depicted in previous sections can be used in RF V-I converter to minimize the noise contribution and improve the linearity simultaneously. The proposed double-balanced Gilbert cell mixer with CCC is shown in Fig. 4. Transistors M_1 and M_2, cross-coupled by capacitors C_1 and C_2, form a differential transconductance stage. The drain current of the M_1 and M_2 is steered through M_3 and M_4 or M_5 and M_6 to perform the mixing function. Output capacitors C_3 and C_4 combined with output resistance R_1 and R_2 to form a low pass filter. The purpose of this filter is to attenuate high frequency components at the IF output. Biasing of the mixer is similar to that of the LNA.

5. Experiment Results

Both LNA and mixer have been implemented in an AMI 0.5µ CMOS process. Measurements of the LNA show a 12.2dB voltage gain and a NF of 3.0dB at 900MHz. The 3.0dB NF, which seems higher than recently reported values, can best be explained by the fact that the LNA was designed for maximum power transfer and not optimized for the noise figure. One can achieve better noise performance by increasing the transconductance as illustrated in Fig. 2. The gain and NF of the LNA are plotted in Fig. 5 with frequency swept from 800M to 950M. The input-referred IP3 is extracted by applying two tones test. The power of both tones was swept while the resulting third-order intermodulation product was measured. Fig. 6 shows the fundamental tone and the third-order intermodulation product at 899.5MHz and 900MHz. Since output impedance of LNA is not 50Ω, "VdBm" is defined as voltage corresponding to a power level of 0dBm in a 50Ω system. Because source resistance is 50Ω, the input "VdBm" is same as original "dBm".

The measured mixer DSB noise and conversion gain are 5.2dB and 13.2dB, respectively. The measured NF is lower than most published mixer. The results of a two-tone measurement on the mixer are shown in Fig. 7. For the mixer measurement, the LO drive amplitude is equivalent to 300mV. Both LNA and mixer prototype are measured in TQFP package with ESD protection. The measured LNA and mixer results are summarized in Table.1 and Table.2 respectively. Microphotographs of both circuits are shown in Fig. 8.

6. Conclusion

In this paper, we have shown how the capacitive cross-coupling technique can be used to improve the noise performance of a common-gate input stage. A LNA and mixer with CCC have been implemented in 0.5µ CMOS process to verify our theoretical findings. The LNA achieves around 3.0dB NF up to 900MHz, In addition, the LNA has significant +6.7dBm input-referred IP3 and only consume 20mW. The mixer has very low DSB NF at 5.2dB and +13.8dBm output IP3. Yet, both circuits do not rely on using on-chip spiral inductors.

Reference

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[2] A. R. Shahani, D. K. Shaffer, and T. H. Lee, "A 12-mW Wide Dynamic Range CMOS Front-End for Portable GPS Receiver ", *IEEE J. Solid-State Circuits*, Dec 1997, vol. 32, pp. 2061-2069.

[3] T. Cho et al, "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones", *ISSCC Digest of Technical Papers*, Feb 1999**,** pp. 228-229.

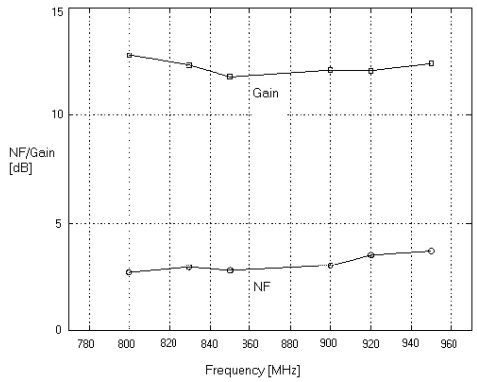

Fig. 5 Measured LNA gain and NF vs. frequency

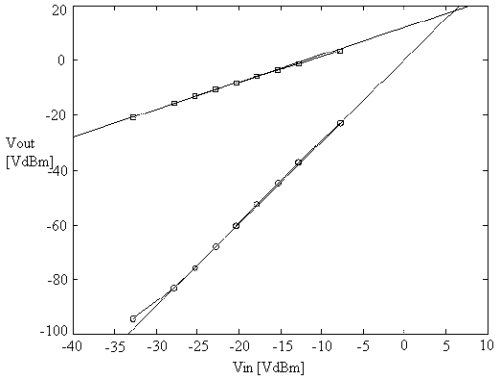

Fig. 6 Measured LNA IP3

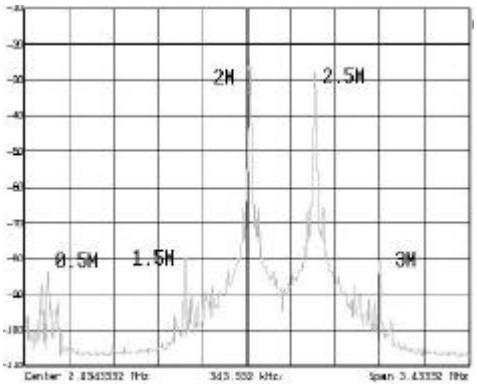

Fig. 7 Measured mixer two tone test

Table 1 Summary of LNA measurements

Frequency	900MHz
NF	3.0dB
Gain (voltage)	12.2dB
IP3 (input)	+6.7dBm
IP2 (input)	+34dBm
1dB (input)	-7dBm
Power Supply	2.7V
Power Consumption	20mw
Silicon area	$0.5\times0.4mm^2$

Table 2 Summary of mixer measurements

RF Frequency	900MHz
LO Frequency	910MHz
LO Amplitude	300mV
NF (DSB)	5.2dB
Gain (voltage)	13.2dB
IP3 (output)	+13.8dBm
IP2 (input)	+25.6dBm
Power Supply	2.7V
Power Consumption	8.1mw
Silicon area	$0.7\times0.5mm^2$

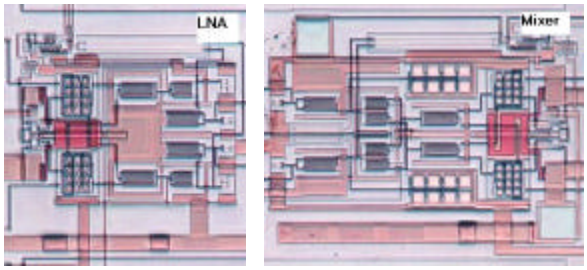

Fig. 8 Microphotograph of the LNA and mixer