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Using SPICE for the modelization of the static behaviour of the insulated gate transistor

F. Gaffiot, J. P. Chante and M. Le Helley

Laboratoire d'Electronique, Automatique et Mesures Electriques de l'Ecole Centrale de Lyon (*), 36, avenue de Collongue, B.P. 163, 69131 Ecully Cedex, France

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Résumé. — Une nouvelle application d'un programme de simulation de circuits (SPICE) est présentée ci-dessous. Le comportement statique d'un composant bipolaire complexe (IGT) est analysé à partir d'un circuit équivalent faisant apparaître les paramètres physiques du dispositif réel. Cette analyse permet de modifier les paramètres technologiques afin d'améliorer le fonctionnement du transistor à grille isolée (IGT).

Abstract. — A new application of a circuit simulation program (SPICE) is presented. The static behaviour of a complex bipolar device (COMFET or IGT) is analysed from an equivalent circuit including the physical components of the real device. It is possible to infer about technological parameters to improve the working of the IGT.

1. Introduction.

The SPICE program is well known for circuit design but its use for the analysis of complex devices is unusual. The purpose of this Letter is to present a new application of the SPICE program : drawing an equivalent circuit of a complex device, it allows one to simulate its behaviour, to point out the influence of the electrical parameters of the model, and thus, to infer the technological parameters of the real device.

Our work deals with the IGT (Insulated Gate Transistor) also known as COMFET (Conductivity Modulation FET), this device has been previously presented [1, 2, 5, 7] it is very similar to a power DMOS, the only difference is a P^+ substrate instead of a N^+ one. This P^+ layer induces a bipolar PNP structure and the resistivity of the lightly doped layer is so modulated by the injection of holes coming from the anode.

Due to this resistivity modulation and to the current gain of the PNP transistor experiments show a great improvement of the ON resistance as compared to a DMOS device having the same features [2-4] ; the other important characteristics of the IGT or COMFET, as switching parameters, voltage capabilities..., allow number of new applications [4, 5].

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2. Equivalent circuit.

Figures 1a and 1b show respectively the elementary structure of the studied device and the equivalent circuit used for the simulation with SPICE.

It should be pointed out that equivalent circuits have already been given [4, 6], but none of them included all the physical components as shown in figure 1b.

The MOSFET, the JFET and the R_x resistance simulate the internal vertical DMOS part of the device. R_x stands for the resistance of the lightly doped N^- layer and it is also the access base resistance of the PNP bipolar transistor. It should be pointed out that the JFET effect, due to the extension of the space charge layer at the PN^- junction, is very important in high voltage structures with low doping level in the N^- base and in strongly densified devices. If the spacing between the P regions increases or if the N^- layer is sufficiently doped the JFET may be suppressed.

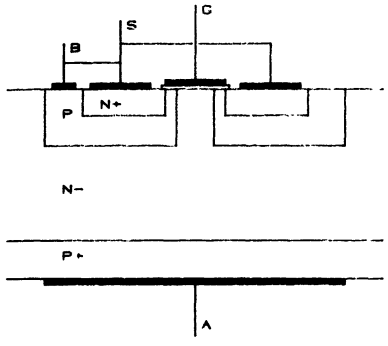

Fig. 1a. — Elementary structure used for experiments (ν-layer : lightly doped N-layer).

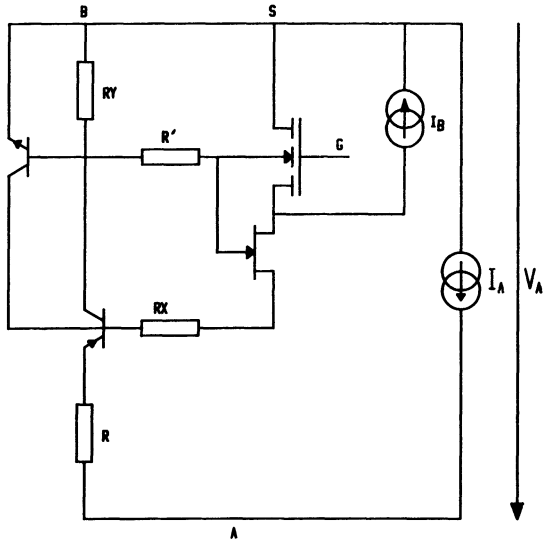

Fig. 1b. — Equivalent circuit of the device (A : anode ; G : gate ; S : source ; B : base).

The bipolar NPN and PNP transistors stand for the thyristor structure. R′ is a little resistance which simulates the P layer between the active base region of the NPN transistor and the channel region of the MOSFET and R_y is the pinched resistance of the P layer beneath the N^+ source layer. This last resistance which is crossed by a hole current has two important effects.

(i) Induction of a positive voltage under the MOSFET channel, resulting in a biasing of the MOSFET substrate and in an increase of its drain current. The parameters required by SPICE 2 to simulate the substrate effect are not very well known so we assign them to be zero and we take this effect into account by means of the current source I_B. This source, being controlled by the substrate voltage, stands for the increase of the drain current. The shift of the threshold voltage due to the substrate bias is

$$\Delta V_T = \frac{\sqrt{2\,\varepsilon_s\,qN_a}}{C_i}\left[\sqrt{2\,\psi_B + V_{BS}} - \sqrt{2\,\psi_B}\right] \quad [8],$$

then the shift of the drain current may be written

$$I_B = \Delta I_D = \left(\frac{Z}{L}\right)\mu_n\,C_i\,\Delta V_T \cdot V_{DS} = \left(\frac{Z}{L}\right)\mu_n\sqrt{2\,\varepsilon_s\,qN_a}\,V_{DS}\left[\sqrt{2\,\psi_B + V_{BS}} - \sqrt{2\,\psi_B}\right],$$

where q is the elementary charge, N_a the substrate doping, Z the channel width, L the channel length, μ_n the electron mobility, ε_s the silicon permittivity, $C_i = \left(\frac{\varepsilon_i}{d}\right)$ the insulator capacitance, V_{DS} the drain to source bias, V_{BS} the substrate to source bias and ψ_B the potential difference between the Fermi level and the intrinsic Fermi level.

In the program, I_B is written as a polynom obtained by a mean square method.

It is clear that this effect occurs for all the gate bias levels and the model can be used to represent normal and subthreshold behaviours.

(ii) Forward biasing of the emitter-base junction of the NPN bipolar-transistor, which leads to a thyristor behaviour [2, 4] (in this case, the gate can no longer turn off the anode current).

Among the electrical parameters required by the SPICE program some of them are obtained by experiments (bipolar transistor current gain, threshold voltage of the MOSFET, carrier lifetime in the N^- layer). Other ones are calculated from the technological parameters of the device like doping profiles, oxide thickness, geometrical dimensions (I_B current source, MOSFET transconductance, JFET parameters). The last ones are used for the fit of the computed and experimental curves (resistances, junction leakage current).

3. Results.

Experimental and theoretical curves are shown in figures 2a and 2b respectively. These characteristics have been drawn with an elementary device : therefore, the values of the anode current are low.

The first negative resistance region (region A, Fig. 2a) is due to the increase of the MOSFET conductance as a result of the internal biasing of the P layer.

The second negative resistance region (region B, Fig. 2a) corresponds to the transition from a bipolar MOSFET Darlington working mode to a thyristor behaviour (the internal biasing of the P layer results also in a biasing of the N^+ P junction in the forward direction). It should be noted that the first negative resistance appears only at relatively low gate bias.

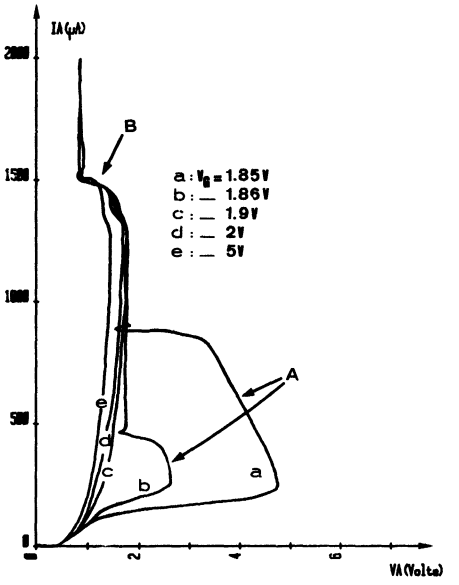

Fig. 2a. — Experimental characteristics : V_A is the anode voltage, V_G, the gate voltage, I_A, the anode current.

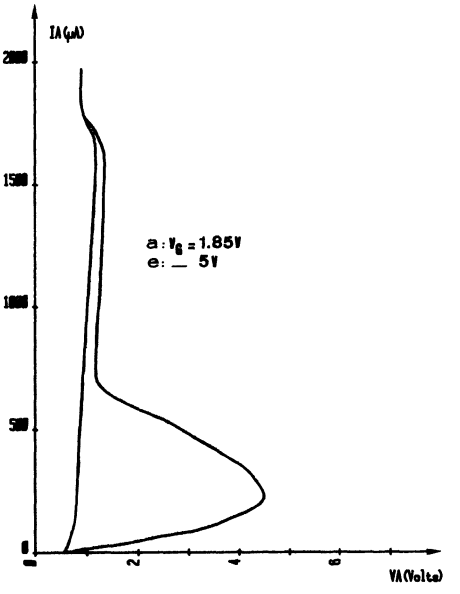

Fig. 2b. — Computed curves, for two values of the gate bias voltage.

4. Conclusion.

This use of SPICE program permits us to analyse the behaviour of a complex structure like the IGT ; the equivalent circuit — suitable for computer aided circuit design — of this peculiar device

gives a good simulation of its $I(V)$ characteristics and allows one to distinguish the different working modes of the device, which we summarize below :

— power MOSFET at low gate bias voltage,
— IGT at higher gate bias voltage and at relatively low anode current level,
— gate controlled thyristor at high gate bias voltage and at high anode current level.

Finally, the SPICE program makes it possible to determine the contribution of each physical component involved in the three working modes and then to choose the parameters which promote any of them.

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