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Utilization of Buried Capacitance™: A Case Study

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Abstract

Embedding capacitive layers inside the Printed Circuit Board (PCB) have demonstrated the ability to reduce the number of Surface Mount Technology (SMT) chip decoupling capacitors on the PCB surface as well as greatly improve the performance of the power distribution system. Many systems today utilize this technology, but most public information is limited to data on test vehicles or emulators. This paper utilizes simulated as well as measured product data to compare the performance of the standard design to one using various types of Buried Capacitance™ layers with a reduced number of SMT decoupling capacitors. A methodology is provided that can be utilized for other designs.

Author(s) Biography

Jun Fan- Dr. Jun Fan received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. He is currently an Assistant Professor at the University of Missouri-Rolla. From 2000 to 2007, he was with NCR Corporation, San Diego, CA, as a Consultant Engineer. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, PCB noise reduction, differential signaling, and cable/connector designs. Dr. Fan received the Conference Best Paper Award from the Applied Computational Electromagnetics Society in 2000. He serves as Chair of the TC-9 Computational Electromagnetics Committee of the IEEE EMC Society

Norm Smith- received a B.S. in Electrical Engineering from Auburn University in 1985 and a M.S. in Computer Engineering from National Technological University in 2000. He is currently employed at NCR Corporation, San Diego, CA (1990 to present) as a Senior Design Engineer. He primarily has been involved in high-speed board level design, including signal analysis of ASIC packaging, cable development, and printed circuit board interconnect. He holds four patents in work related to printed circuit design and layout.

Jim Knighten- received his B.S. and M.S. degrees in electrical engineering from Louisiana State University in 1965 and 1968, respectively, and his Ph.D. degree in electrical engineering from Iowa State University in1976. He is employed by Teradata in San Diego, CA working on EMI and signal integrity design and testing of high-speed digital signal trans-mission systems in massively parallel processing computing systems that are used for data warehousing applications. Prior to joining NCR, he worked for Maxwell Technologies, Inc. and, earlier, IRT Corporation in San Diego, CA, where he was engaged in the study and mitigation design of the effects of the electromagnetic pulse created by nuclear weapon detonation, EMI, lightning, and high-powered microwaves on electronic systems. He has authored numerous technical papers on topics involving various aspects of electromagnetics and taught short courses on electromagnetic pulse effects and electronics survivability both in the USA and in Europe. He is a member of the IEEEEMC Society.

John Andresakis- Vice President of Strategic Technology for Oak-Mitsui Technologies has over 26 years experience in the manufacturing of Printed Circuit Boards. Before Oak-Mitsui, he was Engineering Manager for Hadco Corporation and was in Technical Management at Nelco, Digital Equipment and IBM. He holds a Masters Degree in Chemical Engineering from the University of Connecticut and a Bachelors of Engineering Degree from Cooper Union. He has received 8 patents related to PCB Production and is a member of the IPC Suppliers Technology Council and the various IPC committees developing specifications for Embedded Passives.

Yoshi Fukawa- received his B.S. degrees in Electrical Engineering from Tokyo University of Science, Japan, in 1988. He received a certification of the NARTE EMC Engineer in 2000. He used to be an EMC committee member of the JEIDA in Japan. He currently is a member of the IEEE Santa Clara Valley EMC Chapter. He is a founder of TechDream which is providing EMC total solution selling EMC component, EMI simulation software and PCB material.

Mark Harvey- received his bachelors from Clarkson University in Management and has an MBA. He is a retired Army officer who has worked in the PCB industry for over ten years in both production and engineering. He worked with South Bay Circuits as Processing Manager/Production Manager and later with Hadco in Product Engineering. He now works with Sanmina-SCI as a UL Compliance Manager and with Product Engineering.

Introduction

The development of embedded capacitor technology has been driven by the need to save board area and/or reduce board size, increase functionality, lower costs and improve electrical performance. Many examples exist for the use of this technology (current capacitive material is used in the high-end computing industry, mostly for telecom and networking applications). For these particular high-end printed wire board (PWB) applications, embedded capacitor technology has been utilized to enhance signal integrity, reduce impedance at high frequency and dampen noise. A goal in its use has not necessarily been to remove discrete decoupling capacitors in designs.

Only a few publications regarding the development of materials for embedded capacitors and the advantages of incorporating embedded capacitors in PWBs are acknowledged here [1,2,3]. While some published work demonstrated that the performance of embedded capacitance laminate layers in a PWB stackup are more effective in high-frequency noise suppression than discrete surface mount technology (SMT) capacitors, little detail is provided regarding the number of discrete capacitors that can be safely removed by utilizing this technology. This is the primary topic of this paper.

Two types of Power/Ground simulation tools are utilized to compare the impedance and resonances of the standard design with one using embedded capacitor materials of various dielectric constant (DK) and thickness. We found good correlation of the simulated to measured performance. Furthermore we observed the effect that thin capacitor substrates have on the characteristics of power/ground planar power bus structures. In general, the voltages are more stable with greatly reduced resonances. We show that by using thin core planes and simulation tools one can reduce the number of discrete capacitors and get better electrical performance. The actual number and type (size) of capacitors removed is presented.

In addition to discrete capacitor reduction, the reduction in power/ground plane resonance will be demonstrated. This will minimize the amount of electro-magnetic radiation from the board.

As other applications for incorporating embedded capacitance layers are being examined (such as the modules used in cell phones and laptop PCs,) the ability to predict the number of discrete decoupling capacitor components that can be safely removed is likely to be critical to the decision to use the technology.

In this paper, we will show the approach of using electrical performance simulation of boards with and without embedded capacitors. The number of discrete components the model predicts, to those we can actually remove in actual boards will also be compared. With a good predictive model, the decision to utilize embedded capacitors is simplified.

Formation of Project Team and Design Review

The design team at Teradata, a division of NCR (including the participation of University of Missouri – Rolla) was evaluating a new product and had concerns about the performance of the power distribution system and the number of capacitors required to achieve effective decoupling. It was decided to try embedded capacitor technology on this product. After discussions with the PCB manufacturer (Sanmina-SCI) and the material supplier (Oak-Mitsui), it was determined that a team approach could best evaluate the technology. Each company contributed resources (personnel as was as material/services) to do the evaluation. It was also decided to include a company with simulation software (TechDream) to assist in the simulation expected results.

The standard product is a 12-layer PCB with two 1.5V planes and one 3.3V plane, with the stack-up shown in

Figure 1. To add the embedded capacitance material while maintaining the mechanical symmetry, a new 14-layer stack-up was used with two FaradFlex thin-laminate cores added. As illustrated in

Figure 1, the top FaradFlex core is used for the 3.3V supply, and the bottom one for the 1.5V supply. The thickness of the 1.5V/Ground plane pair in the center of the stack-up remains approximately the same.

Three versions of the new 14-layer PCBs were manufactured, in addition to the standard 12-layer boards, with BC24, BC12, and BC12TM materials as the thin laminate cores, respectively. These boards are denoted as BC24, BC12, and BC12TM in the following descriptions and figures. The standard 12-layer boards are denoted as **FR4** for simplicity.

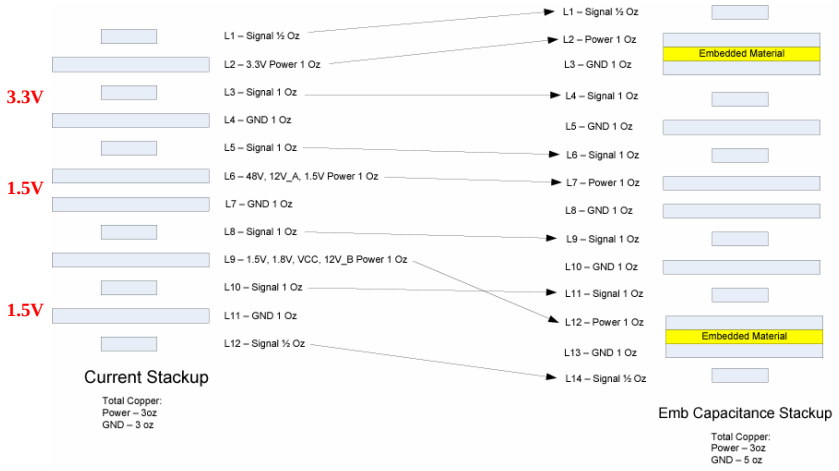

Figure 1: Adding embedded capacitance layers.

BC24 and BC12 are modified epoxy substrates that are 24 and 12 micrometers in thickness respectably. BC12TM is also a 12 micrometer material but has high Dk ceramic particles added to raise the Dk to 10 from the 4.4 of the unfilled products. The materials are formulated to insure durability during PCB processing. The copper foil is a special low profile version to minimize the chance of shorts or leakage. The material is manufactured and distributed under the Buried Capacitance™
license of Sanmina-SCI Corporation.

To evaluate the performance of the FaradFlex® materials, the BC24, BC12, and BC12TM boards were populated only with bulk decoupling capacitors and the FR4 board was fully populated with bulk and high-frequency SMT decoupling capacitors. Compared to the standard FR4 boards, totally **781** SMT capacitors were not populated in the FaradFlex boards.
The decision to remove all the decoupling capacitors was based on the results of the simulations that follow. Also, we used this methodology as it has proven effective in previous designs.

Testing includes swept-frequency S- and Z-parameter measurements for both bare and populated boards, power bus noise measurements in both frequency and time domains,

pre-EMI scan, and environment chamber testing. This project is on-going and not all the planned measurements are completed. This paper reports on current progress.

Product Build

The newly designed 14 layer PCB's were manufactured without any major changes to the current PCB process using ZBC layer processing. Minor wet process allocations were made to process the FaradFlex® thin cores along with a recommended 500 volt HiPot test for the FaradFlex® cores prior to lamination and a final PCB 500 volt HiPot after test. All manufacturers that currently process 0.002" core materials should be able to process these materials with minor process/handling changes.

Product Performance

DC Capacitance of Bare Boards

The dc capacitance of the 1.5V/Ground pair, as well as the 3.3V/Ground pair, was measured for all four types of the bare boards. Two methods were used, and the results were either directly obtained from an LCR meter or indirectly derived from vector network analyzer measurements. As shown in table 1, the results from the two methods agree within less than 10% (those from the network analyzer are in parentheses in the table).

Plane Pair	FR-4 (nF)	BC24 (nF)	BC12 (nF)	BC12TM (nF)
1.5V/GND	76.1 (75.8)	179.5 (179.0)	286.7 (266)	487 (478)
3.3V/GND	21.2 (21.2)	323.8 (321.3)	551 (541)	1148 (1082)

Table 1: DC Capacitance Measurements.

This shows that using the FaradFlex cores significantly increases the dc capacitance values (from between 60-80% for the 1.5V/GND plane pair and from 93-95% for the 3.3V/GND plane pair). The BC12TM cores achieved the largest capacitance values as expected. A large dc capacitance is beneficial for power bus as it can store more charge for logic transitions, as well as decrease power bus impedance at low frequencies.

An interesting observation is that the dc capacitance values are larger for the 3.3V/Ground pair than the 1.5V/Ground pair in the FaradFlex boards. That is because the bottom 1.5V plane shown in is a split plane, and the area of the 1.5V is only approximately one third of the total board area. Therefore, the increase in dc capacitance is less significant due to the reduced plane area.

Swept-Frequency Measurements of Bare Boards

The swept-frequency parameters are good indications of the impedance of the power/ground plane pair. Specifically, Z_{11} is the impedance of the power bus (power/ground plane pair) looking into a port. It determines the noise voltage generated in the power bus due to a current drawn at the same port. However, Z_{11} measurements can be dominated by the port inductance at high frequencies. In such cases, transfer impedance, Z_{21}, can reveal information that is otherwise buried in the input impedance results. The scattering parameter, S_{21}, between two different ports in the power bus, which is a function of the transfer impedance, Z_{21}, is often used to study the noise voltage generated in the power bus due to a current drawn from another location away from the observation port. For both Z_{11} and S_{21}, a lower magnitude indicates a lower noise voltage generated in the power bus due to the same amount of noise current. In other words, the lower the magnitude is, the better the power bus performance.

Bonding pads designed for decoupling capacitors were chosen as the testing ports, and the S-parameters were obtained from a vector network analyzer. Figure 2 and Figure 4 show the $|S_{21}|$ versus frequency curves for the 1.5V/GND and 3.3V/GND pair, respectively, while Figure 3 and Figure 5 show the corresponding $|Z_{21}|$ results that are calculated from the S-parameter measurements.

At frequencies below 10 MHz, all the curves clearly demonstrate that the BC12TM boards have the lowest power bus impedance; hence, their performance in noise reduction in this frequency range is the best among all types of the boards. BC12 is slightly trailing behind, followed by BC24. The standard boards are obviously the worst.

When frequency is higher than 10 MHz, as discussed earlier, the $|Z_{11}|$ curves are dominated by the port inductance (notice the magnitude increases at a rate of approximately 20 dB per decade, which indicates an inductive behavior). However, the $|S_{21}|$ curves still show the differences among the boards up to the GHz range. The benefits of the FaradFlex cores in these bare boards in terms of power bus impedance reduction are clearly demonstrated, especially for the 3.3V/GND pair due to their lower power bus impedance.

It is worth mentioning that the distributed resonant frequencies in the BC12TM boards are relatively lower than those in the others. This is because BC12TM has a slightly larger dielectric constant, which makes the electrical sizes of the boards bigger.

Two port measurements at the top and bottom of the same via [4] could be used to eliminate the effects of the ports and thus effectively quantify the performance of the thin laminate core. However, in this study, we are not interested in the core itself, we want to evaluate the performance when the core is used in a practical multi-layer PCB. The way we chose to make the measurements resembles what a real IC will see from its power and ground pins.

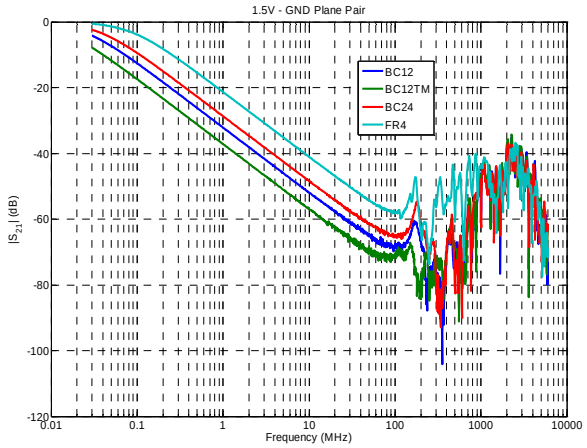

Figure 2: Measured bare board S21: 1.5V/GND pair.

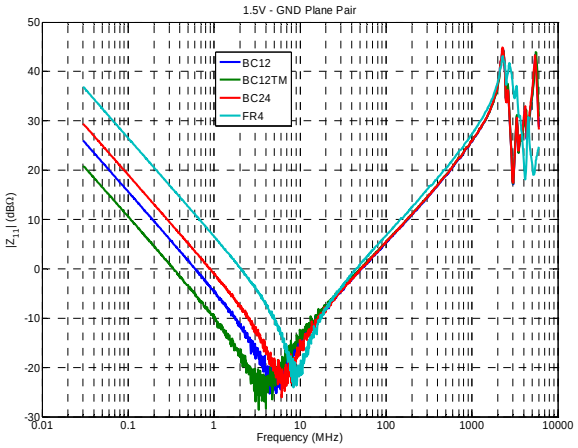

Figure 3: Simulated bare board Z11: 1.5V/GND pair.

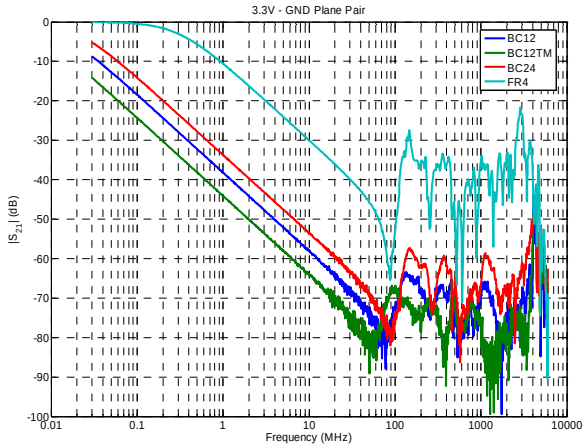

Figure 4: Measured bare board S21: 3.3V/GND pair.

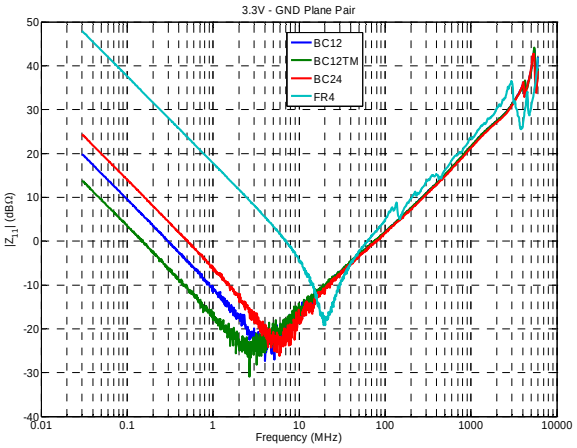

Figure 5: Simulated bare board Z11: 3.3V/GND pair.

Time-Domain Power Bus Noise Measurements

Time-domain power bus noise measurements were taken when the boards are running under a pseudo-functioning script. Again, bonding pads for decoupling capacitors were used as ports, and a flexible coaxial cable was used to connect the port to the Agilent Infiniium 54855A Digital Sampling Oscilloscope. The ac noise voltage was measured using a dc blocking capacitor to prevent damage to the oscilloscope.

Figure 6, Figure 7, Figure 8, and Figure 9 show the power bus noise voltage in the 1.5V/Ground pair measured at one location for the FR4, BC24, BC12, and BC12TM boards, respectively. The noise voltages in the 3.3V/Ground pair at different location are given in Figure 10, Figure 11, Figure 12, and Figure 13.

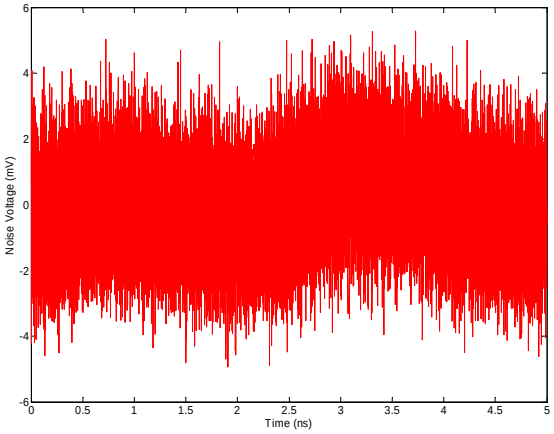

Figure 6: Time-domain power bus noise: 1.5V/GND pair, FR4 (C938).

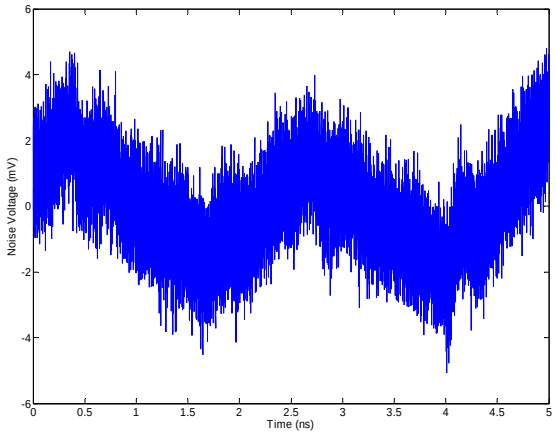

Figure 7: Time-domain power bus noise: 1.5V/GND pair, BC24.

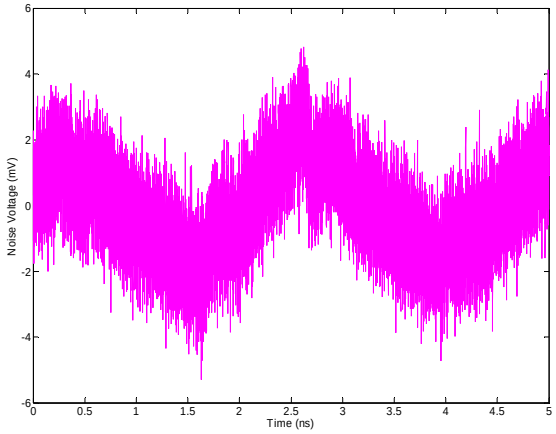

Figure 8: Time-domain power bus noise: 1.5V/GND pair, BC12.

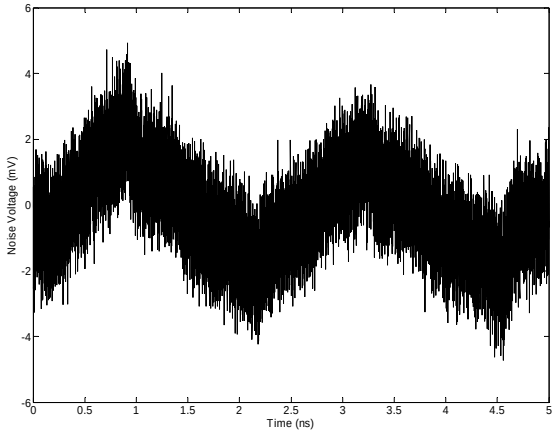

Figure 9: Time-domain power bus noise: 1.5V/GND pair, BC12TM.

From these figures, the FaradFlex® boards have comparable time-domain performance, which is less noisy compared to the standard FR4 boards. For the 1.5V/GND pair, the peak-to-peak noise voltages are approximately the same for all types of the boards. As illustrated in Figure 6, Figure 7, Figure 8, and Figure 9, this peak-to-peak value is dominated by the lower frequency envelop. The higher frequency noise modulated on the envelope is reduced in the FaradFlex boards. For the 3.3V/GND pair, even the overall peak-to-peak noise voltage is lower in the FaradFlex boards than the standard FR4 boards, as illustrated in Figure 10, Figure 11, Figure 12, and Figure 13.

Overall speaking, the embedded capacitance boards result in lower power bus noise. This is achieved when all the high-frequency SMT decoupling capacitors are removed. It is noteworthy that all the FaradFlex boards functioned correctly, with only embedded capacitance layers and bulk decoupling capacitors.

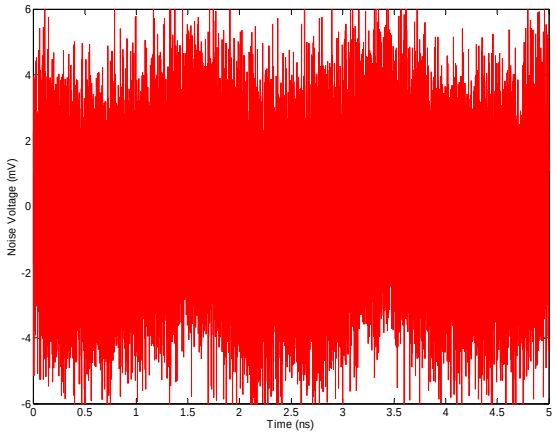

Figure 10: Time-domain power bus noise: 3.3/GND pair, FR4 (C131).

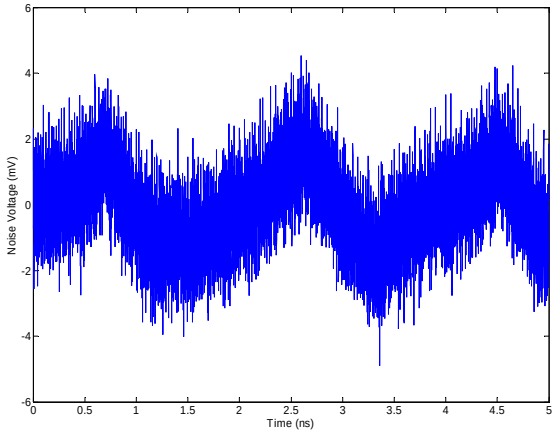

Figure 11: Time-domain power bus noise: 3.3V/GND pair, BC24.

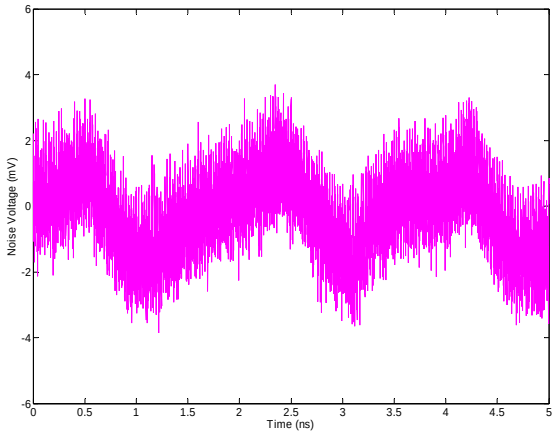

Figure 12: Time-domain power bus noise: 3.3V/GND pair, BC12.

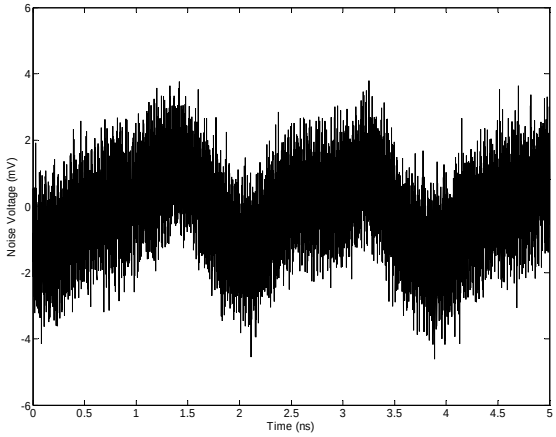

Figure 13: Time-domain power bus noise: 3.3V/GND pair, BC12TM.

Several locations in both the 1.5V/GND and the 3.3V/GND pair were tested. We found the results in one particular location a bit inconsistent to others. The BC12TM board was found to be noisy at this particular test port location. Measurements were carefully repeated and the results were corroborated. Currently this measurement is unexplained.

Frequency-Domain Power Bus Noise Measurements

The power bus noise at the same port locations was measured in the frequency domain as well. An Agilent E7404A EMC Analyzer (a spectrum analyzer) was used with a resolution bandwidth of 10 KHz. Again the dc component was filtered away by a built-in dc block.

The results in the 1.5V/GND pair in the frequency band from 10 MHz to 1 GHz are shown in Figure 14, Figure 15, Figure 16, and Figure 17, for the FR4, BC24, BC12 and BC12TM boards, respectively. The corresponding 3.3V/GND pair results are presented in Figure 18 to Figure 21.

It is quite difficult to draw definite conclusions from these frequency-domain results due to their complexity. Although the noise voltages at some frequencies are lower in the FaradFlex® boards, for example, at the three peaks between 200 MHz and 500 MHz as shown in Figure 14 to Figure 17, the noise magnitudes at some other frequencies are actually higher. Measurements in the future at frequencies higher than 1 GHz may assist in the development of insight.

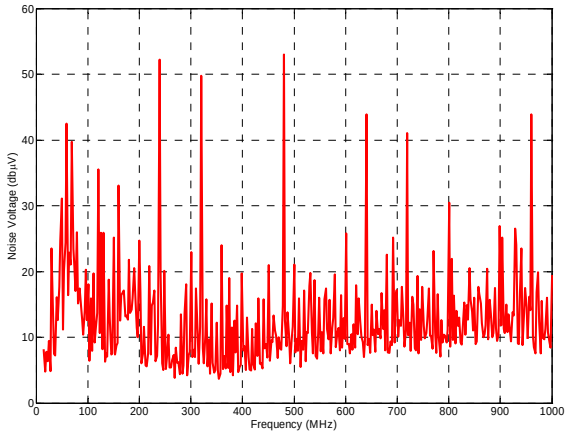

Figure 14: Frequency-domain power bus noise: 1.5V/GND pair, FR4.

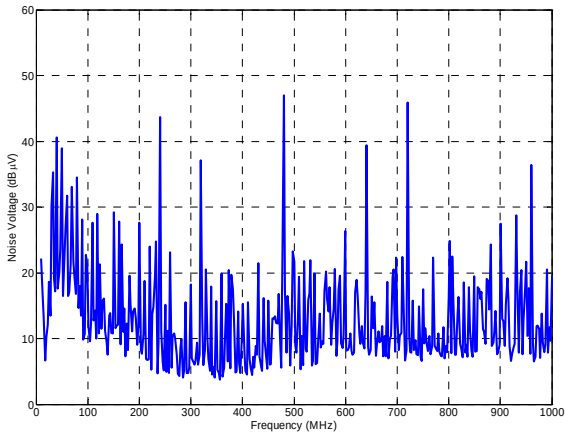

Figure 15: Frequency-domain power bus noise: 1.5V/GND pair, BC24.

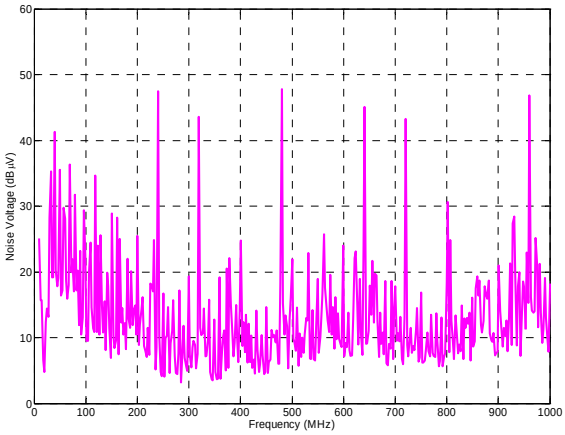

Figure 16: Frequency-domain power bus noise: 1.5V/GND pair, BC12.

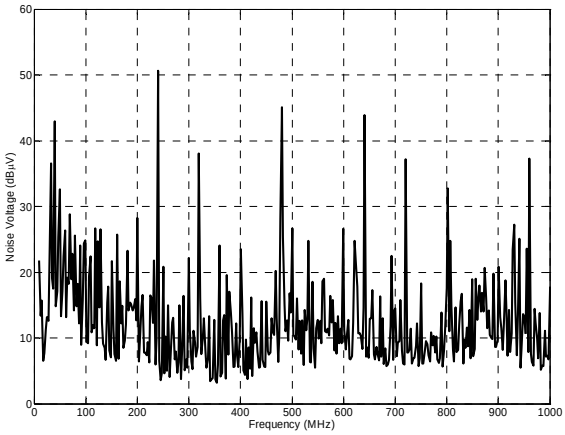

Figure 17: Frequency-domain power bus noise: 1.5V/GND pair, BC12TM.

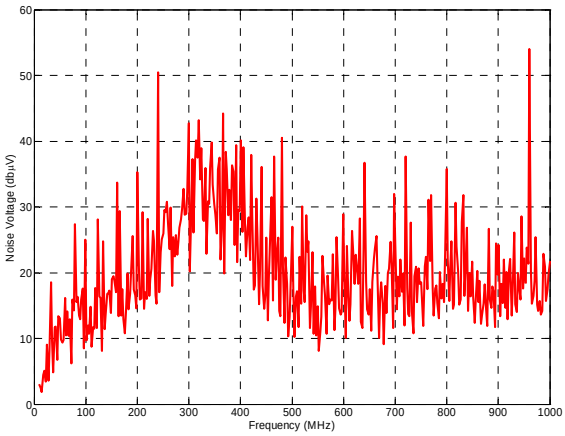

Figure 18: Frequency-domain power bus noise: 3.3V/GND pair, FR4.

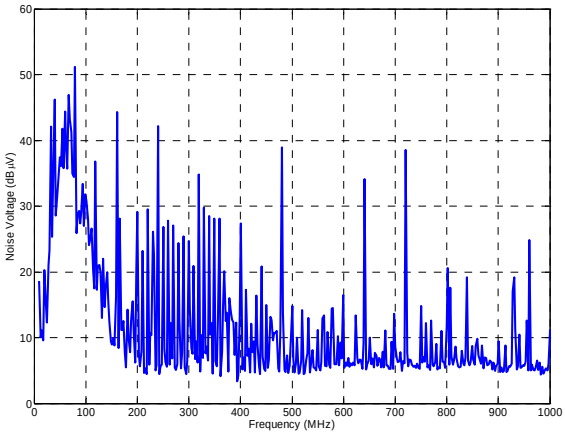

Figure 19: Frequency-domain power bus noise: 3.3V/GND pair, BC24.

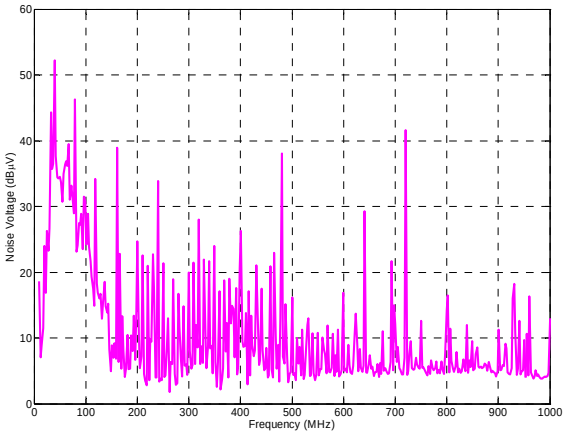

Figure 20: Frequency-domain power bus noise: 3.3V/GND pair, BC12.

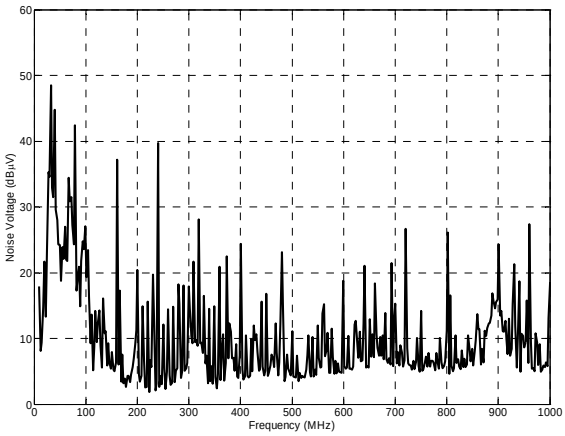

Figure 21: Frequency-domain power bus noise: 3.3V/GND pair, BC12TM.

Simulation Results

The simulation has been performed to compare the result with actual board measurement utilizing EMIStream which was developed by NEC. This simulation calculates impedance (Z_{11}) of a power plane based on PEEC (Partial Element Equivalent Circuit Model) method and Spice simulation. The parameters for this target PCB such as thickness between power and ground plane, Dk and copper thickness have been set prior to running simulation. Also the excitation point has been set at the exact same point as where the actual board measurement was probed.

The simulation results for 3.3V/GND plane are shown in Figure 22 to compare the results between standard FR4 with BC24, BC12 and BC12TM. As shown in figure 5, at the low frequencies below 20 MHz, BC12TM board had the lowest impedance followed by BC12 and BC24. Standard FR4 had the highest impedance.

Apparently, this simulation results shown in figure 22 and measurement results shown in figure 5 are well correlated. This proves the possibility to calculate impedance with PWB information before fabricating a board for optimum PDN design.

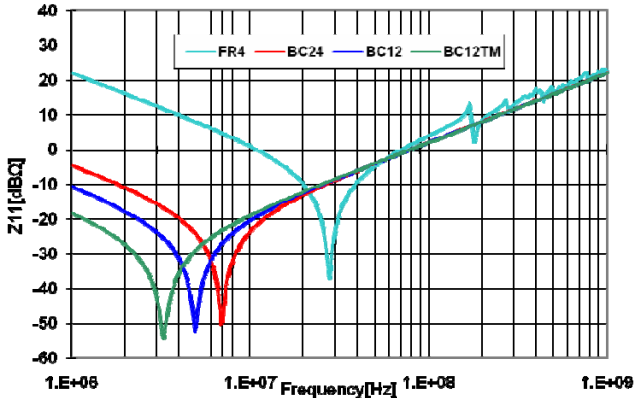

Figure 22: Simulation Result for 3.3V/GND plane between FR4, BC24, BC12 and BC12TM

Cost/Performance Analysis

The cost of a FaradFlex printed circuit board assembly is compared against a standard material assembly for this application. Taking into consideration the cost reduction by removing the capacitors and their associated assembly cost, the estimated cost increase is 8%, 15%, and 26% for the BC24, BC12, and BC12TM assemblies respectively. One reason the cost is higher is the fact that the board had to be redesigned from a 12 layer to a 14 layer. For many applications the layer count would remain the same. Also the BC materials are more expensive than standard FR4.

A larger benefit of removing the capacitors is the area freed up for trace routing and decreasing the board size, which depends upon the application, mechanical constraints

and the number of capacitors required. The cost differences and benefits will vary depending upon the application and volume.

Conclusions

Several FaradFlex® thin laminate materials were applied to a functioning high-speed switch design. Initial measurements and simulations clearly demonstrate the benefits of these embedded capacitance materials used as power/ground plane pair, in terms of lowering power bus impedance and reducing power bus noise. These thin power/ground layers achieved a comparable or even better performance with bulk decoupling capacitors only.

The simulated and actual results compared favorably and the decision to remove all the decoupling capacitors proved to be effective. We still need to investigate the time domain anomalies for the 1.5 volt planes using BC12TM material.
Although the initial cost analysis of implementing BC is higher than the standard board with capacitors, we still need to consider the other benefits to complete the analysis. Designs that do not need additional layers added will be easier to cost justify.

By using the team approach, we effectively evaluated the Buried Capacitance™ technology by utilizing the strengths of each of the team members and having constant and open communication.

Acknowledgments

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