# $V_{\rm TH}$-Hopping Scheme to Reduce Subthreshold Leakage for Low-Power Processors

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***Abstract*—In order to suppress the power consumption in low-voltage processors, a threshold voltage hopping ($V_{\rm TH}$-hopping) scheme is proposed where the threshold voltage is dynamically controlled through software depending on a workload. $V_{\rm TH}$-hopping is shown to reduce the power to 18% of the fixed low-threshold voltage circuits in 0.5-V supply voltage regime for multimedia applications. A positive back-gate bias scheme with $V_{\rm TH}$-hopping is presented for the high-performance and low-voltage processors. In order to verify the effectiveness of $V_{\rm TH}$-hopping, a small-scale RISC processor with $V_{\rm TH}$-hopping capability and the positive back-gate bias scheme is fabricated in a 0.6-$\mu$m CMOS technology. MPEG4 encoding is simulated based on the measured data. The result shows that 86% power saving can be achieved by using $V_{\rm TH}$-hopping compared with the fixed positive back-gate bias scheme.**

***Index Terms*—Back-gate bias, hardware–software cooperation, low-voltage processor, multimedia applications, $V_{\rm TH}$-hopping.**

## I. Introduction

HIGH-PERFORMANCE VLSI design with low supply voltage ($V_{DD}$) becomes one of the most important issues in CMOS VLSIs, since main-stream $V_{DD}$ will be scaled down to below 0.5 V in the coming years. The power and the delay dependence on the threshold voltage at 0.5 V $V_{DD}$ are shown in Fig. 1. As seen from the figure, the threshold voltage ($V_{\rm TH}$) has to be decreased to achieve high performance. Reducing $V_{\rm TH}$, however, could cause a significant increase in the static leakage power component. In particular, when the threshold voltage is lower than 0.1 V, the leakage power becomes a dominant component in the total power consumption even in the active mode. In order to suppress the power consumption in low-voltage processors, it is necessary to reduce the leakage power component in the active mode.

Fig. 2 shows the power reduction techniques. Dual-$V_{DD}$ [1] and $V_{DD}$-hopping [2] mainly reduce the dynamic power and not the leakage power. Boosted gate MOS [3], MTCMOS [4], and VTCMOS [5] reduce the stand-by leakage power and not the power in the active mode. Thus, these schemes cannot suppress the leakage power in the active mode, which becomes the dominant component in total power consumption in low-voltage processors. Another approach is dual-$V_{\rm TH}$ [6]. In dual-$V_{\rm TH}$ technique, logic gates are partitioned into critical and noncritical paths, and low-$V_{\rm TH}$ transistors are only used for the logic gates in the critical paths. The drawback of dual-$V_{\rm TH}$ is that the leakage current cannot be sufficiently suppressed since the large leakage current always flows through the low-$V_{\rm TH}$ transistors.

This paper presents a dynamic threshold voltage hopping ($V_{\rm TH}$-hopping) scheme that can solve the above-mentioned problems. This scheme utilizes dynamic adjustment of frequency and $V_{\rm TH}$ through back-gate bias control depending on the workload of a processor. When the workload is decreased, less power would be consumed by increasing $V_{\rm TH}$. This approach is similar to dynamic $V_{DD}$ scaling (DVS) [7]. In the DVS scheme, $V_{DD}$ and the frequency are controlled dynamically based on the workload variation. The DVS, however, is effective when the dynamic power is dominant. On the other hand, $V_{\rm TH}$-hopping is effective in the low $V_{DD}$ designs where

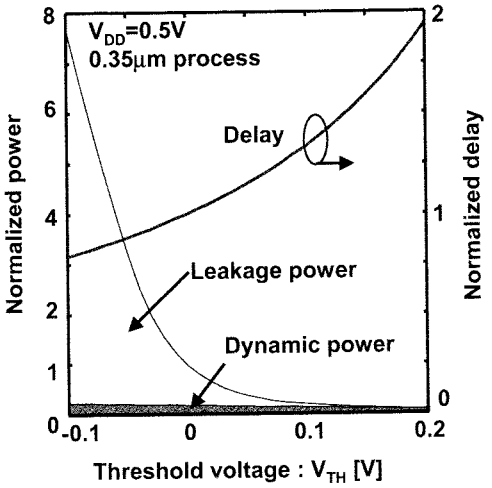


Fig. 1. Power and delay dependence on threshold voltage ($V_{\rm TH}$).

| | Active | Stand-by |
|---|---|---|
| Multiple $V_{DD}$ | Dual-$V_{DD}$ | Boosted gate MOS |
| Variable $V_{DD}$ | $V_{DD}$-hopping | |
| Multiple $V_{TH}$ | Dual-$V_{TH}$ | MTCMOS |
| Variable $V_{TH}$ | $V_{TH}$-hopping | VTCMOS |

Software-hardware cooperation

Fig. 2. Power reduction techniques.

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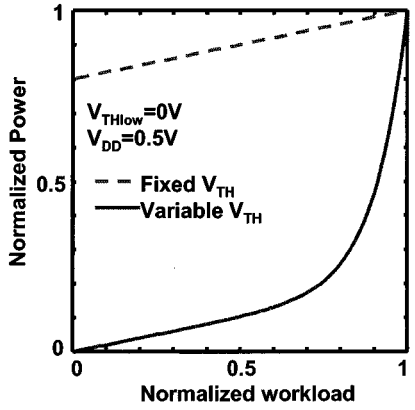


Fig. 3. Power dependence on workload.

$V_{\rm TH}$ is low and the active leakage component is dominant in total power consumption.

The rest of the paper is organized as follows. In Section II, a new hardware–software cooperative power control scheme, which is called $V_{\rm TH}$-hopping, is proposed to suppress the power consumption in low-voltage processors. In order to show the effectiveness of the $V_{\rm TH}$-hopping scheme, performance evaluation is conducted using MPEG-4 video coding in Section III. In Section IV, a small-scale RISC processor with $V_{\rm TH}$-hopping capability is fabricated. Finally, Section V summarizes the work.

## II. $V_{\rm TH}$-Hopping Scheme

Fig. 3 shows the total power consumption depending on the workload. $V_{\rm THlow}$ signifies $V_{\rm TH}$ applied when the workload is maximum. The dynamic power ($P_D$) and subthreshold leakage power ($P_{\rm LEAK}$) are written as

$$P_D = afCV_{DD}^2, \tag{1}$$

$$P_{\rm LEAK} = I_0 \cdot 10^{-V_{\rm TH}/S} \cdot V_{DD} \tag{2}$$

where $a$ is the switching activity, $f$ is the operation frequency, $C$ is the load capacitance, $I_0$ is the leakage current when $V_{\rm TH} = 0$ and $S$ is the subthreshold slope factor. Fig. 3 is calculated from these formulas.

The broken line represents a fixed $V_{\rm TH}$ case with only a frequency control. If the workload is less than the peak workload, frequency can be decreased to the level where the speed requirement is just satisfied. The dynamic power consumption decreases in proportion to the workload, since the dynamic power is proportional to the frequency [see (1)]. The leakage power, however, is not reduced since it does not depend on the frequency, as is seen from (2). The straight line in the figure shows the power dependency of the variable $V_{\rm TH}$ system on the workload. When the workload is lower than the maximum workload (i.e., workload $<1$), the higher threshold voltage can be used while guaranteeing the logic blocks to work with the lower frequency. As is shown in Fig. 3, it is clear that the total power is decreased effectively with dynamic $V_{\rm TH}$ control depending on the workload. This sets the basis for the $V_{\rm TH}$-hopping.

The schematic diagram of the $V_{\rm TH}$-hopping scheme is shown in Fig. 4. Using the control signal (CONT) which is sent from the processor, the power control block generates select signals of $V_{\rm TH}$s, $VTHlow\_Enable$ and $VTHhigh\_Enable$, which in turn control substrate bias for the processor. When the $V_{\rm TH}$ controller asserts $VTHlow\_Enable$, $V_{\rm TH}$ in the target processor becomes $V_{\rm THlow}$. On the other hand, when the $V_{\rm TH}$ controller asserts $VTHhigh\_Enable$, $V_{\rm TH}$ in the target processor becomes $V_{\rm THhigh}$. CONT is controlled by software through a software feedback loop scheme [2], which has been proposed for dynamic $V_{DD}$ scaling (DVS) but is also effective for $V_{\rm TH}$-hopping. The software feedback scheme can guarantee hard real-time for multimedia applications with the DVS and the same algorithm guarantees the real-time operation with $V_{\rm TH}$-hopping, since, software-wise, the DVS and $V_{\rm TH}$-hopping are the same.

CONT also controls the operation frequency of the target processor. When the $V_{\rm TH}$ controller asserts $VTHlow\_Enable$, the frequency controller generates $f_{\rm CLK}$, and when the $V_{\rm TH}$ controller asserts $VTHhigh\_Enable$, the frequency controller generates $f_{\rm CLK}/2$. If necessary, the power control block can be extended so that more than two sets of frequency and threshold voltage can be generated. In order to avoid the synchronization problem at the interface of the processor with the external systems, the frequency has only discrete values of $f_{\rm CLK}$, $f_{\rm CLK}/2$, $f_{\rm CLK}/3$, ....

$V_{\rm THlow}$ is determined so that the maximum performance of the processor achieves the required clock frequency of $f_{\rm CLK}$. On the other hand, $V_{\rm THhigh}$ is determined so that the processor operates at $f_{\rm CLK}/2$.

Fig. 5 shows the power and the performance dependence on the back-gate bias ($V_{\rm BS}$). The back-gate bias for $V_{\rm TH}$-hopping is not only limited to negative value but also can be positive. The negative back-gate biasing is effective in the low-$V_{\rm TH}$ design in which the active leakage power is dominant. Using the negative back-gate biasing, the active leakage power can be suppressed effectively. It is suspected, however, that the strong negative biasing may be difficult in the future since the strong negative biasing enhances a short-channel effect and the band-to-band tunneling (BTBT), which induces leakage [8], [9]. In order to improve the effect of $V_{\rm TH}$-hopping, a positive and negative combined back-gate bias scheme would be ideal. The lowest $V_{\rm TH}$ is achieved by positive back-gate bias and the highest $V_{\rm TH}$ is obtained by negative back-gate bias. Compared with the negative back-gate bias scheme, the effect of $V_{\rm TH}$-hopping with the positive and negative combined back-bias scheme is improved since the wider range of the threshold voltage can be realized when the negative back-gate bias is limited.

The algorithm to adaptively change $V_{\rm TH}$ depending on the workload is of importance. Since the workload strongly depends on data, the control should be dynamic in real time and should not be static at compile time. On the other hand, it is impossible to predict the workload of the task to be done in the future without error.

In order to solve this problem, the algorithm with software feedback loop, which is shown in Fig. 6, is used for $V_{\rm TH}$-hopping. Most real-time applications have a given time interval in which a certain amount of tasks should be executed. For example, a real-time MPEG4 application performs video coding at 15 frames per second. This time interval is called a sync frame

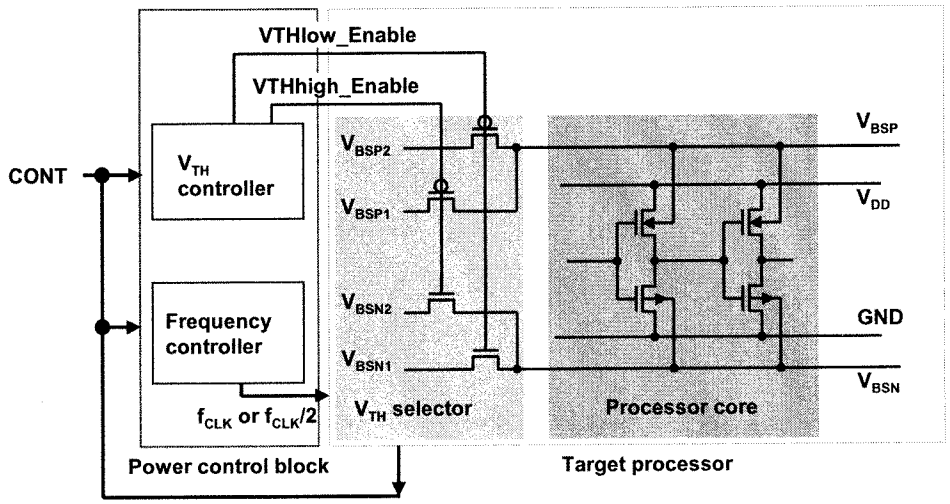


Fig. 4. Schematic diagram of $V_{\rm TH}$-hopping.

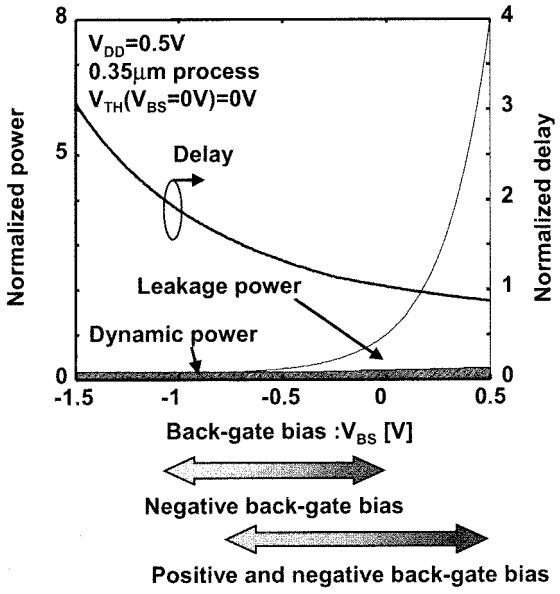


Fig. 5. Power and delay dependence on back-gate bias ($V_{\rm BS}$).

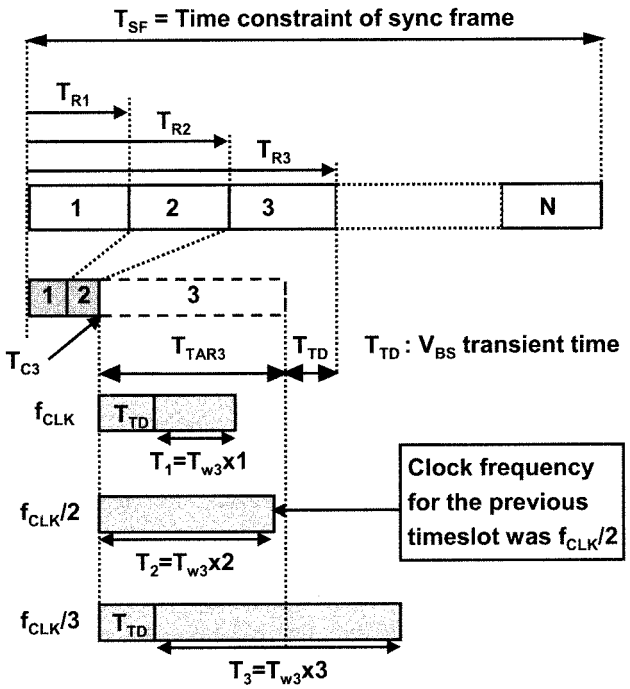


Fig. 6. Determination of $V_{\rm TH}$ and frequency.

($T_{\rm SF}$). Here, the following algorithm is used to guarantee the real-time execution.

1) Every sync frame is divided into $N$ slices called timeslots. The frequency and the threshold voltage of the target processor are determined for each timeslot.
2) For each timeslot, the target execution time, $T_{\rm TAR}$, is calculated. The execution time accumulated from the first to $(i-1)$th timeslots, $T_{Ci}$, can be taken from the internal timer in the power control chip. The target execution time for timeslot $i$, $T_{\rm TARi}$, is calculated as $T_{\rm TARi} = T_{Ri} - T_{Ci} - T_{\rm TD}$, where $T_{\rm TD}$ is the transition delay to change a clock frequency and threshold voltage and $T_{Ri}$ is execution time limit of the timeslot $i$.
3) For each clock frequency ($f_{\rm CLK}/j$, $j = 1, 2, 3, \ldots$), the estimated worst-case execution time (WCET) is calculated as $T_j = T_{Wi} \times j$. $T_{Wi}$ is the worst-case execution time of timeslot $i$. There is no transition delay ($T_{\rm TD}$) if the clock frequency is the same as the clock frequency used in the previous timeslot. On the other hand, if the frequency is not equal to the previous clock frequency, $T_j = T_j + T_{\rm TD}$.
4) The clock frequency is determined as a minimum frequency whose estimated worst case execution time does not exceed the target time ($T_{\rm TARi}$).

Thus, the frequency and $V_{\rm TH}$ are dynamically controlled on a timeslot-by-timeslot basis inside each task by software.

This algorithm is based on the concept of the run-time voltage hopping scheme [2]. The algorithm can be applied to such real-time applications whose worst case execution time (WCET) is known, for example, MPEG2 and VSELP speech encoding. In [2], three typical real-time applications such as MPEG4 video encoding, MPEG2 video decoding, and VSELP speech encoding were simulated and the effectiveness of the

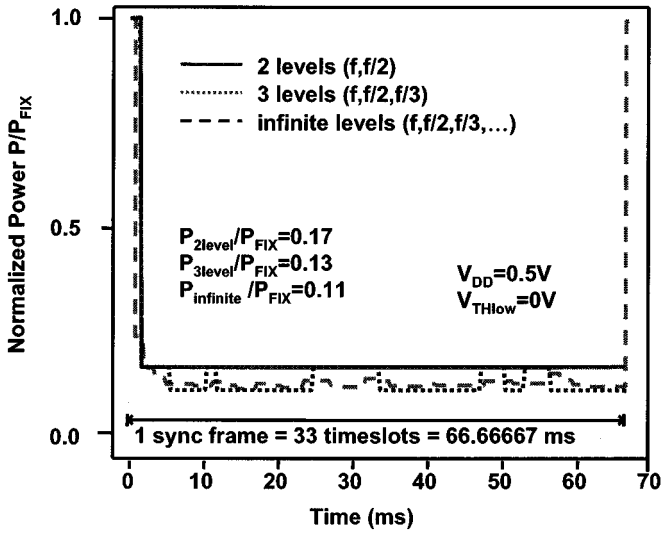


Fig. 7. Power transition of $V_{\rm TH}$-hopping.

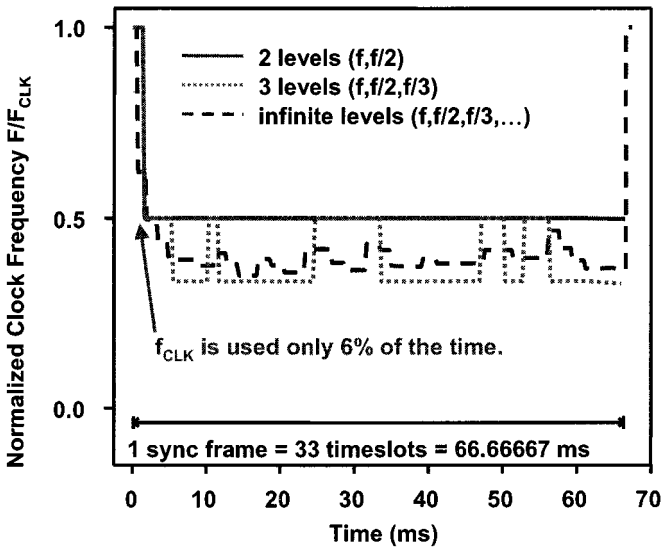


Fig. 8. Frequency transition of $V_{\rm TH}$-hopping.

scheme has been verified. As for robustness, this algorithm guarantees the hard real-time execution of an application if a processor can execute the application in real time with the constant higher frequency.

## III. Simulation Results of MPEG4 Encoding Using $V_{\rm TH}$-Hopping

In order to show the effectiveness of the scheme, performance evaluation is conducted using MPEG-4 video coding.

Fig. 7 shows a simulation result of power transition in time for MPEG4 encoding case using $V_{\rm TH}$-hopping. In this simulation, the transition delay ($T_{\rm TD}$) is set to 0.5 ms. If more than two clock levels, hence more than two $V_{\rm TH}$ levels, are provided, more power reduction is possible but the improvement is minor (only 6%), as is shown in the figure. Moreover, if more levels are provided, there are test issues since speed test should be run at more than two frequencies and more area overhead is needed for the control block and selectors, and controlling $V_{\rm TH}$ through $V_{\rm BS}$ becomes difficult since the negative back-gate bias for $f_{\rm CLK}/3$ and slower is higher than 1 V where the short-channel effects and the BTBT are enhanced. This is why the number of $V_{\rm TH}$ levels is limited to two. Only two levels, that is, $f_{\rm CLK}$ and $f_{\rm CLK}/2$, are sufficient, meaning that the proposed scheme is simple, in both software and hardware.

It is seen from Fig. 8 that $f_{\rm CLK}$ is used only 6% of the time while the processor is run at $f_{\rm CLK}/2$ for 94% of the time. $f_{\rm CLK}$ is still needed because the processor will run at $f_{\rm CLK}$ for 100% of the time when the worst-case data comes, which is very unlikely, and for most of the time the workload is about half on average. This tendency holds for other applications such as MPEG2 decoding and VSELP voice codec.

Fig. 9 shows the simulation result of a power comparison among fixed single $V_{\rm TH}$, dual-$V_{\rm TH}$, and $V_{\rm TH}$-hopping cases for MPEG4 encoding. Dual-$V_{\rm TH}$ [6] can reduce the power only to 65% of the fixed single $V_{\rm TH}$ case since the leakage power of the low-$V_{\rm TH}$ gates cannot be suppressed. $V_{\rm TH}$-hopping can reduce the power to 18% of fixed low-$V_{\rm TH}$ circuit and 27% of the

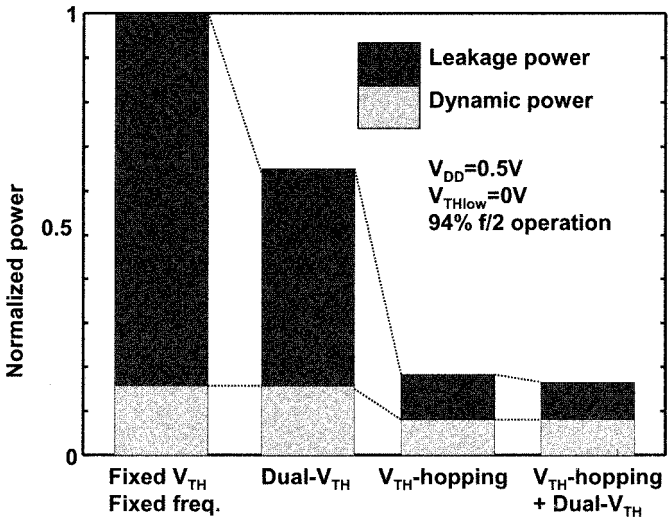


Fig. 9. Power comparison among single fixed $V_{\rm TH}$, dual-$V_{\rm TH}$, and $V_{\rm TH}$-hopping.

dual-$V_{\rm TH}$ scheme in 0.5-V $V_{\rm DD}$ regime. Thus, $V_{\rm TH}$-hopping is effective in the low supply voltage design where the threshold voltage is low and the active leakage component is dominant in total power consumption.

In order to suppress the leakage power further, combining the $V_{\rm TH}$-hopping scheme and the dual-$V_{\rm TH}$ scheme could be useful. Fig. 10 shows the schematic of this scheme. In this scheme, $V_{\rm TH}$-hopping is used only in the critical paths. On the other hand, $V_{\rm TH}$ of the noncritical gates is set to a considerably higher value ($V_{\rm THnon\_crit}$), which is not changed for the entire time.

As shown in Fig. 9, however, the above mentioned combination scheme hardly improves the power (only 9%) compared with the $V_{\rm TH}$-hopping scheme. The reason is that the difference between the leakage power in the critical paths and the leakage power in the noncritical paths is small since the leakage power in the critical paths has already been suppressed by using $V_{\rm TH}$-hopping. Therefore, it can be said that the scheme using only $V_{\rm TH}$-hopping is the most effective.

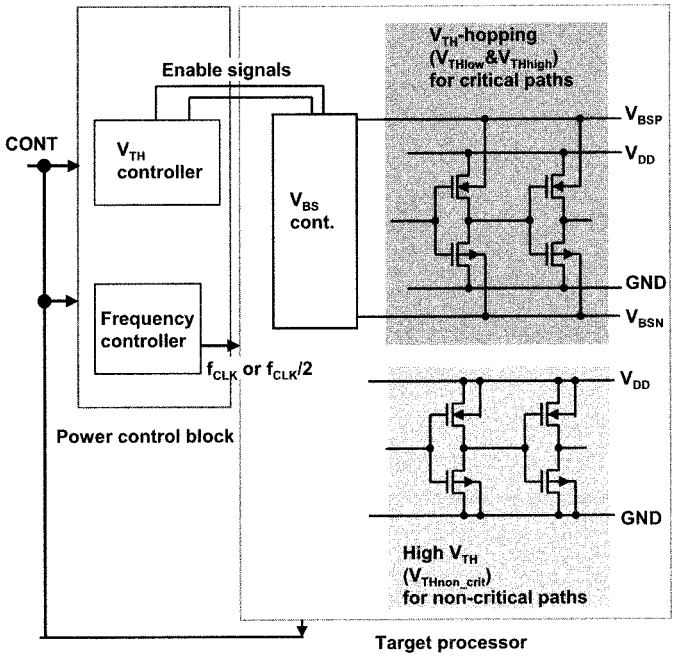


Fig. 10. Schematic diagram of design which combines $V_{TH}$-hopping and dual-$V_{TH}$.

## IV. Measurement of RISC Processor With $V_{TH}$-Hopping

As is mentioned in Section III, the negative back-gate bias scheme and positive and negative back-gate bias scheme are effective in the low-$V_{TH}$ design where the active leakage power is dominant. The negative back-gate biasing, however, has little effect on the total power in the conventional high-threshold voltage designs where the active leakage power is much smaller than the dynamic power. On the other hand, the positive back-gate bias scheme is compatible with the conventional high-threshold voltage design. The performance of the processor can be improved since the lower threshold voltage can be achieved by positive back-gate biasing [10]. The drawback of this scheme is that the forward junction leakage current, which occurs between drain and back-gate, increases exponentially.

In order to suppress the forward junction leakage current, combining $V_{TH}$-hopping and the positive back-gate bias is effective. For example, the low threshold voltage ($V_{THlow}$) is realized by positive back-gate bias to improve the performance and the high threshold voltage ($V_{THhigh}$) is achieved by zero back-gate bias to suppress the leakage power.

A small-scale RISC processor with $V_{TH}$-hopping capability and the positive back-gate bias scheme is fabricated in a 0.6-$\mu$m CMOS technology. The area overhead of the $V_{TH}$-hopping scheme is 14%. This includes the additional $V_{BSP}$ and $V_{BSN}$ lines in the standard cell area and the area of $V_{BS}$ selector. A microphotograph of the RISC processor appears in Fig. 11. The size of RISC core is 2.1 mm $\times$ 2.0 mm and the size of the $V_{BS}$ selector is 0.2 mm $\times$ 0.6 mm.

In normal standard cells, the n-well bias voltage and the p-well bias voltage are fixed at $V_{DD}$ and ground, respectively, since the well contacts and substrate contacts are connected to the $V_{DD}$ and ground lines. In order to design a processor with $V_{TH}$-hopping, it is necessary that the n-well bias and the p-well

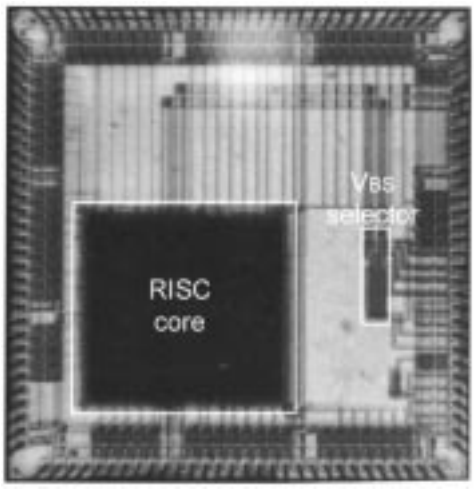


Fig. 11. Microphotograph of RISC processor.

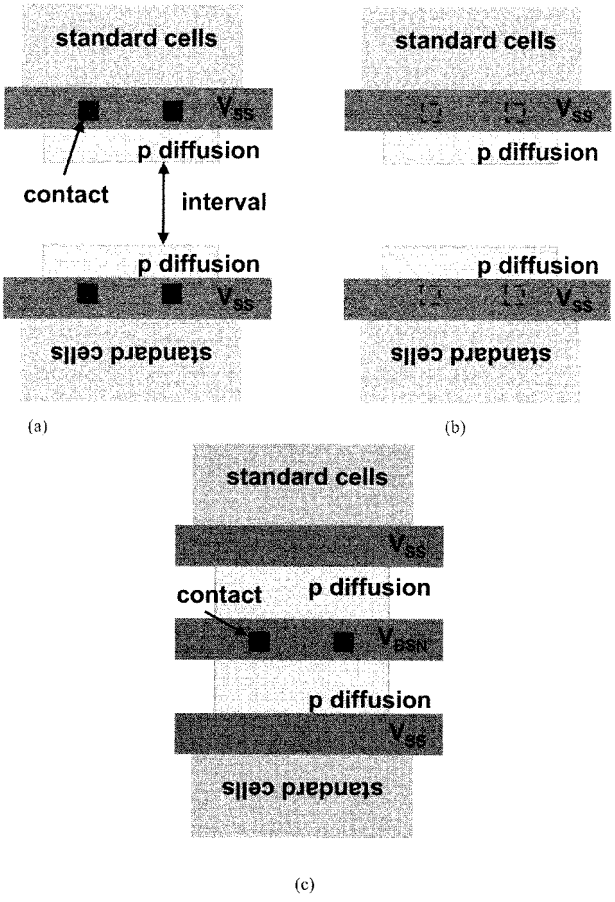


Fig. 12. Place and route using conventional standard cells.

bias can be changed freely. In this study, a simple yet effective design methodology for the $V_{TH}$-hopping is adopted using the commercially available CAD tools [11], [12] and normal standard cells. Fig. 12 shows the detailed process of the place and route (P&R) [11] for $V_{TH}$-hopping, which is summarized as follows.

1) Place and route is executed using the conventional standard cells. In order to add metal lines for $V_{BSP}$ and $V_{BSN}$,

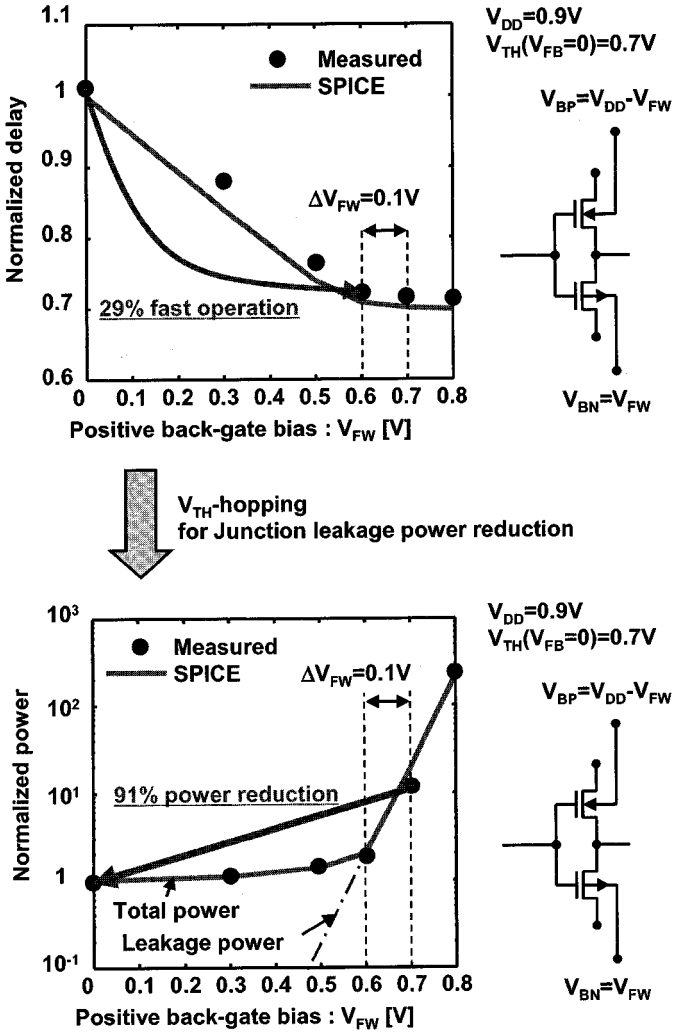


Fig. 13. Measured results of delay and power of $V_{\rm TH}$-hopping with positive back-gate bias.

the standard cells are placed at appropriate intervals, which can be done by using the conventional place and route tool with an appropriate parameter [Fig. 12(a)].

2) Well contacts located on the $V_{\rm DD}$ line and well contacts (or substrate contacts) located on the ground line are removed by using SKILL script [12] [Fig. 12(b)].
3) The n-well pattern, p-well pattern, $V_{\rm BSP}$ lines, $V_{\rm BSN}$ lines, and well/substrate contacts are added to the gap between the standard cells [Fig. 12(c)].

The advantage of this technique is that the standard cells need not be modified at all. If the standard cells can be modified, the area overhead could be reduced to 9%.

Fig. 13 shows the measurement results and SPICE simulation results of the RISC processor using simple hand-coded programs. $V_{\rm FW}$ is the positive back-gate bias voltage and $\Delta V_{\rm FW}$ is the peak-to-peak $V_{\rm FW}$ variation which is set to 0.1 V ($\pm$6% of $V_{\rm DD}$). The variation of $V_{\rm FW}$ includes process variation, temperature variation, and noise of $V_{\rm BSN}$ and $V_{\rm BSP}$ lines. We assumed that the lowest positive back-gate bias is 0.6 V and the highest positive back-gate bias is 0.7 V. When the positive back-gate bias is asserted, the worst delay occurs at the lowest $V_{\rm FW}$. The delay improves 29% at 0.9 V $V_{\rm DD}$ with 0.6 V $V_{\rm FW}$. On the other hand, the worst-case leakage power occurs at the highest back-gate bias voltage, which is 0.7 V in this case. The leakage power increases exponentially when $V_{\rm FW}$ is higher than 0.6 V due to the forward junction leakage. If zero back-gate bias is applied, 91% power reduction can be achieved compared with the fixed 0.7-V positive back-gate bias scheme.

In order to verify the effectiveness of $V_{\rm TH}$-hopping with the positive back-gate bias scheme, MPEG4 encoding is simulated based on the measured data. The simulation result shows that 86% power saving can be achieved by using $V_{\rm TH}$-hopping compared with the fixed positive back-gate bias scheme.

## V. Conclusion

A threshold voltage hopping ($V_{\rm TH}$-hopping) scheme is proposed where the threshold voltage, $V_{\rm TH}$, is dynamically controlled through software depending on the workload of a processor. The $V_{\rm TH}$-hopping scheme can achieve 82% power saving compared with the fixed low-$V_{\rm TH}$ circuits in a 0.5-V supply voltage regime for multimedia applications. $V_{\rm TH}$-hopping is effective in the low $V_{\rm DD}$ designs where $V_{\rm TH}$ is low and the active leakage component is dominant in total power consumption.

A small-scale RISC processor with $V_{\rm TH}$-hopping and the positive back-gate biased scheme is fabricated. The measured data shows that if zero back-gate bias is applied, 91% power reduction was possible compared with the fixed 0.7-V positive back-gate bias scheme. Based on the measured data, performance evaluation is conducted using MPEG-4 video coding. The simulation result shows that 86% power saving can be achieved by using $V_{\rm TH}$-hopping compared with the fixed positive back-bias scheme.

## Acknowledgment

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