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Validation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop With On-Chip Delay Measurement

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***Abstract*—Power integrity is a crucial design issue for nano-meter technologies because of decreased supply voltage and increased current. We focused on gate delay variation caused by power/ground noise, and developed a full-chip simulation current model with capacitance and a variable resistor to accurately model current dependency on voltage drop. Measurement results for 90-nm technology are well reproduced in simulation. The error of average supply voltage is 0.9% in average. Measurement results also demonstrate that gate delay depends on average voltage drop.**

***Index Terms*—Delay estimation, full-chip simulation, linear element model, power-supply noise, transistor model.**

I. Introduction

POWER-SUPPLY noise has become a critical issue in current VLSI design. The power consumption of high-performance chips is still increasing, and supply voltage is decreasing, resulting in a rapid increase in current. Increased current makes power distribution more difficult, and nowadays power-supply noise can not be easily eliminated. Moreover, even when the amplitude of power-supply noise remains the same, its impact on timing becomes more and more significant as supply voltage decreases. To advance chip design, delay degradation caused by power-supply noise must be addressed.

To study on-chip power-supply noise, [1]–[4] measured noise waveforms. The effect of noise on timing, however, has been reported in few works [5], [6] and other works have been investigated through simulation [4], [7]. studied transition waveform distortion due to sharp voltage spike. Reference [6] discusses impact of power noise on clock signal. Reference [5] is a primary version of this work.

This brief discusses the gate delay variation caused by power-supply noise, comparing the results from measurement and simulation in a CMOS 90-nm technology. The contributions of this brief are as follows.

1) Demonstration on silicon that gate delay is mainly dependent on average supply voltage, not on peak voltage.
2) Construction of a full-chip simulation model that can accurately reproduce switching current dependence on noise-induced supply voltage.
3) Demonstration of agreement between delay measurement results and full-chip simulation results.

Our switching current model considerably reduces computational cost, and enables the full-chip simulation of the test chip. This work demonstrates gate delay dependence on average supply voltage on silicon, whereas [4] and [7] discussed with simulation. For this purpose, ring oscillator is suitably used for the measurement, similarly to [8].

The rest of this brief is organized as follows. Section II discusses the impact of average voltage drop on gate delay. Section III presents a full-chip simulation model that translates transistors into linear elements. Section IV describes measurement circuit structure. Section V presents and discusses the results of our measurements. Section VI concludes the brief.

II. Effect of Power Supply Noise on Timing

Peak voltage drop is a serious issue in design of a power distribution network. However, average power-supply voltage is more important than peak noise voltage where timing is the principal issue in digital circuit design because timing distortion is more dependent on average supply voltage during gate switching than on peak voltage [4].

Here, we show an example of how the impact of power-supply noise on timing can be estimated with average supply voltage. We assume the four pseudo V_{dd} noise waveforms shown in Fig. 1, referring to [2]. V_{ss} waveforms are set to be upside down to V_{dd} waveforms. A 90-nm CMOS process and an ideal supply voltage of 1.0 V are assumed. 50 cascaded inverter gates operate with the pseudo waveforms. A rise signal was input to the first gate at 0 ps, and we evaluate the average delay of gates through which the signal propagated within 500 ps. The peak voltage drop of `noise 1` is 0.2 V, and supply voltage recovers to 1.0 V in 500 ps. The average gate delays of `noise 1, 2, 3, 4` are 14.5, 12.0, and 129.8 ps, respectively.

The peak voltage drop of `noise 1` is 0.2 V and supply voltage recovers to 1.0 V in 500 ps. The voltage drop of `noise 2` is set to average the drop of `noise 1` from 0 to 500 ps. It can be seen that the average gate delay with `noise 1` is almost the same as `noise 2`, and the delay difference is only 2.0%. In contrast, though the peak voltage drop of `noise 3` is 0.3 V, which is larger than that of higher than that of `noise 1`, the average gate delay with `noise 3` is smaller because its recovery to 1.0 V is faster. Therefore, the average supply voltage of `noise 3` is higher than that of `noise 2`. If we use the voltage of the worst case drop (`noise 4`), the estimated delay is unrealistically large. Timing estimation based on average supply voltage is more accurate than that based on peak voltage drop.

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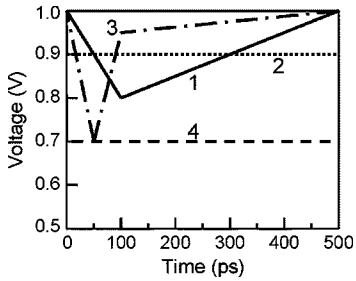

Fig. 1. Pseudo V_{dd} noise waveforms.

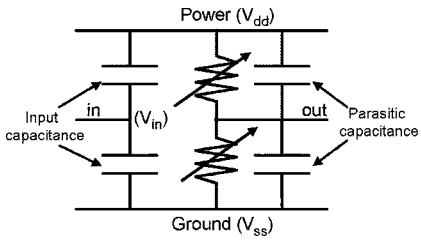

Fig. 2. Variable switch model.

III. Switching Current Model for Full-Chip Simulation

Full-chip simulation of power/ground noise uses a great deal of CPU time and memory because of the tremendous number of elements on a chip. To efficiently simulate noise for a full chip, we developed a switching current model with capacitance and a variable resistor, a so-called variable switch model. This model can reproduce the switching current dependence on noise-induced supply voltage. In this section, we begin by describing the accuracy and computational cost of the variable switch model. Then we explain the parameter characterization method of the variable switch model.

A. Accuracy and Simulation Cost of Linear Element Models

To make the simulation more efficient, transistor elements are generally replaced with linear circuit models such as current source and switch models [9]. The current source model represents a switching gate consisting of transistors as a voltage-independent current source. The switch model replaces a switching gate with resistance and capacitance [9]. The resistance value is ∞ or on-resistance of the corresponding transistor. Though supply voltage fluctuation changes the switching current, the switch model does not explicitly consider dependence of switching current on noise-induced supply voltage. The current consumption is not well reproduced in this model because the gate delay degradation due to power-supply noise is not modeled.

We developed the variable switch model which has finely-defined variable resistance. The variable switch model is shown in Fig. 2. Supposing an inverter gate, a transistor element is represented with input gate capacitance, output parasitic capacitance, and variable resistance depending on $V_{\rm in} - V_{ss}$ for nMOS and $V_{dd} - V_{\rm in}$ for pMOS. For simulating the test chip, other single state cells, e.g., 2-input NAND, are modeled as Fig. 2. Each of the pull-up and pull-down networks are replaced by a single resistor whose resistance depends on $V_{\rm in} - V_{ss}$ for nMOS or $V_{dd} - V_{\rm in}$ for pMOS. There is another detailed approach that replaces each transistor with a single resistor. However, it is not necessary for simulation in this brief, and thus it will not be discussed further.

Gate switching delay is accurately modeled in the developed model, which contributes to accurate full-chip simulation of the test chip. To distinguish between models, the conventional model with a constant resistance is called the constant switch model.

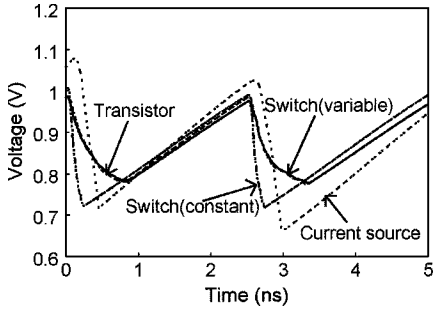

Fig. 3. Supply noise waveform with transistor model, current source model, and two switch models. The waveforms with transistor and variable switch models are overlapping.

TABLE I
Simulation Time With Each Models Normalized by That With Transistor Model. Average of Absolute Error and Modeling Time are Also Shown

	transistor	current source	constant switch	variable switch	variable sw. (merged)
Sim. time	1	0.021	0.043	0.063	0.0059
Avr. error	-	97.3mV	38.2mV	4.3mV	4.0mV
Modeling	-	10sec.	5min.	9min.	9min.

Fig. 3 shows power-supply noise waveforms simulated with the transistor model, the current source model, and the two switch models. The circuit for simulation includes 68 cells of 12-stage NAND gates. 400 times inductance of package is attached to the circuit so that the voltage drop becomes comparable to the measured voltage drop that will be demonstrated in Section V. The V_{dd} waveform at the center of the grid is shown in Fig. 3. The current source and constant switch models show sharper voltage drop waveforms than the transistor model. On the other hand, the noise waveform of the variable switch model nicely follows that of the transistor model. This is because only the variable switch model can reproduce the gate delay degradation caused by the voltage drop.

Table I shows normalized simulation time, average of absolute error from the transistor model, and the time needed for modeling. As can be seen, using the variable switch model reduces simulation time to 6.3%, which is considerable reduction. Integration of multiple cells into a single cell can further reduce simulation cost. When 68 cells in a grid are merged into 4 cells, simulation cost is decreased to 0.59%, without accuracy degradation. Clearly, the variable switch model has reasonable simulation cost and accurately estimates noise waveforms. The modeling time is also acceptable. This model can be used for full-chip simulation, which is discussed in the Section V.

B. Characterization of Variable Switch Model

In this section, we describe the characterization method for the model. To characterize the variable switch model, parameters such as variable resistances, input gate capacitances, and output parasitic capacitances must be determined. A schematic of the model is shown in Fig. 2. Variable resistance can be realized in circuit simulation with G-element [10] or behavioral description such as in Verilog-A.

We adopt the total power consumption and current waveform for determination of capacitance and resistance in variable switch model. Total power consumption mainly depends

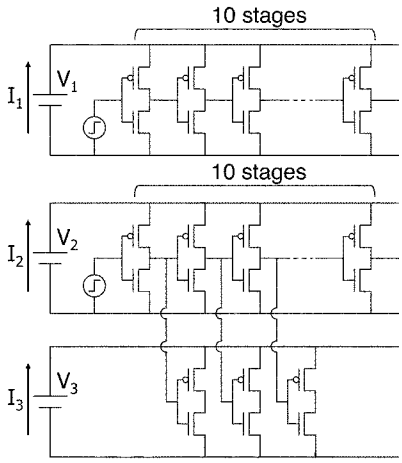

Fig. 4. Circuits used to characterize variable switch model in case of inverter gate. Supply voltage of ideal voltage source V1, V2, and V3 are the same.

on capacitance and is independent of resistance. These are determined in the following two steps. Step 1 determines capacitance based on total power consumption. Step 2 determines resistance based on current waveform. In each step, we determine parameters by minimizing the following objective functions.

In Step 1, the objective function is the difference between the integrations of current simulated with a variable switch model and of that simulated with a transistor model. Two circuits are shown in Fig. 4, which have current values of three voltage sources. These two circuits are used to simulate current because we cannot compute input and output capacitance separately with the upper circuit alone, as shown in Fig. 4. Here, $C_{\rm in}$ and $C_{\rm out}$ are input and output capacitances, respectively. Total current consumption I_1 for the upper circuit is proportional to $C_{\rm in} + C_{\rm out}$, and $C_{\rm in}$ and $C_{\rm out}$ are indistinguishable. To compute input and output capacitance separately, we use the lower circuit. Output parasitic capacitances are connected to a separate independent voltage source in the lower circuit. I_2 and I_3 are proportional to $(2C_{\rm in} + C_{\rm out})$ and $C_{\rm out}$, respectively, meaning that $C_{\rm in}$ and $C_{\rm out}$ become distinguishable. Though it is possible to determine parameters with the lower circuit alone, we use both the upper and lower circuits to improve fitting reliability. Input and output capacitances consist of capacitance between power and input/output and that between ground and input/output, respectively. The ratio between capacitance to the power and to the ground is fixed to the ratio between pMOS and nMOS width. This is because these capacitance values cannot be determined separately using the above procedure.

The objective function in Step 2 is the average absolute error of current waveform and it is expressed as an integral of $|I_{vsw}(t) - I_{tr}(t)|$ in the time range from T_1 to T_2. T_1 and T_2 are chosen such that the circuit operation for characterization are fully included in the timing range. $I_{vsw}(t)$ and $I_{tr}(t)$ are current values at time t simulated with a variable switch model and a transistor model, respectively.While minimizing the objective function, we vary resistance values and keep capacitance values unchanged. Variable resistance is piecewise linear function of $V_{dd} - V_{\rm in}$ or $V_{\rm in} - V_{ss}$. Resistance value at every $V_{dd} - V_{\rm in}$ or $V_{\rm in} - V_{ss}$ sample point is varied in this process.

As initial values of variable resistance, we adopted V_{ds}/I_{ds} values when V_{ds} is set to $V_{dd}/2$. Initial values of input capacitance are found in the datasheet of a standard cell library or can

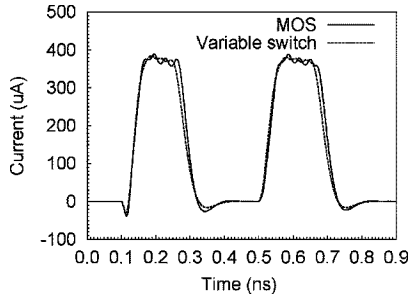

Fig. 5. Current waveform of 20X size inverter simulated with transistor model and variable switch model. Waveform in this figure is simulated with upper circuit in Fig. 4.

be calculated with T_{ox} and transistor sizes. Output parasitic capacitance can be computed with peripheral length and area of drain/source, or, for simplicity set to, for example, 20% of the input capacitance. Other common approximation methods for resistance and capacitance of MOS can be used to determine initial values.

In Fig. 5, we compare the simulation results for the inverter chain with those for the transistor and variable switch models. A variable switch model is characterized by the procedure described in this section. We use the feasible sequential quadratic programming (FSQP) algorithm [11] for numerical optimization. The current waveform fits well and average error is only 2.4% of peak current consumption. We also found that modeling accuracy is not sensitive to the initial values of numerical optimization.

IV. Measurement Circuit Structure

The objective of test chip design is to make possible measurements that can be used as a reference for circuit simulation results. We designed a test circuit that can control power-supply noise flexibly and measure gate delay variation caused by power-supply noise.

The left-hand side of Fig. 7 is a micrograph of the fabricated test chip. The locations of the components, such as phase-locded loop (PLL), NANDUNIT area, and shift registers are indicated in this micrograph. DC transistor TEGs are placed in the area in the upper right. Measured *I–V* characteristics are considered in circuit simulation. Test chip was fabricated in STARC 90-nm six metal layer CMOS technology. The supply voltage of this process is 1.0 V.

The right-hand side of Fig. 7 roughly illustrates the layout of the test circuitry, which consists of a phase-locked loop (PLL), shift registers, grid power lines, ring oscillators, and NANDUNIT circuits. 1000×1500 μm area is divided into 20×20 areas by the power grid. The horizontal lines of the grid are 2.5 μm width, 50-μm pitch, and 0.9-μm thickness, and vertical lines are 7.5-μm width, 75-μm pitch, and 0.3-μm thickness. We represent the location of grids as (x, y) in this brief; $0 \leq x \leq 19$, $0 \leq y \leq 19$, leftmost rectangles are $x = 0$, uppermost rectangles are $y = 0$, as indexed in Fig. 7.

NANDUNIT circuits, which are twelve-stage two-input NAND chains are regularly and densely spaced in every grid, and their operation causes power-supply noise. 17×4 NANDUNIT circuits are located in each grid. 75% of a 1000×1500 μm area is occupied by NANDUNIT circuits.

The PLL can generate a clock signal from 100 MHz–1 GHz, which is delivered to NANDUNIT circuits with H-tree clock lines. Controlling PLL can change the noise frequency. Fig. 6

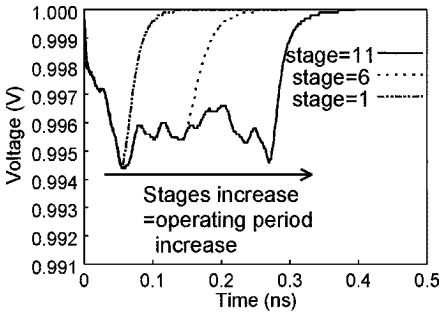

Fig. 6. Power line noise waveform. Number of active gate stages changes.

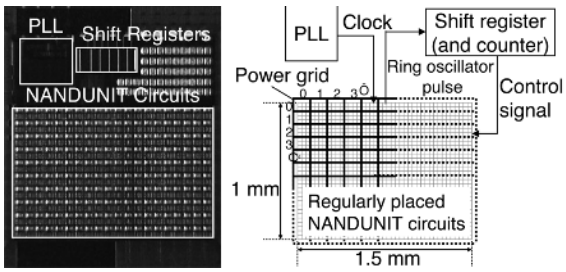

Fig. 7. Micrograph of fabricated test chip.

shows simulated supply noise waveforms of 68 NANDUNITs in a single grid area with resistive power lines. The number of active gate stages can be changed using "en2"–"en4" signals, i.e., operating time of the noise source is variable (Fig. 6), and noise waveform can be changed in time. The operating ratio is defined as the ratio of active NANDUNITs with "en1 $=$ 1". A control logic circuit is implemented so that the ratio can be selected from 100%, 50%, 25%, 0% for each 4×4 grid, aiming to control noise amplitude.

NANDUNIT and PLL control signals are stored in the shift register. The counters are included in the shift register and operate both as the shift register and as the counter. Values of the shift register and counters are serially set/read externally.

To measure the variation in delay caused by power-supply noise, 100 ring oscillators are uniformly placed at the center of $(2n+1, 2m+1)$ grids $(0 \leq n \leq 9, 0 \leq m \leq 9)$. Power/ground lines are shared by ring oscillators and NANDUNITs, and the generated power and ground fluctuations influence the ring oscillator cycle. The counters counts the time cycle of the ring oscillators. The test chip packaged in a quad flat package (QFP) is mounted on a printed circuit board (PCB). All external input and output signals are digital. Measurement is performed with a pattern generator and logic analyzer. External signal includes input, output, clock of shift registers and several control signals.

V. Measurement Results and Discussion

A. Simulation Setup

In our circuit simulation setup, NANDUNIT circuits are replaced by the variable switch model, which enabled us the full-chip simulation. The power/ground wires are carefully modeled as resistance based on the layout pattern. Well junction capacitance is also attached. The inductance of package and bonding are measured and attached between ideal power/ground and chip power/ground pads.

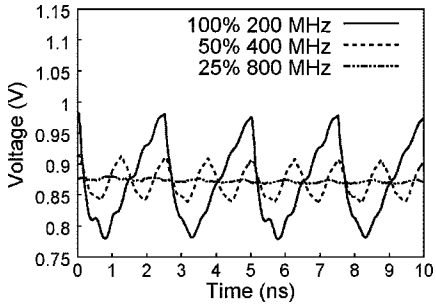

Fig. 8. Three simulation waveforms whose PLL clock frequency (megahertz) $\times$ operating ratio values are equal.

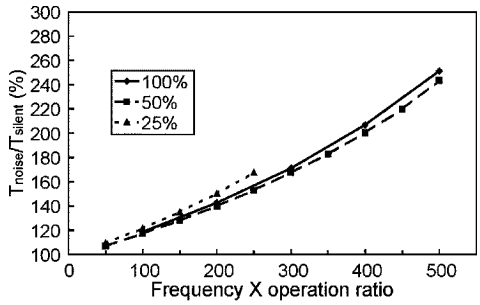

Fig. 9. Measurement results for $T_{\rm noise}/T_{\rm silent}$ at (9,9). Stage of NANDUNIT is set to 6. X-axis represents PLL clock frequency(MHz) $\times$ operating ratio.

B. Dependence of Gate Delay on Average Voltage Drop

Our measurement results demonstrate that our comments in Section II were correct: the gate-delay variation mainly depends on average supply voltage.

Fig. 8 shows the noise waveforms in our simulation. The average voltage values of the three waveforms are 0.867, 0.868, and 0.870 V with 100%, 50%, 25% activity, respectively. As can be seen, they are almost equal, even though the noise shapes are different. These waveforms are selected such that the product of PLL clock frequency and the operating ratio of NANDUNITs arrive at the same value. Roughly speaking, as long as the product is identical and the clock distribution is ignored, power consumption stays the same. This is because power consumption is proportional to frequency and the number of active gates. Hence, the averages of the supply voltage are expected to be almost the same as those shown in Fig. 8.

We evaluate $T_{\rm noise}/T_{\rm silent}$ ratio; $T_{\rm silent}$ is the ring oscillator cycle when all NANDUNITs are inactive, and $T_{\rm noise}$ is the cycle at the power-supply noise caused by NANDUNITs. The ring oscillator cycle is computed from the measured counter value. The cycle time is measured for five times and average of five values are used for discussion. The standard deviation of 200 measurement results is 0.186 ps, and the reproductivity is adequate.

Fig. 9 shows plots of $T_{\rm noise}/T_{\rm silent}$ at 100%, 50%, and 25% activity based on measurement results. The x axis is the product of frequency and activity. When the product is the same, $T_{\rm noise}/T_{\rm silent}$ values are almost the same as we expected, even though the operating conditions in frequency and activity differ and the peak voltage is estimated to be much different. $T_{\rm noise}/T_{\rm silent}$ value at 100% operating ratio agrees with that of 50% and 25%, and the average error is 4.0%. These measurement results demonstrate that the comments based on the simulation in Section II were accurate, i.e., gate delay strongly depends on average supply voltage, not on the shape of the noise waveform.

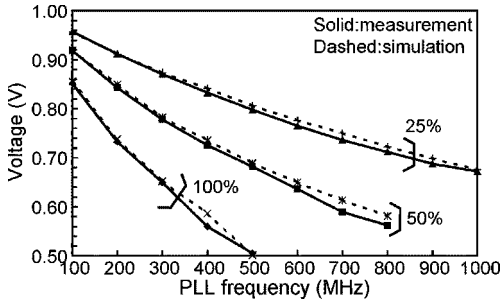

Fig. 10. Average voltage drop calculated from ring oscillator cycle in measurement and simulation results. 100%/50%/25% of NANDUNITs are uniformly activated by 100-MHz–1-GHz PLL clock.

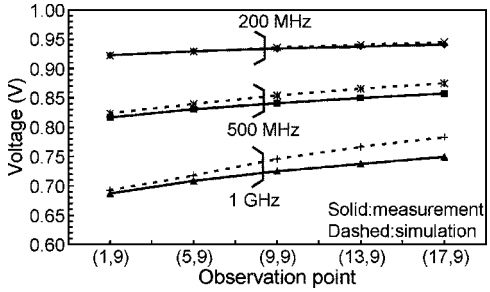

Fig. 11. Calculated voltage drop at (1,9), (5,9), (9,9), (13,9), and (17,9). NANDUNITs in $0 \leq x \leq 3$ area are activated with 200-MHz, 500-MHz 1-GHz PLL clock.

C. Accuracy of Simulation Model

This section evaluates the appropriateness of the variable switch model in Section III for power-supply noise simulation.

Here we compare the average measured voltage drop with the average simulated voltage drop. The measurement results reported in Section V-B indicate that gate delay depends on average voltage drop. This result means that the measured delay increase can be translated into average supply voltage. Oscillation cycles without noise were measured beforehand, varying the supply voltage from 1.0 to 0.5 V in 20 mV steps. These measurements were used for the translation. As for simulation results, the delay increase was first estimated by circuit simulation and then translated into average voltage. In this case, the relation between the oscillation cycle and supply voltage estimated by circuit simulation was used.

Fig. 10 shows the calculated average voltage drop at (9,9) ring oscillator based on measured and simulated results. In the results shown in Fig. 10, the output clock frequency was changed from 100 MHz to 1 GHz, and the ratio of active NANDUNITs was also varied. Simulation results correlate well with measurement results, and the average error is 0.9%. In the range over 600 MHz with 100% activity and over 900 MHz with 50% activity, the counter does not work well due to very high power-supply noise, so the results are not plotted in the figure. The good correlation between simulation and measurement results indicates that the simulation model can accurately estimate power-supply noise on a real chip.

We next evaluate spatial distribution of power-supply noise. NANDUNITs in $0 \leq x \leq 3$ are operated, and the cycles of the ring oscillators at (1,9), (5,9), (9,9), (13,9), and (17,9) are observed. Fig. 11 shows the average voltage drop values calculated from the ring oscillator cycles. The simulated voltage drop curves agree well with the measured ones at all PLL clock frequencies, and the average error is 1.4%. The agreement between simulation and measurement results implies that the spatial distribution of the power-supply noise is well reproduced by our circuit simulation.

VI. Conclusion

In this brief, based on the measured results, we demonstrated the fidelity of the full-chip circuit simulation model and the dependence of gate delay on average voltage drop.

To conduct a full-chip simulation, we developed a switching current model with capacitance and a variable resistor. This model reproduces the switching current well and reduces simulation time by 94%.

Measurement circuitry was designed to measure the delay degradation caused by power-supply noise. The test chip was fabricated in a 90-nm CMOS technology. Measurement results agreed well with simulation results, validating the simulation model. Measurement results also demonstrate that gate delay mainly depends on average voltage drop.

Acknowledgment

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