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Validation of Fast and Selective Protection Scheme for an LVDC Distribution Network

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***Abstract*--Low Voltage Direct Current (LVDC) distribution systems potentially enable more efficient power distribution and wider uptake of distributed renewables and energy storage. They do however present significant fault protection and safety challenges. To address these, the use of advanced protection techniques or significant system redesign is required. This paper reviews these protection key challenges, and presents experimental results of a prototype advanced protection scheme designed to help enable LVDC distribution networks for utility applications. The developed scheme is DC current direction-based and uses multiple intelligent electronic devices (IEDs) relays in combination with controllable solid-state circuit breakers to detect and locate DC faults. This scheme provides selective protection tripping within sub-millisecond timescales. A scaled laboratory demonstrator that emulates an LVDC distribution network is used as a test platform. It allows the characterisation of the transient behaviour for various fault conditions and locations. The developed protection algorithm is implemented in LabVIEW, and its performance against such fault conditions is tested within this environment.**

***Index Terms*-- Low Voltage Direct Current (LVDC) distribution systems, power system protection, multiple intelligent electronic devices, solid state circuit breakers**

I. Introduction

THE requirement for more flexible and efficient power systems to deliver low carbon energy and the evolutionary leap in power electronics and controls have stimulated the market for DC technologies. At transmission level, high voltage DC (HVDC) point-to-point systems have already proven their effectiveness for transferring electricity over long distances. Also, multi-terminal HVDC (MTDC) systems have been introduced as the next step for better control and sharing of renewables within different regions such as in the European "Supergrid" concept [1].

At distribution level, the rapid growth of digital loads has encouraged LVDC to be considered as an efficient solution with enhanced controllability for powering data centres, commercial buildings, street lighting, and public networks [2]-[4]. LVDC is also more suitable for connecting distributed renewables where many of these devices generate DC. More advantages of LVDC in terms of energy management, and increased power capacity are presented in detail in [2]-[4].

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However, replacing an existing part of an AC network using DC is very challenging. One of the major challenges is the lack of effective protection solutions that keep the new complex AC-DC systems safe and reliable [5][6]. DC faults are more difficult to detect and clear. Their associated arcs lack zero crossing points and are more aggressive than in AC, and thus require longer time to be cleared. In addition, the relatively small values of resistance and inductance in cables, their limited impact on DC faults, and the sensitivity of AC-DC converters to faults make the realisation of protection selectivity difficult. Such issues increase the need for fast and reliable DC protection solutions that reduce the risk and cost of operating such emerging hybrid AC-DC systems.

Therefore, this paper presents results from the experimental validation of a new protection scheme that can deliver resilient operation for an LVDC distribution network. The paper is structured as follows. Section II details the key protection and safety challenges in DC systems. Section III reviews a number of possible DC protection solutions. Section IV presents the developed DC protection scheme and evaluates its performance within an experimental hardware environment. Finally, the paper conclusions are drawn in section V.

II. DC Protection Challenges

Adding new power electronics to convert AC to DC will introduce new forms of faults with different characteristics. For example, the 2-level IGBT-based voltage source converters (VSCs) which are widely used for interfacing DC systems are defenceless against faults on the DC side. When a DC fault as shown in Fig. 1 initiates, the smoothing capacitor of the VSC will discharge, and supply a high transient current. After the capacitor is completely discharged, the antiparallel-diodes will be forward biased, and allow high steady state fault currents to be supplied from the AC grid to the fault point. This current will circulate in the converter as shown in Fig. 1 until the fault is cleared. A detailed mathematical model of a faulted LVDC network are presented in [2] [3] and [5].

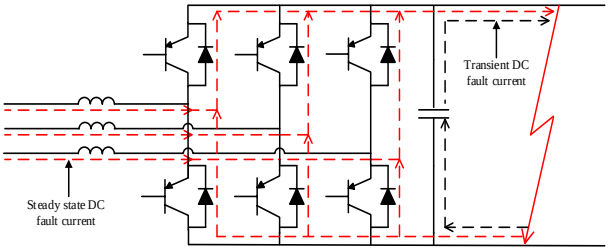

Fig. 1: The pole-to-polt DC fault response of 2-level AC-DC VSC converter

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The high transient current and uncontrolled steady state current with no natural zero crossings in addition to the limited restraint on the fault current magnitude and rise rate by the line impedances create new challenges in protecting DC systems. These challenges are discussed in details as follows.

A. The requirement for high speed DC protection

Due to the power electronics' relatively limited short circuit handling capability, DC protection systems need to isolate faults far faster than conventional protection. Their operating time has to be fast enough to: prevent a high transient and steady state DC currents from damaging equipment; prevent the main converters from losing control and tripping unnecessarily; and reduce the impact of post-fault power quality and stability issues. Previous research has shown that the fault transient current can reach up to 35 times the steady-state fault current within less than 4ms [3]. The research in [6] has also proven that when an LVDC fault was cleared after 5ms, the large subsequent transient voltage was large enough to cause power quality issues on the un-faulted feeders' loads.

B. Detecting and locating DC faults

In DC systems, the natural small DC line impedance can lead to more complexity for locating DC faults. This will lead to very fast rate of fault current change and the differentiation of faults at different locations is limited. It will be more complicated in the case of resistive faults where the fault resistance will dominate the total fault impedance, leading to increased error in the impedance estimation and selectivity. Such an issue will make coordinated overcurrent and impedance relay-based protection for locating DC faults less effective compared to AC faults [7].

C. Interrupting DC faults

DC current interruption is one of the key issues in DC protection. DC fault currents without zero crossings do not provide a natural low point to extinguish the arc, resulting in the need for larger breakers compared to equivalent AC systems. More complex techniques such as increased arc length and arc splitters are required. The use of mechanical CBs for interrupting a high DC current such as in MTDC systems with tens of GWs is impractical [7][8]. However, their use in LVDC applications with lower ratings may be more feasible. This issue is discussed further in section III.

D. Protection against DC voltage disturbances

There are two types of voltage disturbances that can be experienced in DC systems. One is the rapid DC voltage drop that can be caused by a short circuit on a DC feeder. The relatively small values of DC cable impedance will accelerate the propagation of voltage disturbances very rapidly. AC/DC converters are very sensitive to such events, and they are more likely to lose control if fast protection is unavailable.

The second type of voltage disturbance is overvoltage on the DC side. This can be caused by a line-to-earth fault on the AC side, or due to the loss of the supply neutral/earth on the DC side of a bipolar DC system. In addition, if a DC fault is not quickly cleared and higher DC fault currents flow, large post-fault voltage spikes can be anticipated due to the release of substantial stored energy in the line inductance [6]. In such case, voltage surge protection or fast protection that reduces the fault duration and magnitude is desired.

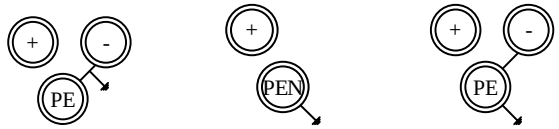
E. Safety implications

In general, the risk of fire and materials degradation in DC is larger than in AC due to the aggression of DC arcs [9]. Also, protection against indirect contact under DC fault conditions can be an issue in LVDC installations. Residual current devices (RCDs) that are normally used in AC to limit fault currents to safe levels and interrupt them within a non-dangerous period are not yet standardised and not commercially available for DC [9].

The DC safety issue can also have a significant impact on the selection of the optimal DC operating voltage, and the configuration of DC earthing systems. In 2-wire DC systems as shown in Fig. 2, it is recommended to earth the negative pole instead of the positive pole. According to the IEC 60479-1 [10], the threshold of ventricular fibrillation for "an upward" DC current caused by an earthed positive pole is half of "a downward" DC current that can be caused by an earthed negative pole. In terms of the safe operating voltage, the IEC has reached the following conclusions [11]:

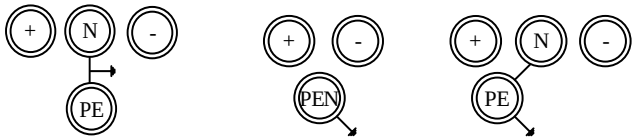
- In the case of direct contact with an energised DC pole for 2-wire LVDC systems (unipolar) as shown in Fig. 2, only DC voltages up to 200V can provide a comparable safety margin as for 250Vac as recommended by the IEC 60479 [10].
- 3-wire LVDC systems (bipolar) as shown in Fig. 3 can have lower touch voltages, and up to 400Vdc pole to pole with a grounded middle point can be used, and provide safety margins close to the 250V in AC.

On the other hand, the use of Extra LVDC (ELVDC) (i.e. <120Vdc) will reduce the risk of electric shock, and make electrical systems in buildings safer than the AC installations. In normal and dry conditions DC systems with voltages up to 60V do not require basic protection if the system is separated from the mains LV by isolation transformer such as in safety (separated) extra-low-voltage (SELV) and in protected extra-low voltage (PELV) systems [10]. In addition, most domestic DC electronic devices run on an ELVDC, and this could encourage the use of Power over Ethernet (PoE) cables to deliver low power and data in one wire for such devices, resulting in a safer environment similar to IT networks.



TN-S DC system TN-C DC system TN-C-S DC system

Fig. 2: Possible earthing systems for a 2-wire LVDC installation



TN-S DC system TN-C DC system TN-C-S DC system

Fig. 3: Possible earthing systems for a 3-wire LVDC installation

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III. Solutions Toward DC Protection

This section investigates a number of protection schemes as well as hardware solutions that have been proposed and developed by different researchers for various DC systems.

A. Protecting DC systems from the AC side

Protecting DC systems using AC side CBs has been used as a simple approach to protect point-to-point HVDC links. Such an approach cannot be applied to MTDC or LVDC systems where the selectivity is required as any single DC fault can lead to the disconnection of the entire network.

A "handshaking" method for protecting an MTDC grid from the AC side is presented in [12]. The technique is based on a combination of AC CBs and fast DC mechanical switches. The detection of DC faults is based on current directions and magnitude. When a DC fault occurs, the MTDC grid will be disconnected by the AC CBs, and the faulted DC line will be isolated during the dead time by the mechanical switches. The MTDC grid is then re-energised by reclosing the AC CBs. Drawbacks of such as scheme include the time taken to operate the AC side protection and reconfigure the DC system. This can cause a supply interruption and also continue to leave converters exposed to large DC transient fault currents.

B. Hardware for interrupting DC fault currents

1) DC Mechanical breaker

Unlike HVDC with its high ratings, the use of mechanical CBs in LVDC is more feasible. There are three main breakers that do not require zero crossing points and can be used in LVDC [13]. The first type is AC Moulded Case CBs (MCCBs) and Miniature CBs (MCBs). These CBs can be used for DC if their ratings (the magnetic trip unit protecting against instantaneous fault current) are adjusted for DC use. The second type is DC CBs that are equipped with permanent magnetic on "the internal arcing chambers" in order to break DC arcs with voltages up to 440Vdc. The third type is a DC mechanical CB equipped with electronic trip units. These units contain a set of curves to control the CB trip characteristics.

The aforementioned CBs have normally lower DC current and voltage ratings compared to equivalent AC due to the higher risk of fire. For higher ratings, multiple poles may be required, resulting in increased size and cost. These CBs normally take longer time to clear DC faults compared to their performance for AC faults. These operating speeds can restrict their use within LVDC systems where very fast protection operation is required.

2) DC solid state breakers

For fast DC protection, solid state circuit breakers (SSCBs) become attractive. Such devices can operate 900 times faster than mechanical breakers [14]. The common examples of SSCBs are: normally-on Silicon Carbide Junction Field Effect Transistor (SiC JFET), Integrated Gate-Commutated Thyristors (IGCT), and Isolated Gate Bipolar Transistors (IGBT). The main issue with SSCBs is the on-state losses, which can be considerable in HVDC systems and in the range of 30% of the VSC station [8]. This makes SSCBs more applicable to LVDC systems with lower ratings, especially if silicon carbide (SiC) technologies that offer reduced losses, size and better operational lifespan are used.

3) DC hybrid breakers

To reduce SSCB on-state losses, a hybrid DC breaker has recently been introduced [8]. This breaker has two parallel paths: the main path carries the current during normal operation, and has a reduced number of electronic switches in series with a low loss mechanical switch; and the bypass path contains a number of electronic switches for rapid interruption of DC faults. The operational sequences of such breakers is given in [8], and it has already been prototyped for 320kVdc systems with operating time <5ms. In relation to LVDC applications, hybrid DCCBs are not widely used compare to mechanical and SSCBs due to their immaturity [15].

C. Blocking DC faults using different converter topologies

DC/DC converters which interface two DC systems with different voltages have been recently proposed to control DC faults [16]. The full bridge DC/DC chopper presented in [17] has the capability of fully interrupting DC currents. The other type is the full-bridge Modular Multi-level Converters (MMCs) which can control the fault current to zero by controlling its real component, and simultaneously acting as a STATCOM in supporting grid voltages by controlling the reactive current component [7]. MMC is still a hot area of research in HVDC systems, but not widely proposed for LVDC applications. While DC/DC converters are important components in LVDC systems, their protection functionality still needs to be coordinated with any existing downstream protection for good selectivity levels.

D. Detecting and locating DC faults

1) Overcurrent based protection

In general, existing AC distribution systems are protected using traditional overcurrent non-unit protection. Given the challenges which exist for DC systems, such techniques need to be improved for DC. For example, the research in [18] has proposed an overcurrent relay equipped with a passive circuit consists of an inductor and capacitor in parallel. The relay detects overcurrent DC faults using overcurrent function. Whilst, the LC circuit generates a specific frequency under DC fault conditions which can be captured by a discrete wavelet transform (DWT) tool to detect high resistive faults. This relay operates locally, but no coordination with other protection devices for adequate selectivity was considered.

DC overcurrent can also be controlled to low value or zero using converters with fault management capability. A boost converter is used in [19] and added after an uncontrolled rectifier to reduce the fault current to low rated values which can be cleared by low rated contactors. Another approach based on a coordinated control scheme of mechanical switches and converters to protect a ring DC bus system is presented in [20]. This approach eliminates the use of DCCBs by reducing the fault current to zero using the converter to de-

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energise the bus, and the switches to reconfigure the bus during the dead time. Both of these solutions are applicable only with fully controllable converters. Inclusion of these non-conventional converters may add to the cost and complexity of the network design.

2) Rate of current change-based protection

The measurement of rate of change of DC current can be used to detect DC faults at an early stage. The technique is used in [21] and analysed by a central processing unit to protect a ring DC bus. The current magnitudes received from each zone through communication links are derived, and the highest current change indicates the location of the fault.

For compact LVDC systems, the fault current rate will both be large and very sensitive to line and fault impedances. Therefore whilst it is straight forward to detect a fault has occurred, the location of this fault for effective protection selectivity is extremely challenging [22].

3) Using differential protection

Given the challenges for using typical non-unit overcurrent protection for fault discrimination in DC systems, differential protection has been proposed as an alternative solution [7]. The research in [23] has proposed the use of differential protection for an LVDC compact system. It uses a central microcontroller which converts all the analogue measurements to digital and uses them for detection and locating the DC faults. This will also overcome the time synchronisation issue between the measurements.

4) Using signal processing techniques-based protection

Travelling waves and Active Impedance Estimation (AIE) methods have been proposed for locating DC faults. One example of using such techniques is the Electromagnetic Time Reversal (EMTR) as presented in [24], and proposed for locating faults in MTDC systems. The method is based on recording DC fault transients at an observation point in a finite time period. The recorded signals are reversed and injected back from the observation point into the system. The signals' energy is then calculated and the point with the highest energy indicates the fault location. The approach requires a high sampling frequency and significant data processing equipment for performing fast computation.

The AIE technique as presented in [25] is developed for locating DC faults in DC marine systems. This approach is based on the estimation of harmonic impedance using a short current pulse injection. The transient pulse is injected when a fault is detected from a dip in the DC voltage. The method measures the voltages and currents before and after the injection. The time domain transient values are then transformed into the frequency domain where the harmonic impedance is determined, and used for identifying the faulted part. This technique may be useful for detecting DC faults with high impedance in an LVDC network. However additional injection units will be required to perform the AIE.

It can be concluded from the above discussion that there are different DC protection techniques that can be used for different applications and with different operating timescales. However, the solutions for fast and resilient protection for an LVDC public distribution network application (shown as single line diagram in Fig. 5a) are still very limited, where safety, reliability, and selectivity are significantly important. Resilient last mile LVDC operation will require the detection and interruption of DC faults with a good level of selectivity within < 4ms [3]. Such timescale will ensure the protection of the system against high transient currents and the circulation of steady state fault currents in the converters. It also addresses the post-fault power quality and safety issues. Such sub-millisecond protection is not possible to achieve without using advanced methods and technologies as presented next.

IV. Fast Acting and Selective LVDC Protection Scheme

This section presents an advanced DC protection scheme which can detect, locate, and interrupt DC faults on an active LVDC distribution network within <1ms. The scheme is based on sensing DC current directions at an early stage of the fault development. These directions are then converted to digital signals which are exchanged between coordinated relays for locating the fault and providing selective protection actions. The use of DC current directions eliminates the time synchronisation issues (for accurately comparing two remote values as in differential protection), and the issues associated with limited and low DC fault current magnitudes and their impact on overcurrent protection operation. The developed scheme presented in this section is a revised version of the concept proposed in [2]. In the concept in [2], the point of common coupling (PCC) and the main AC-DC converter were protected by a CB on the AC side. The AC CB is controlled by a relay on the DC side of the converter to clear the fault at the first zero crossing point. In this paper, the concept has been improved by adding protection on the DC side of the main converter as shown in Fig. 5a to operate immediately and improve the protection speed from 13.2ms to <1ms for faults on the PCC. In this paper, the developed scheme is also experimentally validated against physical DC faults using a reduced scale experiment.

A. Scheme description

The proposed protection takes advantage of the local measurements and communications expected in future smart grids. Its main elements are:

- Multiple Intelligent Electronic Devices (IEDs) that can have self-monitoring, control and communication functions are used as relays for detecting DC faults and providing the required protection decisions.
- Communication links are proposed between the IEDs to enable their coordination and the exchange of signals that are used for quickly locating and tripping the faulted circuits.
- SSCBs are used to provide fast current interruptions. The aim is to clear DC faults at an early stage during their transient phase, and reduce the duration of the fault currents circulating in the converters.

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The developed protection algorithm and functionality are given in Fig. 4, and its principles are explained as follows:

1) Measured parameters and fault detection

The parameters that are monitored by the scheme sensors are: DC current magnitudes and directions, and the DC voltages. Rapid changes in the currents and voltage magnitudes are used for sensing DC faults. When the measured magnitudes pass the thresholds, the fault location based on current directions will be quickly identified. DC voltage changes can also be used for detecting disturbances due to an earth fault on the AC side or due to the loss of neutral link in 3-wire DC systems (this functionality is out of the scope of this paper).

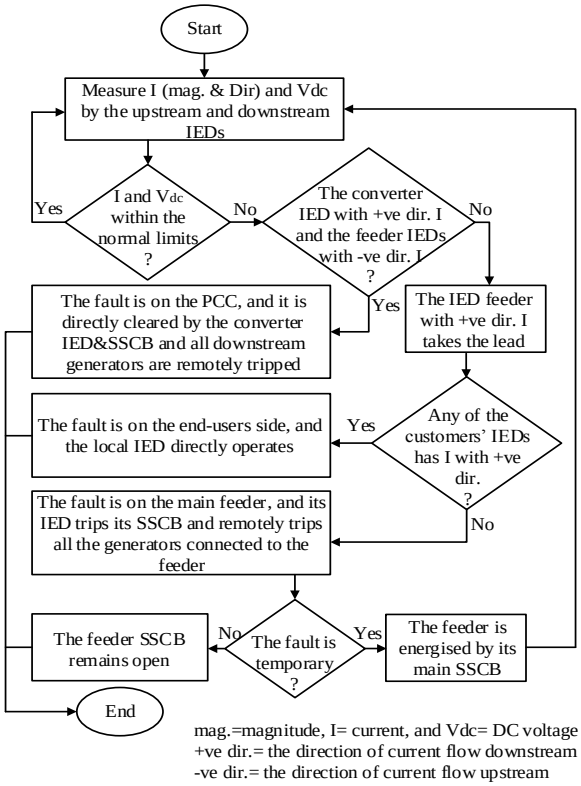

Fig. 4: The algorithm of the developed DC multifunction protection scheme

2) DC Fault location

When an IED detects a fault, the directions of the currents that flow towards the fault point are used for establishing fault location. It is defined that the direction of the current flow downstream as shown in Fig. 5a is positive, and the direction upstream is negative. The positive and negative directions are then converted to digital signals "1" and "0" respectively. The IED on the converter side (shown as an IED1 in Fig. 5b, the experimental test setup utilised and detailed in the latter sections) is set to act as a master relay. It compares its digital current direction signals to the received signals from the main feeder IEDs (shown as IED2 and IED3 in Fig. 5b). If the IED1 signal is "1" and all the received signals from the feeders IEDs are "0", the fault is located on the PCC. In the case of one of the feeder IEDs having a direction signal "1", this IED takes the lead and compares its direction signal to the other downstream IEDs connected to the same feeder. If all the received signals from the downstream IEDs are "0", then the feeder is faulted, otherwise the fault is deemed on the end-user's side. Therefore, the IED at the end-user can be set to operate on its local direction signal only. If its current direction is "1" and the fault threshold is exceeded, then the fault should be locally cleared.

No communication delay is expected between the IEDs protecting the PCC, as these devices will be located at the same location. Communication latency is expected to be between the feeder IEDs and the remote end-users' IEDs. The digital signals representing current directions from downstream IEDs need to be sent to upstream IEDs. In general, total communication delays are normally influenced by four components: transmission delay, queuing delay propagation delay, and processing delay [26]. Advanced communication such as fiber optic with high bandwidth will make the transmission and queuing delays insignificant (with bandwidth 100-1000Mbps the delay is around 0.1ms). Also, the distances in distribution systems are normally short. This will lead to small propagation delay (for 1-5miles the delays are 8.2μs-41μs) [27]. The processing delay is only the concern, and it can be minimised using advanced routing (e.g. for 64bytes Packet size with 1.5Mbpa link size is 0.35ms, and with 100Mbps link size the delay can be <5μs) [27]. Hence, such delays will be small enough to enable the developed protection scheme to operate within timescale <1ms.

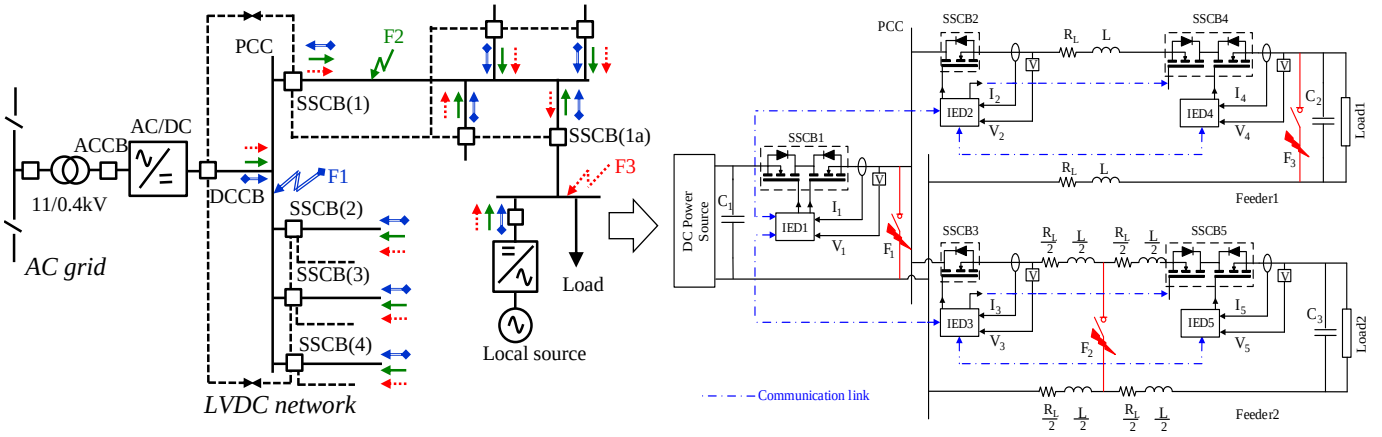

Fig. 5: (a) An LVDC radial last mile distribution network (b) LVDC experiment circuit schematic

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3) Protection actions and selective tripping

Fig. 5 is used to explain the protection actions by different IEDs for different fault locations. For a fault on the PCC (shown as F1 in Fig. 5b), two actions are performed. The converter IED (represented as IED1) trips its associated SSCB1, and the IED2 and IED3 of the feeders block the fault current contribution from the downstream generators. In the case of a fault on the main feeder (shown as F2 in Fig. 5b), the IED3 will trip the associated SSCB3 at the beginning of the faulted feeder, and simultaneously tripping any active downstream source connected to the faulted feeder. Taking the advantage of an automatic reset of the SSCB, a controllable reclosing action against temporary faults can be implemented by the IED3. As for a fault on the end-user side (shown as F3 in Fig. 5b), the fault can be locally cleared when a predetermined threshold value is exceeded.

B. Validation of the protection algorithm by experiment

A scaled DC laboratory demonstrator is utilised for replicating different DC faults transients, and testing the performance of the protection algorithm against such faults. The experimental testing and results are explained as follows.

1) Description of the test platform

An LVDC distribution network as shown in Fig. 5a is simplified and imitated using the low-power test demonstrator shown in Fig. 5b. The layout of the setup is presented in Fig. 5b and Fig. 6. The main VSC and its smoothing capacitor are represented by using a DC source in parallel with a capacitor as shown in Fig. 5b. The source supplies two loads shown as load1 and load2 in Fig. 5b via two DC branches. Each branch is built with resistance in series with inductance, and each load is connected in parallel with a capacitor shown as C_2 and C_3 in Fig. 5b. The capacitors are used to stabilise the voltage at the load side and supply transient fault currents that will help in the fault detection process. This is a valid representation for the transient current which the scheme is targeting.

DC currents and voltages are measured using hall-effect sensors, and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are used as SSCBs. The MOSFETs are used because their switching capability and controls have been successfully tested in previous projects [23]. The MOSFET switches (used as CBs) on the load side are configured as bidirectional for blocking the current from two directions and on the main feeder as unidirectional (as no need for having two bidirectional switches in the same path, see Fig. 5b). The parameters of the test rig are given in TABLE I.

The protection algorithm given in Fig. 4 is implemented in LabVIEW, and Fig. 7 shows the control circuit model of one of the main feeder's IEDs (shown as IED2in Fig. 5b). The measurement sensors are interfaced to the IED controllers which are emulated on a National Instrument (NI) CRIO-based FPGA. The measured current directions are converted to binary signals and used by the Fault Location Circuit (FLC) as given in Fig. 7 to identify the fault locations. The FLC drives the Tripping and Blocking Circuit (TBC) (shown in Fig. 7) to send the trip signals to the related SSCB through the FPGA.

2) Experimental testing and results

The first testing phase has characterised the natural transient responses of a number of DC faults at different locations. The test circuit shown in Fig. 5b is energised at low voltage equal to 20Vdc. This voltage is enough to test the protection coordination of the developed algorithm, and provides safer environment to conduct the tests. Three pole-pole solid faults, labelled as F_1, F_2, and F_3 in Fig. 5b are applied. F1 emulates a fault on the PCC, and F2 and F3 represent faults at the middle of the DC cable and at the end-user side respectively. The results of the fault contribution converging into these three faults are presented in Fig. 8.

The second testing phase has evaluated the performance of the protection scheme during short circuit faults at F_1, F_2 , and F_3. For a typical LVDC network, the transient currents can last up to 5ms as discussed earlier in the paper. But for the low power laboratory rig, the scaled transient durations of the applied faults as shown in Fig. 8 can be as low as <1ms. Hence subsequent communication delay within the software was minimised to zero to allow the scheme to operate within the rig lower transient timescales (<1ms). This assumption during the test does not reduce the stability of the algorithm.

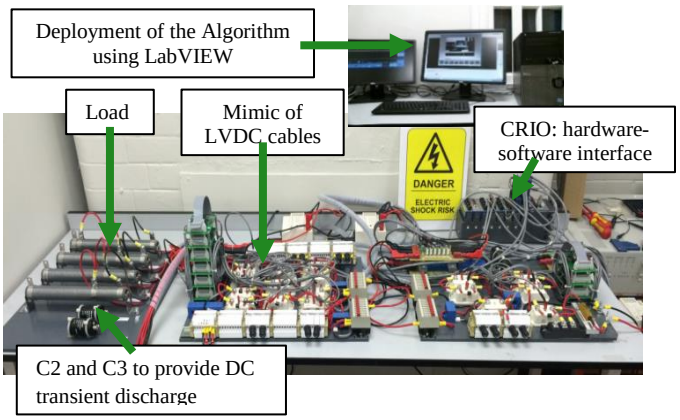

Fig. 6: Actual experiment setup on a low power LVDC circuit protected by fast acting protection scheme

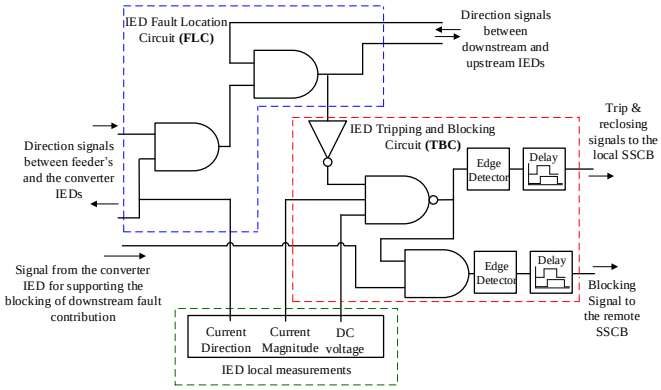

Fig. 7: The model of the IED located at the beginning of the main feeder

TABLE I. LVDC EXPERIMENT CIRCUIT PARAMETERS

V_{dc} (V)	C_1 (μF)	C_2 (μF)	C_3 (μF)	MOSFET	R_L (Ω)	L (mH)	Load (Ω)
20	4700	2200	2200	Rated 100V/200A (600A peak)	0.0042	0.0022	6

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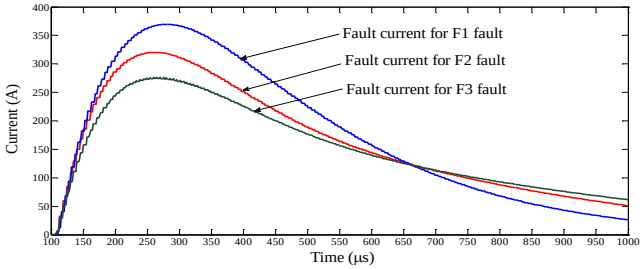

Fig. 8: Transient DC current profiles of pole-to-pole faults

The fault current thresholds for the relays were set to less than half of the applied fault currents peaks. IED1 threshold was set at 100A, IED2 and IED3 set at 90A, and IED4 and IED5 set at 60A. The tests against F_1, F_2, and F_3 faults were conducted as follows.

For the fault at F_1, the fault was applied at t=0.1ms. Fig. 9 shows the results with and without protection. The IEDs converted the positive direction (i.e. the direction of the currents from the upstream source) to a digital signal "1" and the negative directions (i.e. the direction of the currents from the load side) to the digital signal "0", and successfully used these signals to identify the faulted part. When the current and voltage thresholds were exceeded as shown in Fig. 9, only the faulted part was quickly disconnected within < 100μs.

The fault F_2 was separately tested (again the fault applied at t=0.1ms). Fig. 10 shows the current and voltage profiles with and without protection actions during this fault. Base on sensing the current directions, the fault point was accurately identified by the IED3 and IED5, and the fault was completely cleared within <100μs.

As for the fault on the load side at F_3, IED4 sensed the fault current with a positive direction, and treated the fault as local. The fault was quickly cleared by the associated SSCB4 within less than 70μs as shown in Fig. 11.

The rig test results have shown that the developed protection algorithm was stable and fast to detect and interrupt a number of DC faults at different locations, and with good selectivity. The current direction-based fault detection of different DC faults achieved within <1ms. Such fast operation at low current level will deliver the following key elements:

- Reduce the fault stress on LVDC power electronics, and on insulation materials, hence avoid the use of more expensive equipment with higher current ratings
- Heighten the safety challenges associated with DC and risk of fire hazard DC by limiting fault currents and interrupt them within non-dangerous periods
- Improving the voltage profiles on adjacent feeders will improve the transient stability of LVDC local microgenerators, as these devices are very sensitive to voltage drops and have poor inherent damping [28]. Similarly improved voltage profile helps to remove the risk of undervoltage protection mal-operation.
- Improve post-faults power quality which can be caused by post-fault high transient voltages

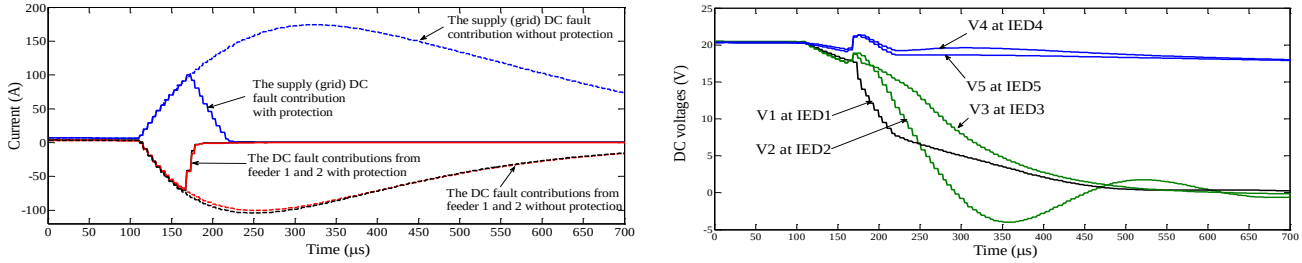

Fig. 9: The current and voltage profiles during fault F1 on the PCC

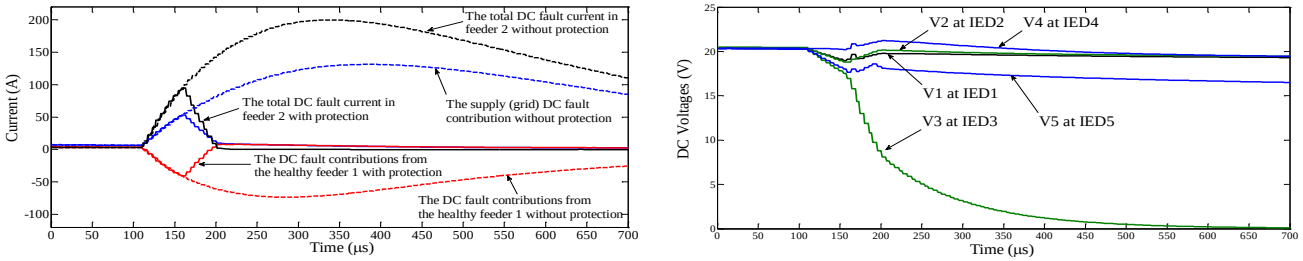

Fig. 10: The current and voltage profiles during fault F2 at the middle of the feeder

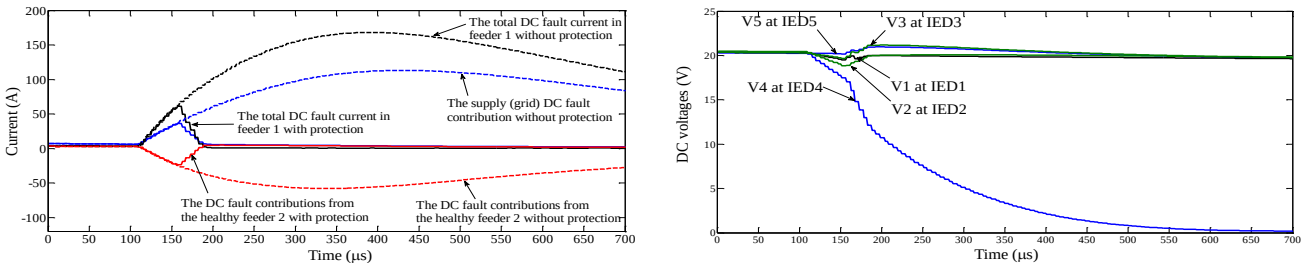

Fig. 11: The current and voltage profiles during fault F3 at the end of the feeder

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V. Conclusions

Modern LVDC distribution systems are very promising technologies for a radical improvement in the performance of LV networks. However, their applications are still at very early stage in utility sector. Effective DC protection and safety still present outstanding challenges in the public LVDC arena. The paper has broadly discussed these challenges, and presented a new fast acting DC protection solution that can address such challenges. The new solution has been experimentally validated against a number of faults within a scaled rig. The results have proven the credibility for achieving fast detection of different DC faults, and fast interruption of the faults (i.e. <1ms) at low levels with a good level of selectivity. Clearing the faults within such small timescales and at low levels as proven by the results will significantly reduce the fault let through energy, enable the use of equipment with lower ratings, reduce the risk of fire hazard which is particularly problematic in DC, and reduce the stress on the insulations materials.

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