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# Van der Waals integration of high-κ perovskite oxides and two-dimensional semiconductors

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**Two-dimensional semiconductors can be used to build next-generation electronic devices with ultrascaled channel lengths. However, semiconductors need to be integrated with high-quality dielectrics—which are challenging to deposit. Here we show that single-crystal strontium titanate—a high-κ perovskite oxide—can be integrated with two-dimensional semiconductors using van der Waals forces. Strontium titanate thin films are grown on a sacrificial layer, lifted off and then transferred onto molybdenum disulfide and tungsten diselenide to make n-type and p-type transistors, respectively. The molybdenum disulfide transistors exhibit an on/off current ratio of $10^8$ at a supply voltage of 1 V and a minimum subthreshold swing of 66 mV dec$^{-1}$. We also show that the devices can be used to create low-power complementary metal–oxide–semiconductor inverter circuits.**

Dielectric layers with a high dielectric constant (κ), minimal leakage current and reduced thickness are essential for creating low-power electronic devices and circuits. High-κ dielectrics such as hafnium oxide ($HfO_2$) have, for instance, been used in silicon electronics for over a decade[1–4]. Similar approaches to grow high-κ dielectric layers have been attempted on two-dimensional (2D) layered materials including graphene, transition metal dichalcogenides and black phosphorus[5–11]. However, unlike conventional semiconductors, the surfaces of 2D materials are free of dangling bonds and thus a seeding layer or surface functionalization is typically required to provide nucleation sites before the growth of a high-κ dielectric[12–14]. These additional treatments increase the processing complexity and degrade the interface between the dielectric and 2D material[15].

Surface oxidation of semiconducting $Bi_2O_2Se$ into $Bi_2SeO_5$—a high-κ dielectric material—can avoid such pretreatment, but this method faces challenges to become more generally applicable[16,17]. Pretreatment can also be avoided if the dielectric can be integrated on the 2D material using only van der Waals forces, instead of chemical bonding during in situ growth. Various van der Waals heterostructures have been fabricated by creating layers on another substrate and then transferring them onto a 2D material as a freestanding thin film[18,19], but using such methods with dielectrics is challenging due to the difficulties in preparing and handling freestanding high-κ dielectric thin films. Single-crystal strontium titanate, $SrTiO_3$ (STO), is a complex oxide with a high dielectric constant of over 300 at room temperature[20,21]. These properties make it attractive for exploring the emergent transport properties of 2D materials in an ultrahigh-κ dielectric environment[21,22], as well as for fabricating 2D-material-based electronic devices with scaled supply voltage. However, it is challenging to integrate STO on 2D materials, which is required for independent gate control in practical applications, due to structure mismatch and processing incompatibility common for oxide materials[23–25].

In this Article, we report high-performance n-type molybdenum disulfide ($MoS_2$) and p-type tungsten diselenide ($WSe_2$) field-effect transistors (FETs) on silicon substrates with single-crystal STO as the top-gate dielectric. The STO is epitaxially grown on a sacrificial layer and subsequently transferred with the help of van der Waals forces. The $MoS_2$ FETs exhibit an on/off current ratio ($I_{on}/I_{off}$) of over $10^8$ within the top-gate voltage ($V_{TG}$) range of ±1.0 V and a minimum subthreshold swing (SS) of 66 mV dec$^{-1}$. The $WSe_2$ FETs exhibit an on/off ratio of $10^7$ within a $V_{TG}$ value of ±1.0 V. The near-ideal SS and negligible residual doping illustrate the high quality of the STO–2D material interfaces. Double-gate and Hall-effect measurements on graphene devices yield an effective dielectric constant of 17–20, which is higher than that of $HfO_2$ ($\kappa \approx 13$–$17$)[26,27], when grown by atomic layer deposition on 2D materials. We also create a low-power complementary metal–oxide–semiconductor (CMOS) inverter that has a static power consumption of only several picowatts by combining STO-gated n-type $MoS_2$ and p-type $WSe_2$ transistors.

## Fabrication of STO–2D material heterostructures

Our integration of STO on 2D layered materials begins with the sequential pulsed laser deposition (PLD) of $Sr_3Al_2O_6$ (SAO) and STO layers on STO substrates[28–31] (Methods provides details of growth) (Fig. 1a). Next, the surface of the as-grown STO thin film was covered with a thin polydimethylsiloxane (PDMS) sheet. The stack was then floated in a deionized (DI) water bath to etch the sacrificial SAO layer and produce an STO membrane adhering to the PDMS sheets due to van der Waals forces (Supplementary Fig. 1 shows the optical images of the STO membrane on PDMS). This membrane was then deliberately ruptured and transferred onto multiple PDMS sheets by repetitive laminating and peeling the PDMS sheets to produce scattered micrometre-sized STO flakes. In this way, we could choose STO flakes with lateral sizes similar to those of mechanically exfoliated 2D materials, facilitating subsequent device fabrication. The STO flakes on PDMS were accurately aligned and brought into contact with target 2D flakes on $SiO_2$/Si substrates and being monitored under a microscope.

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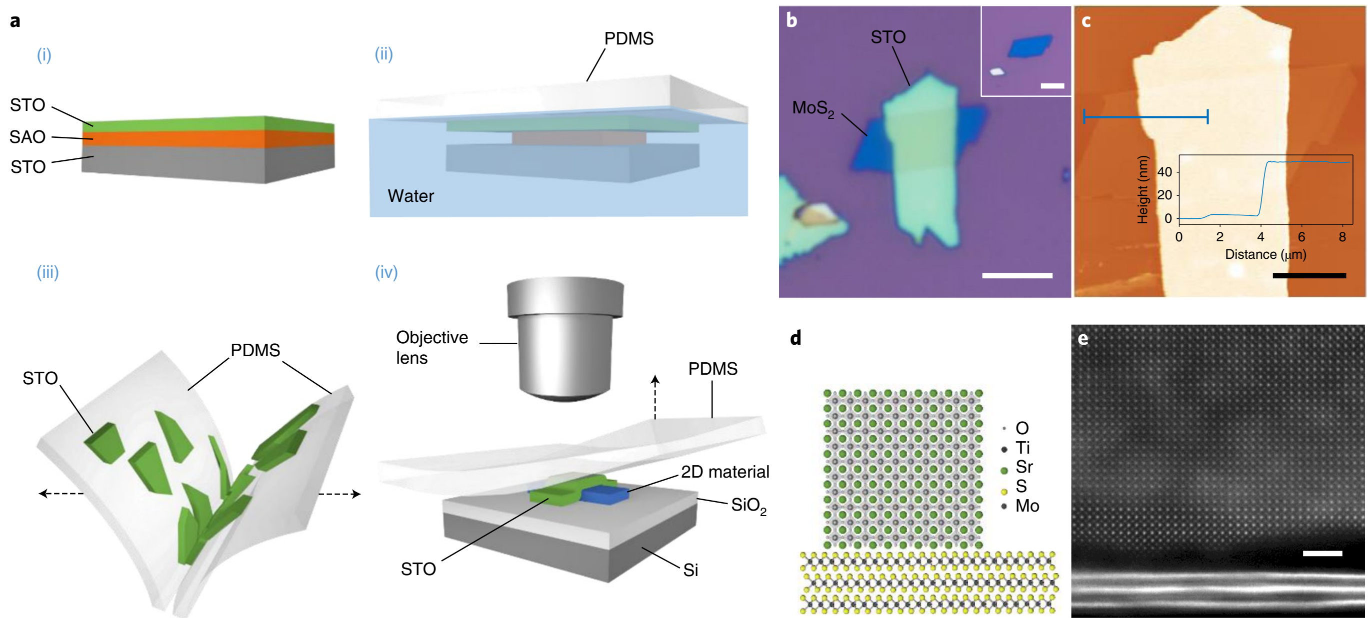


**Fig. 1 | STO–2D material heterostructures on $SiO_2$/Si. a**, Schematic of the fabrication process: (i) sequential PLD growth of SAO and STO on a bulk STO substrate; (ii) the surface of the STO thin film is covered with a PDMS sheet and the stack is then floated in a DI water bath to dissolve the sacrificial SAO layer; (iii) the PDMS sheet supporting the STO membrane is laminated with another PDMS sheet and peeled off slowly, yielding micrometre-sized STO flakes on both PDMS sheets; (iv) a micrometre-sized STO flake is aligned and laminated, under a microscope, onto a 2D material on $SiO_2$/Si. The PDMS sheet is then peeled off, leaving STO on $SiO_2$/Si. **b**, Optical image of a representative STO–$MoS_2$ heterostructure on $SiO_2$/Si. The inset displays the optical image of the original $MoS_2$ flake. Scale bars, 10 μm. **c**, AFM height image of the heterostructure shown in **b**. Scale bar, 5 μm. The inset shows the height profile along the marked line, from which the thicknesses of $MoS_2$ (3.4 nm) and STO (45.9 nm) were extracted. **d**, Schematic of three-dimensional cubic and 2D layered crystal structures of STO and $MoS_2$. **e**, Cross-sectional HAADF-STEM image of an STO–$MoS_2$ heterointerface. Scale bar, 2 nm.

Last, the PDMS was peeled off slowly, leaving the STO flakes on $SiO_2$/Si substrates because of a stronger interaction between STO and $SiO_2$ than that between STO and PDMS[32]. The freestanding STO film can be transferred, in principle, onto any 2D material, which is crucial for fabricating complex electronic circuits involving 2D materials with different electronic properties.

A representative STO–$MoS_2$ heterostructure on $SiO_2$/Si is shown in Fig. 1b. Transferring STO on $MoS_2$ did not induce noticeable contamination. The morphology of this heterostructure was further examined by atomic force microscopy (AFM) imaging (Fig. 1c). Both STO and $MoS_2$ flakes exhibited uniform thicknesses and clean surfaces. Conformal contact was formed at the heterointerface, although STO has a distinctively different crystal structure compared with $MoS_2$ (Fig. 1d). Figure 1e shows the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of an STO–$MoS_2$ interface. Individual atoms of STO arranged in a cubic lattice can be clearly identified in the STEM image and the X-ray diffraction peaks of STO film transferred on the $SiO_2$/Si substrate can be clearly identified (Supplementary Fig. 1). Both these results confirm the excellent crystallinity of STO even after transfer. The intact layered structure of $MoS_2$ demonstrates that the van der Waals integration process is non-invasive to the underlying 2D materials.

## Dielectric properties of transferred STO

The quantitative evaluation of the effective dielectric constant of transferred STO flakes, which includes contributions from the van der Waals gap and interfacial impurities, is not currently available experimentally. Therefore, to ensure the accuracy of the extracted value, we employed two methods: double-gate[33] and Hall-effect[34] measurements. Figure 2a shows a graphene Hall bar device on a p-Si substrate with a 285 nm $SiO_2$ capping layer. $SiO_2$ and STO act as the bottom- and top-gate dielectric layers, respectively. The graphene sheet was patterned by electron-beam lithography and etched into a Hall bar using oxygen plasma before being covered with STO (Supplementary Fig. 2). The thicknesses of STO (44.2 nm) and graphene (double layer) were determined by AFM and Raman spectroscopy, respectively (Supplementary Fig. 3). The charge carrier concentration in graphene can be simultaneously modulated by the top and bottom gates. As a result, the top-gate transfer curves shift with a varying back-gate voltage ($V_{BG}$) (Fig. 2b). The slope of the top-gate Dirac point voltage ($V_{DIRAC,TG}$), which marks charge neutrality, versus $V_{BG}$ is equal to the ratio of the bottom-gate to top-gate capacitance ($C_{SiO_2}/C_{STO}$), if the parallel-plate capacitor model is assumed for both top and bottom gates[27,33]. Substituting the fitted value (0.03) in Fig. 2c into

$$\frac{C_{SiO_2}}{C_{STO}} = \frac{\varepsilon_{SiO_2} t_{STO}}{\varepsilon_{STO} t_{SiO_2}}, \quad (1)$$

where $\varepsilon_{STO}$ and $\varepsilon_{SiO_2}$ (3.9) are the dielectric constants of STO and $SiO_2$, respectively, and $t_{STO}$ and $t_{SiO_2}$ are the thicknesses of STO and $SiO_2$, respectively, we derived $\varepsilon_{STO}$ of 20.2 from this device, which corresponds to a capacitance of 0.4 μF cm$^{-2}$.

Carrier concentrations, from which the dielectric constant of STO can also be derived, were directly extracted by Hall-effect measurements. Figure 2d shows that the Hall resistance ($R_{xy}$) linearly depends on the magnetic field ($B$) at different $V_{TG}$ values. The $R_{xy}$–$B$ slope is equal to $1/(en_{2D})$ or $1/(ep_{2D})$ depending on the carrier type, where $e$, $n_{2D}$ and $p_{2D}$ are the elementary charge, electron concentration and hole concentration, respectively. At $V_{TG}$ away from the Dirac point, one type of carrier dominates in graphene and their concentration changes linearly with $V_{TG}$ (ref. [35]). From the linear fit of $p_{2D}$–$V_{TG}$ (Fig. 2e), the top-gate capacitance $C_{STO}$ is calculated to be 0.34 μF cm$^{-2}$ according to $dp_{2D}/dV_{TG} = C_{STO}/e$. The accuracy of the Hall-effect measurements was further verified by its application in

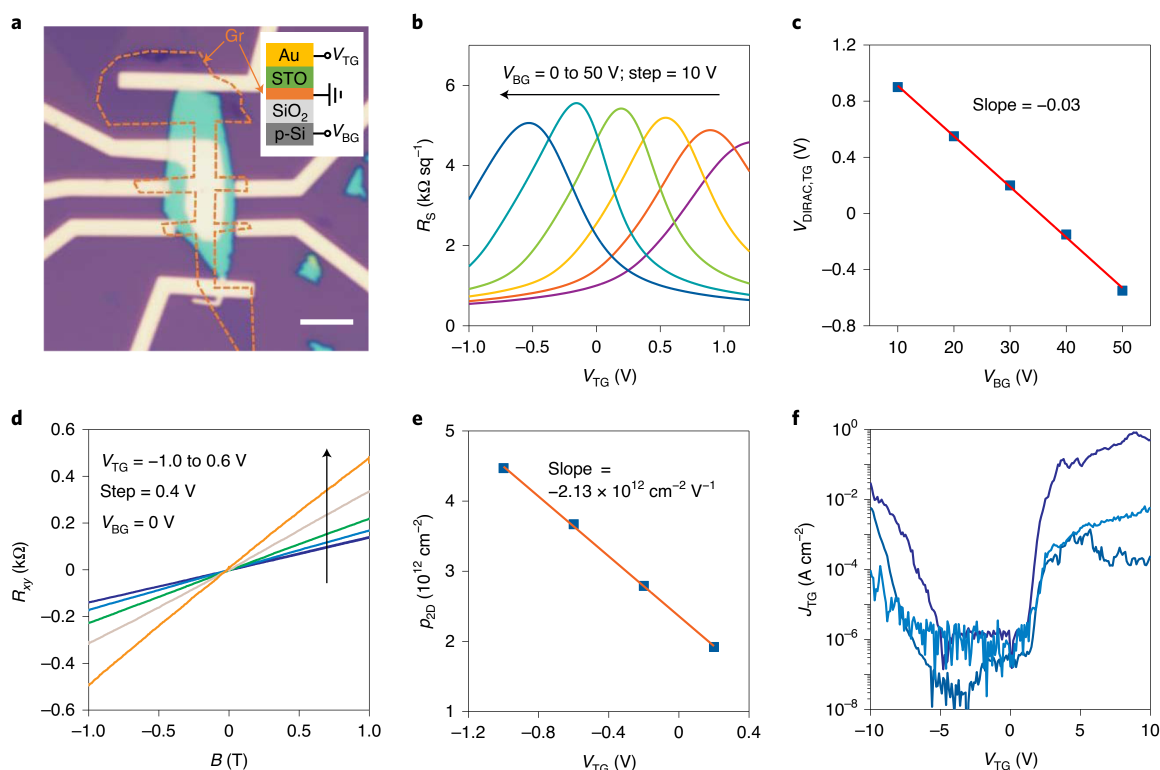


**Fig. 2 | Dielectric constant and strength of STO top-gate dielectrics.** **a**, Optical image of a graphene Hall bar device with STO top-gate dielectrics. The boundary of the double-layer graphene is indicated by the dashed line. Scale bar, 10 µm. The inset illustrates the device geometry. **b**, Sheet resistance ($R_S$) of graphene (Gr) as a function of top-gate voltages ($V_{TG}$) at different back-gate voltages ($V_{BG}$). **c**, $V_{BG}$-dependent top-gate Dirac voltages ($V_{DIRAC,TG}$). The linear fitting, represented by the solid line, yields a slope of −0.03. **d**, Hall resistance ($R_{xy}$) as a function of magnetic field ($B$) at different $V_{TG}$ values. **e**, Hole concentration ($p_{2D}$) versus $V_{TG}$, extracted from the linear fitting of $R_{xy}$–$B$ relations in **d**. The solid line indicates the linear fitting of $p_{2D}$–$V_{TG}$. **f**, Leakage current density ($J_{TG}$) versus $V_{TG}$ of three representative devices.

back gating. They yield $\varepsilon_{SiO_2}$ of 4.0 (Supplementary Fig. 4), which matches the theoretical value of $SiO_2$ (3.9–4.0). It is worth noting that the extracted $\varepsilon_{STO}$ from double-gate (20.2) and Hall-effect (17.2) measurements includes contributions from polymethyl methacrylate (PMMA) residues between STO and graphene, which reduce the effective capacitance and dielectric constant. Nonetheless, these values are already greater than that of atomic-layer-deposited $HfO_2$ on 2D materials, demonstrating the feasibility of using STO for practical devices[27].

The dielectric strength of STO was also investigated. Leakage currents through Au–STO–graphene stacks ($J_{TG}$) display similar attributes (Fig. 2f). The leakage current is very small and below the detection limit of our measurement setup (~$10^{-13}$ A) when $V_{TG}$ is within the range of roughly −4 to 2 V. Beyond this range, $J_{TG}$ increases rapidly but no catastrophic failure is observed within ±10 V, which corresponds to a nominal electric field of around 2.5 MV cm$^{-1}$. These results prove the electrical robustness of the transferred STO. In addition, the forward-biased $J_{TG}$ is substantially larger than the reverse-biased $J_{TG}$, which can be explained by the band alignment of the heterostructures (Supplementary Fig. 5). STO is an insulator with a bandgap of 3.3 eV (ref. [36]), and the Fermi level of graphene, which can be tuned by $V_{TG}$, aligns closer to the conduction band edge of STO. As a result, electrons (holes) can be injected into STO at a large positive (negative) $V_{TG}$, and electron injection starts at a smaller bias. Such leakage behaviour does not deter the operation of 2D transistors because the large dielectric constant of STO, compared with more commonly used dielectric materials for 2D electronics such as hexagonal boron nitride (hBN), $Al_2O_3$ and $HfO_2$ (Supplementary Table 1), provides sufficient electrostatic modulation to 2D semiconductors at small gate voltages, as demonstrated in the following sections.

## $MoS_2$ transistors with STO top-gate dielectrics

As the most studied 2D semiconductor for field-effect transistors, few-layer (FL) $MoS_2$ was selected to prove the feasibility of STO as the dielectric layer in high-performance transistors. To fully explore the potential of STO-gated $MoS_2$ transistors, we employed FL graphene as the drain/source electrodes for the following reasons. First, its gate-tuneable Fermi level facilitates barrier-free injection of charge carriers into 2D semiconductors[37,38]. Second, its atomically flat and ultrathin nature allows the fabrication of multilayer van der Waals heterostructures with clean and flat interfaces[39–41]. Third, the mechanical flexibility and optical transparency of graphene are desirable for potential flexible and transparent electronics based on 2D semiconductors[42]. To fabricate graphene-contacted $MoS_2$ transistors, we sequentially transferred graphene, $MoS_2$ and STO on $SiO_2$/Si substrates (Supplementary Fig. 6). The device structure is sketched in Fig. 3a. The channel length and width of the fabricated device based on an FL $MoS_2$ flake and 38.1 nm STO (Fig. 3b, inset) are 5.4 µm and 4.8 µm, respectively. The graphene electrodes are beneath $MoS_2$ and overlap with the top gate so that the whole $MoS_2$ channel as well as the graphene–$MoS_2$ contact regions are simultaneously modulated by the top gate. Thus, the transistor is effectively turned on and off by applying $V_{TG}$ within the range of ±1 V. As shown in Fig. 3c and Supplementary Fig. 7, the output curves are linear when $V_{DS}$ is small, indicating ohmic contacts. When $V_{DS}$ further increases, $I_{DS}$ gradually saturates, signalling pinch-off of the $MoS_2$ channel at larger $V_{DS}$. The transfer curves in Fig. 3b, measured

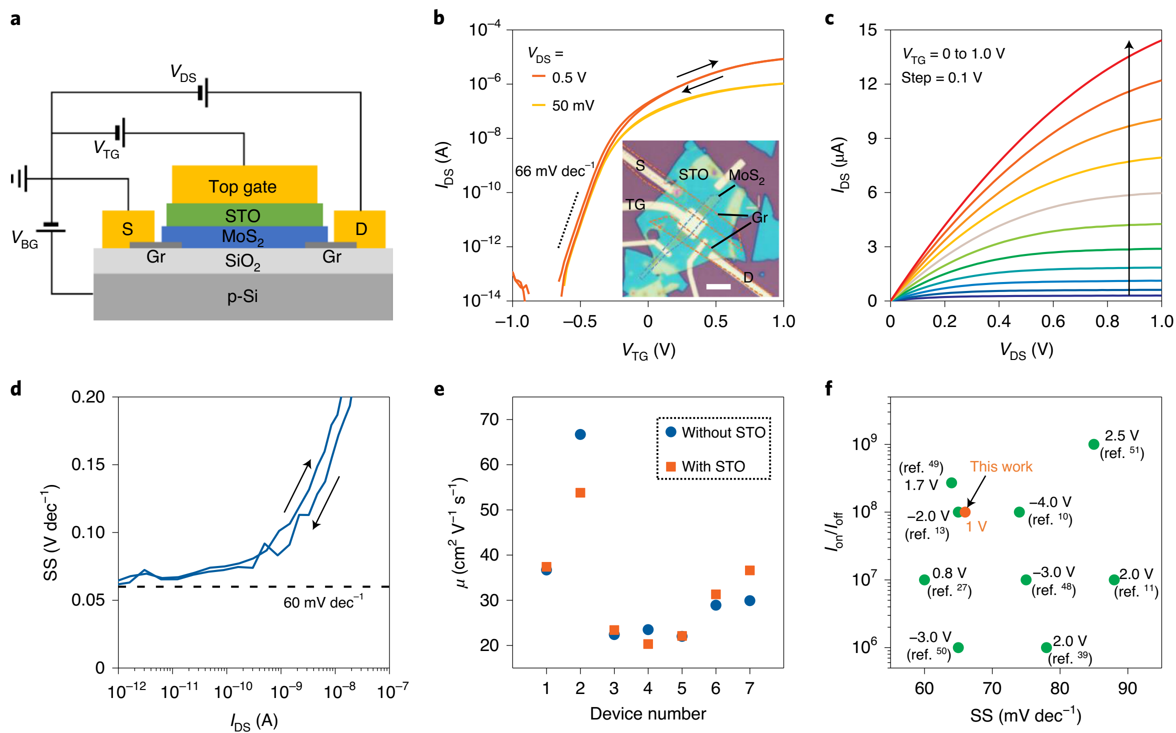


**Fig. 3 | High-performance Gr-contacted $MoS_2$ transistors with STO top-gate dielectrics. a**, Schematic of the double-gated transistor together with the electrical measurement configuration. S, source; D, drain. **b**, Double-sweep $I_{DS}$–$V_{TG}$ characteristics of the device with the back gate grounded. The gate sweeping directions are indicated by the arrows. The inset shows the optical image of the device. The boundaries of graphene and $MoS_2$ are outlined by dashed lines. Scale bar, 10 μm. **c**, Output curves ($I_{DS}$–$V_{DS}$) with $V_{TG}$ varying from 0 to 1.0 V at steps of 0.1 V. **d**, Subthreshold swing (SS) as a function of $I_{DS}$. **e**, Mobility ($\mu$) of $MoS_2$ measured by four-probe (device numbers 1–4) and two-probe (device numbers 5–7) method before and after the deposition of STO. **f**, A comparison of the current on/off ratio ($I_{on}/I_{off}$) and SS of our transistor with state-of-the-art $MoS_2$ transistors with hBN or high-$\kappa$ dielectrics in the literature[10,11,13,27,39,48–51]. The required gate voltages for the corresponding $I_{on}/I_{off}$ and SS are also labelled.

with the back gate grounded ($V_{BG}=0$ V), display characteristics of a typical n-type transistor with a current on/off ratio ($I_{on}/I_{off}$) of over $10^8$ at a drain–source bias ($V_{DS}$) of 0.5 V and an SS value as small as 66 mV dec$^{-1}$, close to the thermionic limit at room temperature (60 mV dec$^{-1}$). The SS remains low for $I_{DS}$ of several orders of magnitude (Fig. 3d). Little hysteresis in the $I_{DS}$–$V_{TG}$ or SS–$I_{DS}$ curves is observed between the forward and reverse top-gate sweeping, indicating a low interfacial trap density. The reproducibility of these performance metrics was verified by the measurements of nine devices (Supplementary Table 2).

The high $I_{on}/I_{off}$ at small operation voltages of our STO-gated $MoS_2$ transistors can be attributed to the following three reasons. First, the top-gate electrode and high-$\kappa$ STO covers both $MoS_2$ channel and graphene–$MoS_2$ contacts and simultaneously exerts strong electrostatic modulation to them. Thus, the on current is not limited by the access resistance (Supplementary Fig. 8), which exists in many locally top-gated $MoS_2$ transistors[10,27]. Second, the near-ideal SS value permits turning the transistor on and off within a narrow gate-voltage span. It originates from a relatively small capacitance related to the interfacial traps compared with the dielectric capacitance of STO according to

$$SS = (\ln 10)\left(\frac{k_B T}{q}\right)\left(\frac{C_{STO}+C_{it}}{C_{STO}}\right), \quad (2)$$

where $k_B$, $T$, $q$, $C_{STO}$ and $C_{it}$ are the Boltzmann constant, absolute temperature, elementary charge, areal capacitance of STO and areal capacitance related to interfacial traps, respectively[13,43]. Third, the deposition of STO has a trivial effect on the doping level and mobility of $MoS_2$. In recent reports, it was shown that the atomic layer deposition of high-$\kappa$ dielectrics tends to exert a considerable n-doping effect on $MoS_2$ to the extent that a large negative top-gate voltage is required to turn off the transistors[13,15,44]. Such a doping effect has been frequently attributed to the unbalanced positive charges in the dielectric layer[15,45]. In contrast, the van der Waals integration of STO has a negligible doping effect on $MoS_2$, indicating little net charges in STO. This phenomenon is proved by the very similar back-gate transfer characteristics of $MoS_2$ transistors before and after the deposition of STO (Supplementary Fig. 9c). The $I_{DS}$–$V_{BG}$ curves show little horizontal shift and the transistor without and with the STO coverage is switched off at almost the same $V_{BG}$. The high-$\kappa$ dielectric environment has been proposed as a booster for the mobility of $MoS_2$ because it benefits the screening of charged impurity scattering[34,46]. However, the extra high-$\kappa$ dielectrics also bring additional scattering sources, such as trapped charges in high-$\kappa$ dielectrics and at the interfaces, which deteriorate the mobility[44,46,47]. The mobility of $MoS_2$ before and after the deposition of STO was investigated by both two- and four-probe field-effect measurements (Supplementary Fig. 9 and Supplementary Table 3). As shown in Fig. 3e, the mobility exhibits varied behaviours for the seven devices, but the change after STO deposition is generally small. The relatively unchanged mobility compared with that before covering with STO is probably due to counteraction from the previously mentioned opposed effects. Nonetheless, the retained value of mobility allowed the STO-gated $MoS_2$ transistors to exhibit sufficient on-state conductance leading to $I_{on}/I_{off}$ over $10^8$ within the $V_{TG}$ range of ±1 V.

Figure 3f shows that the performance of our $MoS_2$ transistors is competitive compared with the state-of-the-art $MoS_2$ transistors

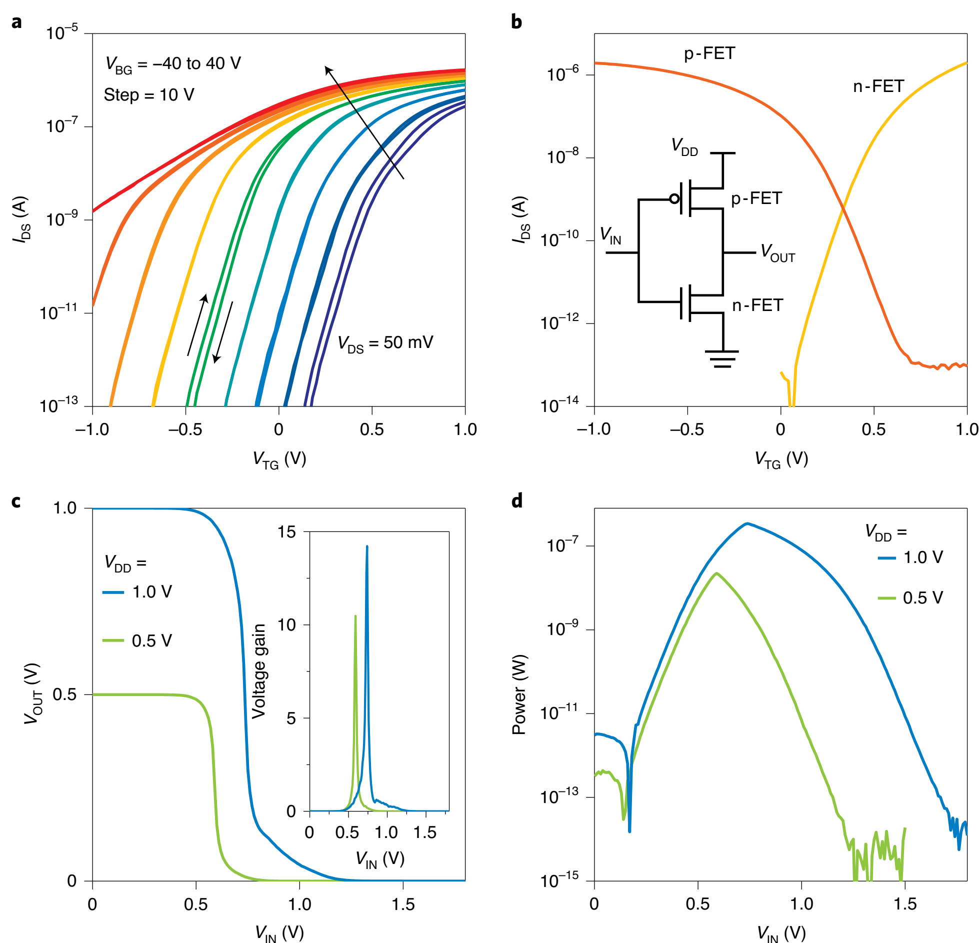


**Fig. 4 | Low-power CMOS inverter based on $WSe_2$ p-type and $MoS_2$ n-type transistors.** **a**, Transfer curves ($I_{DS}$–$V_{TG}$) of the $MoS_2$ transistor at different back-gate voltages. **b**, $I_{DS}$–$V_{TG}$ of the $WSe_2$ transistor (p-FET) and $MoS_2$ transistor (n-FET) at $V_{BG}=-40$ V. They were measured at $V_{DS}=1$ V (n-FET) and $V_{DS}=-1$ V (p-FET). The inset shows the circuit diagram of the CMOS inverter. $V_{DD}$, $V_{IN}$ and $V_{OUT}$ stand for the supply voltage, input voltage and output voltage, respectively. **c**, Voltage transfer curves of a CMOS inverter built on a $WSe_2$ p-type and $MoS_2$ n-type transistor. The inset shows the voltage gain ($-dV_{OUT}/dV_{IN}$) of the inverter. **d**, Instantaneous power consumed by the inverter against $V_{IN}$.

employing hBN or high-$\kappa$ dielectrics, such as $HfO_2$ and $Al_2O_3$, in terms of $I_{on}/I_{off}$ and SS. A large $I_{on}/I_{off}$ is indispensable for the explicit recognition of the on and off states for practical digital electronics. A smaller SS means more abrupt switching of the transistor between the on and off states because SS represents the minimum required change in the gate voltage for a tenfold increase in $I_{DS}$. In addition, the magnitude of the required gate voltage also depends on the initial doping level of $MoS_2$, which shifts the $I_{DS}$–$V_{BG}$ curves close to or away from the zero gate voltage (as explained above). The required gate voltages for the corresponding $I_{on}/I_{off}$ and SS are labelled in Fig. 3f for comparison. As can be seen, the magnitude of the required gate voltages of our STO-gated $MoS_2$ transistors is also among the lowest.

## Low-power CMOS inverter

The top-gate transfer characteristics of our $MoS_2$ transistors can be tuned by $V_{BG}$ (Fig. 4a). As $V_{BG}$ decreases, the $I_{DS}$–$V_{TG}$ curves shift monotonously in the positive direction. At a large negative $V_{BG}$, the transistor transforms into the enhancement mode, which means the threshold voltage ($V_{TH}$) becomes positive, and a positive $V_{TG}$ is required to switch on the transistor. In particular, with a back-gate biasing of −30 V, $I_{DS}$ is below 1 pA at $V_{TG}=0$ V. However, due to the preserved low SS, $I_{DS}$ reaches over 1 μA at $V_{TG}$ of only 1 V, displaying an $I_{on}/I_{off}$ of over $10^7$ (Fig. 4b). These merits demonstrate that our top-gated transistor can operate with a very low standby power consumption. It is worth noting that both dynamic and static power consumed by back-gate biasing are negligible since $V_{BG}$ is fixed and the d.c. current through the relatively thick $SiO_2$ is negligible. Tuning $V_{TH}$ by back-gate biasing in this work is analogous to the back-gate biasing strategy in advanced silicon-on-insulator and FinFET technologies[52,53]. Properly scaling the thickness of the bottom $SiO_2$ may reduce the required $V_{BG}$ to a value comparable to $V_{TG}$. The combination of near-ideal subthreshold slope, large $I_{on}/I_{off}$ and small operation voltage of our transistors is especially useful for low-power electronic applications.

Low-power digital circuits are critical to extend the service time of ubiquitous portable devices that rely on batteries, as well as to avoid overheating that leads to the malfunction of processors. As usually implemented for emerging materials and technologies[54,55], the potential of our STO-gated transistors for low-power digital circuits was verified by fabricating and testing inverters (or 'NOT' logic gates), the basic functional unit in CMOS digital circuits. A CMOS inverter (circuit diagram shown in Fig. 4b, inset) consists of a p-type and n-type transistor in series and their conductance is simultaneously controlled by a single gate voltage ($V_{IN}$). It outputs a logic state that opposes the input and these logic states are represented by

the respective voltage levels. To fabricate the CMOS inverter, we realized p-type transistors with a local STO top gate through chemical doping and back-gate biasing of $WSe_2$ (Supplementary Fig. 10). The transfer characteristic of the $WSe_2$ transistor (Fig. 4b) reveals $I_{on}/I_{off}$ of ~$10^7$ within the $V_{TG}$ range of ±1 V. Connecting the $WSe_2$ and $MoS_2$ transistors in the inverter configuration, we obtained an excellent inversion action (voltage transfer characteristics are shown in Fig. 4c). When the input voltage ($V_{IN}$) is zero (corresponding to logic '0'), the output voltage ($V_{OUT}$) approaches the supply voltage ($V_{DD}$), corresponding to logic '1'. On the contrary, when $V_{IN}$ is increased to a higher value (logic '1'), $V_{OUT}$ is close to zero (logic '0'). Benefitting from the gate-tuneable $I_{DS}$–$V_{TG}$ characteristics of our $MoS_2$ transistors, the inverter functions well at totally positive voltages, a requirement for practical applications. The peak values of voltage gain (10.5 at $V_{DD}=0.5$ V and 14.2 at $V_{DD}=1.0$ V), defined as $-dV_{OUT}/dV_{IN}$, are far greater than unity, demonstrating that our inverter is robust to errors and suitable for multistage logic circuits.

The total power consumed by an inverter in practical CMOS digital circuits include dynamic, static and short-circuit power[56]. The dynamic power results from the charging and discharging of the next-stage metal–oxide–semiconductor capacitor during switching and is proportional to the square of the operation voltages. Therefore, the minimized operation voltages of our transistors should be highly beneficial for a reduction in dynamic power. To analyse the static and short-circuit power consumed by our inverter, we plotted the instantaneous power against $V_{IN}$ (Fig. 4d). The instantaneous power is equal to $V_{DD}\times I_{DD}$, where $I_{DD}$ is the current flowing from supply to ground. The static power, that is, the power consumed at idle '0' or '1' states, comes mainly from subthreshold conduction. The static power consumed by our inverter is shown to be at the picowatt level, which is difficult to achieve with typical 2D semiconductor-based CMOS inverters due to subthreshold current still consuming considerable power at $V_{IN}=0$ V. The short-circuit power, which is the instantaneous power at $V_{IN}$ other than the '0' and '1' states, has peak values of 21 nW at $V_{DD}=0.5$ V and 0.34 μW at $V_{DD}=1.0$ V. Although these values are not outstanding, the short-circuit power makes up a very small portion of the total power because the inverter stays at the '0' and '1' states for most of the time during each functioning cycle of digital circuits[56]. It is also worth mentioning that our locally gated $WSe_2$ transistors operate in the depletion mode. This fact limits the voltage gain, increases the required $V_{IN}$ (higher than the respective $V_{DD}$) to switch off the p-type $WSe_2$ transistor of the inverter and deteriorates the short-circuit power. The realization of enhancement-mode p-type transistors, whose performance matches the $MoS_2$ n-type transistors, should improve the gain and power consumption further.

## Conclusions

We have shown that thin films of high-κ STO can be integrated with 2D materials using a van der Waals approach. Using stacked STO as the top dielectric material, we created a $MoS_2$ n-type transistor that, due to the large dielectric constant of STO and excellent interfacial quality, exhibits an $I_{on}/I_{off}$ value of over $10^8$ at a supply voltage of 1 V and minimum SS of 66 mV dec$^{-1}$. We also created a CMOS inverter with picowatt standby power consumption by combining the n-type $MoS_2$ transistors with p-type $WSe_2$ transistors. Our van der Waals integration strategy circumvents many technical problems of established methods, which tend to deteriorate the interface quality or restrict material combinations during fabrication, and other complex oxides and 2D materials may be able to adopt this strategy to construct high-performance devices and circuits. Our approach provides a potential route to a wide range of hybrid oxide–oxide and oxide–2D material heterostructures, which could be used to create advanced forms of electronics such as hybrid spintronics and oxide-based twistronics.

## Methods

**Material preparation.** STO/SAO bilayer films were sequentially grown by PLD on $TiO_2$-terminated STO(001) substrates with sintered SAO and STO ceramic targets. Before the deposition, the STO substrates were buffered HF etched and then annealed at 950 °C to achieve a $TiO_2$-terminated atomically flat surface[57]. During growth, the target materials were vapourized by irradiation of an excimer laser (wavelength $\lambda=248$ nm) operated with a repetition rate of 2 Hz and a laser fluence of 1.8 J cm$^{-2}$, whereas the STO substrates were kept at 760 °C. The partial pressures of oxygen ($P_{O2}$) for the growth of SAO and STO were $1\times10^{-6}$ and $1\times10^{-2}$ torr, respectively. After deposition, all the samples were cooled down to room temperature at the rate of 10 °C min$^{-1}$ under a $P_{O2}$ value of $1\times10^{-2}$ torr.

$SiO_2$/Si substrates were treated with oxygen plasma (CUTE-1MPR dual-mode plasma processing system, Femto Science) for 5 min at a power of 50 W before mechanical exfoliation and transfer of graphene (Gr), $MoS_2$ and $WSe_2$. To transfer $MoS_2$ on Gr, $MoS_2$ flakes on $SiO_2$/Si were lifted off by PDMS sheets using a wedging transfer method[58]. Briefly, the surface of the $SiO_2$/Si substrate supporting the target $MoS_2$ flake was covered with a PDMS sheet. Then, DI water was added to the surrounding of the PDMS sheet, and it slowly penetrated into the gap between PDMS and $SiO_2$ because the $SiO_2$ surface is hydrophilic after oxygen plasma treatment. The PDMS sheet with the target $MoS_2$ flake finally floated up on the surface of DI water. The PDMS/$MoS_2$ stack was then picked up, dried and transferred onto graphene on another $SiO_2$/Si substrate using the method described earlier.

**Material characterization.** HAADF-STEM images were obtained at 300 kV using an aberration-corrected FEI Titan Themis G2 instrument. The AFM images were measured in the tapping mode using a Cypher ES Environmental AFM (Asylum Research). Raman spectra were measured on a WITec alpha300 confocal Raman system with an excitation wavelength of 532 nm.

**Device fabrication.** Drain, source and top-gate electrodes were defined by electron-beam lithography followed by thermal deposition of 5 nm Cr and 60–100 nm Au.

**Electrical measurements.** The transistors were bonded to chip carriers and measured using a Keithley 2635b sourcemeter and two Keithley 2450 sourcemeters in a shielded vacuum chamber (0.1 mbar) at room temperature. The CMOS inverters were measured with an additional Keithley 2230G power supply. Two-terminal $I$–$V$ measurements were performed using the Keithley 2635b sourcemeter. Hall-effect measurements were carried out in a helium atmosphere (~0.1 torr) in an Oxford TeslatronPT cryostation equipped with a magnetic field of up to 8 T.

## Data availability

The data that support the conclusions in this paper are available from the corresponding authors upon reasonable request.

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## Author contributions

A.J.Y. and X.R.W. conceived the idea and designed the experiments. A.J.Y. fabricated the heterostructures and devices. A.J.Y., assisted by K. Huang and C.Y., performed the electrical measurements and analysis. K. Han grew the oxides. W.W. performed the Raman characterization. Rui Zhu, Ruixue Zhu, J.X. and P.G. performed the STEM characterization and analysis. A.J.Y. and X.R.W. wrote the manuscript. All the authors contributed to the scientific discussion and commented on the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

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